(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 February 2004 (26.02.2004)

PCT

(10) International Publication Number
WO 2004/017381 A2

(51) International Patent Classification[7]: H01L

(21) International Application Number: PCT/US2003/025954

(22) International Filing Date: 19 August 2003 (19.08.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/405,085 19 August 2002 (19.08.2002) US

(71) Applicant (*for all designated States except US*): THE TRUSTEES OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK [US/US]; 116th Street and Broadway, New York, NY 10027 (US).

(72) Inventor; and
(75) Inventor/Applicant (*for US only*): IM, James, S. [US/US]; 520 West 114th Street, Apt. 74, New York, NY 10025 (US).

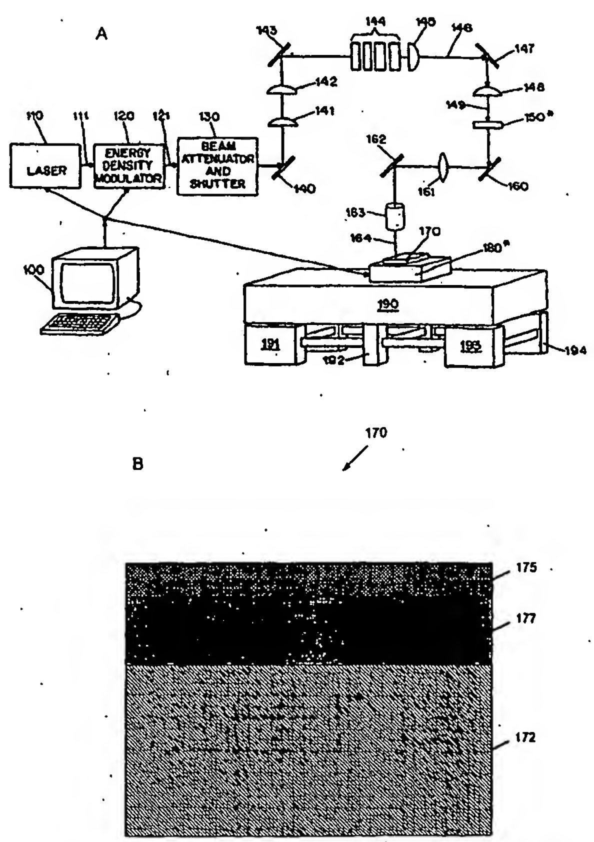
(74) Agents: TANG, Henry et al.; Baker Botts L.L.P., 30 Rockefeller Plaza, New York, NY 10112-4498 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: PROCESS AND SYSTEM FOR LASER CRYSTALLIZATION PROCESSING OF FILM REGIONS ON A SUBSTRATE TO MINIMIZE EDGE AREAS, AND STRUCTURE OF SUCH FILM REGIONS



(57) Abstract: A process and system for processing a thin film sample are provided. In particular, a beam generator can be controlled to emit at least one beam pulse. The beam pulse is then masked to produce at least one masked beam pulse, which is used to irradiate at least one portion of the thin film sample. With the at least one masked beam pulse, the portion of the film sample is irradiated with sufficient intensity for such portion to later crystallize. This portion of the film sample is allowed to crystallize so as to be composed of a first area and a second area. Upon the crystallization thereof, the first area includes a first set of grains, and the second area includes a second set of grains whose at least one characteristic is different from at least one characteristic of the second set of grains. The first area surrounds the second area, and is configured to allow an active region of a thin-film transistor ("TFT") to be provided at a distance therefrom.

BEST AVAILABLE COPY

WO 2004/017381 A2

WO 2004/017381 A2

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

PROCESS AND SYSTEM FOR LASER CRYSTALLIZATION PROCESSING OF FILM REGIONS ON A SUBSTRATE TO MINIMIZE EDGE AREAS, AND STRUCTURE OF SUCH FILM REGIONS

SPECIFICATION

RELATED APPLICATION

This application claims priority to United States Provisional Application No. 60/405,085, which was filed on August 19, 2002, and is incorporated by reference.

NOTICE OF GOVERNMENT RIGHTS

The U.S. Government may have certain rights in this invention pursuant to the terms of the Defense Advanced Research Project Agency award number N66001-98-1-8913.

FIELD OF THE INVENTION

The present invention relates to techniques for processing of thin films, and more particularly to techniques for processing semiconductor thin films to reduce non-uniform edge areas of the crystallized regions of the thin film so that at least an active region of an electronic devices, such as a thin-film transistor ("TFT"), can be placed away from such non-uniform edge areas.

BACKGROUND OF THE INVENTION

Semiconductor films, such as silicon films, are known to be used for providing pixels for liquid crystal display devices and organic light emitting diode displays. Such films have previously been processed (i.e., irradiated by an excimer laser and then crystallized) via excimer laser annealing ("ELA") methods. However, the semiconductor films processed using such known ELA methods often suffer from microstructural non-uniformities such as edge effects, which manifest themselves in availing a non-uniform performance of thin-film transistor ("TFT") devices fabricated on such films.

Such non-uniformity in edge regions is particularly problematic in that the visual transitions between the neighboring pixels corresponding to the irradiated and crystallized areas of the semiconductor thin film on the liquid crystal displays ("LCDs") or organic light emitting diode displays are not as smooth as could be desired, and may even be visible in certain cases, which is undesired. This is also because the edge effects promote a low performance in TFT devices whose active regions are provided thereon.

Significant efforts have been made into the refinement of "conventional" ELA (also known as line-beam ELA) processes in the attempt to reduce or eliminate non-uniformities on the crystallized areas of the semiconductor thin film. For example, U.S. Patent No. 5,766,989 issued to Maegawa et al., the entire disclosure of which is incorporated herein in its entirety by reference, describes the ELA methods for forming polycrystalline thin film and a method for fabricating a thin-film transistor. This publication attempts to address the problem of non-uniformity of characteristics across the substrate, and provide certain options for apparently suppressing such non-uniformities. However, details of previous approaches make it impossible to completely eliminate the non-uniformities that are introduced from the edge areas (which are typically between 100µm to 1,000µm or higher). Thus, the cross sectional area of the portions of the semiconductor thin film on which the TFT devices could be placed would be significantly reduced due to such disadvantageous edge effects causing large non-uniform edge areas which border these portions.

For example, one such conventional ELA process uses a long and narrow shaped beam 800 as shown in Figs. 11A and 11B. The fluence of this beam 800 is above a melting level in a center portion 810 thereof, while side areas 820 of this beam 800 have a fluence that is gradually reduced at the edges thereof. The width of the center portion 810 of the beam 800 may be 1cm and the length thereof may be 30cm. In this manner, the beam can potentially irradiate the entire semiconductor thin film during one pass across it. As shown in Fig. 11B, portions 830 of the side areas 820 of the beam 800 can be provided between the melting level and the crystallization threshold. Thus, when the beam 800 irradiates particular portions of the

semiconductor thin film which is then crystallized, such portions would likely have an edge regions in thus irradiated and crystallized areas of the semiconductor thin film that are likely to have large non-uniform edge regions spatially corresponding to the portions 830 of the beam 800. The edge regions are known to be disadvantageous for placing the TFT devices (and especially their active regions) thereon.

Attempts have been made to eliminate the edge effect (i.e., non-uniformity of the edge areas) of the irradiated and crystallized portions of the semiconductor film. U.S. Patent No. 5,591,668 issued to Maegawa et al. tries to minimize these edge areas by using a substantially square shaped beams (rotated 45° and having rounded peaks) that sequentially overlap one another using a laser annealing method. However, such conventional procedure would require multiple irradiation by the beam pulses of the same areas, and the processing of the semiconductor film would be somewhat slow.

Accordingly, it is preferable to irradiate and crystallize at least some of the areas of the semiconductor films by passing the beam pulses through a mask in a way so as to eliminate the problem caused by such edge effect by clearly defining the profile of the beam pulse. It is preferable to significantly reduce the spatial scale associated with the edge region so as to make it possible to have such regions be provided away from the active regions of the TFT devices. In addition, multiple irradiations of the same area on the semiconductor film would therefore no longer be necessary.

SUMMARY OF THE INVENTION

Therefore, one of the objects of the present invention is to provide an improved process and system which can make the edge regions of the crystallized areas of the semiconductor thin film relatively small (e.g., one such region can be smaller than the distance between the adjacent TFT devices). Thus, it is possible to place the active regions of the TFT devices on the semiconductor thin film away from these edge regions. Another object of the present invention is to increase the speed to process the semiconductor films for their use with the liquid crystal displays and/or organic light emitting diode displays. Still another object of the present is to have a

capability for utilizing various fluences of the beam pulse for irradiating the areas of the semiconductor thin film, so long as such fluence induces a crystallization of the irradiated areas of the semiconductor thin film.

In accordance with at least some of these objectives as well as others that will become apparent with reference to the following specification, it has now been determined that the reduction the size of the edge regions of the irradiated and crystallized areas of the semiconductor thin film is advantageous to reduce the edge effect. It was also ascertained that the grains provided in the edge regions of such areas are different from the grains of the areas that are arrangement, e.g., between two oppositely-spaced edge regions of the semiconductor thin film. Further, it was determined that the use of the two-dimensional mask to pass the beam pulse there through configured the profile of the resultant masked beam pulse to be well defined, thus decreasing or eliminating the portion of the beam pulse which may have a gradually-reducing fluence level that may cause the undesired edge effect.

In one exemplary embodiment of the present invention, a process and system for processing a semiconductor thin film sample are provided. In particular, a beam generator can be controlled to emit at least one beam pulse. The beam pulse is then masked to produce at least one masked beam pulse, which is used to irradiate at least one portion of the semiconductor thin film sample. With the at least one masked beam pulse, the portion of the film sample is irradiated with sufficient intensity for such portion to later crystallize. This portion of the film sample is allowed to crystallize so as to be composed of a first area and a second area. Upon the crystallization thereof, the first area includes a first set of grains, and the second area includes a second set of grains whose at least one characteristic is different from at least one characteristic of the second set of grains. The first area surrounds the second area, and is configured to allow an active region of a thin-film transistor ("TFT") to be provided at a distance therefrom.

In another embodiment of the present invention, the masked beam pulse can have the intensity sufficient to completely melt the irradiated portion of the semiconductor thin film sample throughout its thickness (or partially melt such

portion). The active region of the TFT can be situated within the second area. The second area may correspond to at least one pixel. The second area has a cross-section for facilitating thereon all portions of the TFT. A size and a position of the first area with respect to the second area are provided such that the first area provides either no effect or a negligible effect on a performance of the TFT.

According to still another embodiment of the present invention, a location of the first area can be determined so as to avoid a placement of the active region of the TFT thereon. The beam pulse may include a plurality of beamlets, and the first and second areas can be irradiated by the beamlets. The semiconductor thin film sample may be a silicon the film sample. The semiconductor thin can be composed of at least one of silicon and germanium, and may have a thickness approximately between 100Å and 10,000Å. The first set of grains provided in the first area may be laterally-grown grains.

According yet another embodiment of the present invention, a semiconductor thin film sample includes at least one section irradiated by at least one masked beam pulse which is configured to irradiate the at least one section of the sample for a later crystallization thereof. The irradiated portion of the film sample is crystallized to include a first area and a second area. Upon the crystallization thereof, the first area includes a first set of grains, and the second area includes a second set of grains whose at least one characteristic is different from at least one characteristic of the second set of grains. The first area surrounds the second area, and is configured to allow an active region of a thin-film transistor ("TFT") to be provided at a distance therefrom.

The accompanying drawings, which are incorporated and constitute part of this disclosure, illustrate a preferred embodiment of the invention and serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a schematic block diagram of an exemplary embodiment of an irradiation system according to the present invention which irradiates particular areas of a semiconductor thin film of a sample such that these areas have a relatively small edge regions;

Fig. 1B is an enlarged cross-sectional side view of the sample which includes the semiconductor thin film;

Fig. 2 is a top exploded view of an exemplary embodiment of the sample conceptually subdivided, and having a semiconductor thin film thereon on which a process according to the present invention is performed for the entire surface area a semiconductor thin film using the exemplary system of Fig. 1A;

Fig. 3 is a top view of a first exemplary embodiment of a mask according to the present invention which has a beam-blocking area surrounding one open or transparent area, and which can be used with the exemplary system of Fig. 1A to mask the beam pulses generated by a laser beam source into a patterned beam pulse, such that such masked beam pulses irradiate the particular areas on the semiconductor film thereby reducing the edge regions provided at the peripheries of such areas;

Figs. 4A-4D are irradiations, by the radiation beam pulse which is masked by the mask of Fig. 3, and then re-solidifications and crystallizations of the particular portions of the semiconductor film provided on the sample for an first exemplary conceptual column of the sample at various sequential stages of the exemplary embodiment according to the process of the present invention in which the edge regions of the particular portions are significantly reduced;

Figs. 4E-4F are irradiations, by the radiation beam pulse which is masked by the mask of Fig. 3, and then re-solidifications and crystallizations of the particular portions of the semiconductor film provided on the sample for an second exemplary conceptual column of the sample at two exemplary sequential stages of the processing according to the process of the present invention, which continue from the first conceptual column of Figs. 4A-4D;

Fig. 5A is a top view of a second exemplary embodiment of the mask according to the present invention which has a beam-blocking area surrounding multiple small open or transparent areas or slits, and which can be used with the exemplary system of Fig. 1A to mask the beam pulses generated by a beam source into patterned beamlets, such that such masked beamlet pulses irradiate the particular areas on the semiconductor film whose edge regions are significantly reduced;

Fig. 5B is an enlarged view of the beamlets of the second embodiment of the mask illustrated in Fig. 5A;

Figs. 6A-6D are irradiations, by the radiation beam pulse intensity pattern which is masked by the mask of Fig. 5, and then re-solidifications and crystallizations of the particular portions of the semiconductor film provided on the sample for the first conceptual column of the sample at various sequential stages of the first exemplary embodiment of the exemplary embodiment according to the process of the present invention;

Fig. 7 is an illustration of the semiconductor thin film provided on the sample, and such thin film being irradiated by the beam pulse having a cross-section that is patterned by a mask having a beam-blocking area surrounding one long and narrow open or transparent area, and which can be used with the exemplary system of Fig. 1A;

Fig. 8A is an illustration of the two particular areas irradiated, re-solidified and crystallized areas corresponding to the areas of Figs. 4D and 6D in which the edge regions of each of these areas are provided away from the entire TFT device;

Fig. 8B is an illustration of the two particular areas irradiated, re-solidified and crystallized areas corresponding to the areas of Figs. 4D and 6D in which the edge regions of these two areas are provided away from the entire cross-section of the active region of the TFT device, while other regions are provided on such edge regions;

Fig. 9 is a flow diagram representing an exemplary processing procedure of the present invention under at least partial control of a computing

arrangement of Fig. 1A using the exemplary techniques of the present invention of Figs. 4A-4F and 6A-6D;

Fig. 10 is a flow diagram representing another exemplary processing procedure of the present invention under at least partial control of a computing arrangement of Fig. 1A using the exemplary techniques of the present invention of Figs. 4A-4F and 6A-6D, and in which the beam source of Fig. 1A is triggered based on the positions of the semiconductor film with respect to the impingement of the beam;

Fig. 11A is a perspective cut-away view of a profile of a long and narrow beam which is shaped by a projection irradiation using conventional systems and processes;

Fig. 11B is a graph of the fluence of the beam of Fig. 11A against the spatial profile of the beam generated by the conventional systems and processes; and

Fig. 12 is a exemplary graph of the fluence of the beam against the spatial profile of the beam generated by the system and process according to the present invention which reduces the edge regions of the particular portions of the semiconductor thin film irradiated by such beam.

DETAILED DESCRIPTION

It should be understood that various systems according to the present invention can be utilized to mask, irradiate and crystallize one or more portions on the semiconductor (e.g., silicon) film so as to reduce edge areas of these portions and to place at least an active region of a thin-film transistor ("TFT") away from the edge regions of such portions. The exemplary embodiments of the systems and process to achieve such areas as well as of the resulting crystallized semiconductor thin films shall be described in further detail below. However, it should be understood that the present invention is in no way limited to the exemplary embodiments of the systems processes and semiconductor thin films described herein.

In particular, Fig. 1A shows a system according to the present invention which is used on a sample 170 which has an amorphous silicon thin film

thereof that is being irradiated by masked irradiation beam pulses to promote the masked irradiation, solidification and crystallization of the particular areas of the semiconductor thin film in which the edge regions are minimized. The exemplary system includes a beam source 110 (e.g., a Lambda Physik model LPX-315I XeCl pulsed excimer laser) emitting an irradiation beam (e.g., a laser beam), a controllable beam energy density modulator 120 for modifying the energy density of the laser beam, a MicroLas two plate variable attenuator 130, beam steering mirrors 140, 143, 147, 160 and 162, beam expanding and collimating lenses 141 and 142, a beam homogenizer 144, a condenser lens 145, a field lens 148, a projection mask 150 which may be mounted in a translating stage (not shown), a 4×-6× eye piece 161, a controllable shutter 152, a multi-element objective lens 163 for focusing a radiation beam pulse 164 onto the sample 170 having the semiconductor thin film to be processed mounted on a sample translation stage 180, a granite block optical bench 190 supported on a vibration isolation and self-leveling system 191, 192, 193 and 194, and a computing arrangement 100 (e.g., a general purpose computer executing a program according to the present invention or a special-purpose computer) coupled to control the beam source 110, the beam energy density modulator 120, the variable attenuator 130, the shutter 152 and the sample translation stage 180.

The sample translation stage 180 is preferably controlled by the computing arrangement 100 to effectuate translations of the sample 170 in the planar X-Y directions, as well as in the Z direction. In this manner, the computing arrangement 100 controls the relative position of the sample 40 with respect to the irradiation beam pulse 164. The repetition and the energy density of the irradiation beam pulse 164 are also controlled by the computer 100. It should be understood by those skilled in the art that instead of the beam source 110 (e.g., the pulsed excimer laser), the irradiation beam pulse can be generated by another known source of short energy pulses suitable for completely melting throughout their entire thickness selected areas of the semiconductor (e.g., silicon) thin film of the sample 170 in the manner described herein below. Such known source can be a pulsed solid state laser, a chopped continuous wave laser, a pulsed electron beam and a pulsed ion beam, etc. Typically, the radiation beam pulses generated by the beam source 110 provide a

beam intensity in the range of 10 mJ/cm^2 to $1J/cm^2$ (e.g., $500mJ/cm^2$) a pulse duration (FWHM) in the range of 10 to 103 nsec, and a pulse repetition rate in the range of 10 Hz to 104 Hz.

While the computing arrangement 100, in the exemplary embodiment of the system shown in Fig. 1A, controls translations of the sample 170 via the sample stage 180 for carrying out the processing of the semiconductor thin film of the sample 170 according to the present invention, the computing arrangement 100 may also be adapted to control the translations of the mask 150 and/or the beam source 110 mounted in an appropriate mask/laser beam translation stage (not shown for the simplicity of the depiction) to shift the intensity pattern of the irradiation beam pulses 164, with respect to the semiconductor thin film of the sample 170, along a controlled beam path. Another possible way to shift the intensity pattern of the irradiation beam pulse is to have the computer 100 control a beam steering mirror. The exemplary system of Fig. 1 may be used to carry out the processing of the silicon thin film of the sample 170 in the manner described below in further detail. It should also be understood that it is possible to exclude the mask 150 from the system according to the present invention. Without such mask 150, the beam source 11 0, the energy density modulator, the beam attenuator and/or other components of the system of the present invention can be used to shape the beam 149 so as to impinge and irradiate selected portions of the semiconductor thin film of the sample 170.

As illustrated in Fig. 1B, the semiconductor thin film 175 of the sample 170 can be directly situated on e.g., a glass substrate 172, and may be provided on one or more intermediate layers 177 there between. The semiconductor thin film 175 can have a thickness between 100Å and 10,000Å (1μm) so long as at least certain necessary areas thereof can be completely melted throughout their entire thickness. According to an exemplary embodiment of the present invention, the semiconductor thin film 175 can be composed of silicon, germanium, silicon germanium (SeGe) all of which preferably having low levels of impurities. It is also possible to utilize other elements or semiconductor materials for the semiconductor thin film 175. The intermediary layer 177, which is situated immediately underneath the semiconductor thin film 175, can be composed of silicon oxide (SiO_2), silicon nitride (Si_3N_4), and/or

mixtures of oxide, nitride or other materials that are suitable for promoting nucleation and small grain growth within the designated areas of the semiconductor thin film 175 of the sample 170. The temperature of the glass substrate 172 can be between room temperature and 800°C. Higher temperatures of the glass substrate 172 can be accomplished by preheating the substrate 172 which would effectively allow larger grains to be grown in the nucleated, re-solidified, and then crystallized areas of the semiconductor thin film 175 of the sample 170 due to the proximity of the glass substrate 172 to the thin film 175.

Fig. 2 shows an enlarged view of an exemplary embodiment of the semiconductor thin film 175 (e.g., an amorphous silicon thin film) of the sample 170, and the relative translation paths of the beam pulse 164 with respect to the locations on the sample 170. This exemplary sample 170 has exemplary dimensions of 40 cm in the Y direction by 30 cm in the X direction. The sample 170 can be conceptually subdivided into a number of columns (e.g., a first conceptual column 205, a second conceptual column 206, a third conceptual column 207, etc.). The location/size of each conceptual column may be stored in a storage device of the computing arrangement 100, and utilized by the computing 100 for later controlling the translation of the sample 170, and/or firing of the beam in by the beam source 110 at such relative locations of the semiconductor thin film 175, or on other locations that are based on the stored locations. Each of the conceptual columns 205, 206, 207, etc. is dimensioned, e.g., ½ cm in the Y direction by 30 cm in the X direction. Thus, if the sample 170 is sized 40 cm in the Y direction, the sample 150 may be conceptually subdivided into eighty (80) columns. The sample 170 may also be conceptually subdivided into such columns having other dimensions (e.g., 1 cm by 30 cm columns, 2 cm by 30 cm columns, 2 cm by 30 cm columns, etc.). In fact, there is absolutely no restrictions on the dimensions of the conceptual columns of the sample 170 so long as the masked beam pulse 164 is capable of irradiating certain areas of the semiconductor thin film 175 in such columns to promote crystallization within such areas.

In particular, according to the present invention, it is important to provide relatively small edges region at the peripheries of these areas of the film

sample 175 so as to allow at least the active region of the TFT device to be placed away from these very small edge regions. The small size of the edge regions is primarily due to the use of the mask 150 to generate a sharp pro file of the beam 111 as the masked beam pulse 164 The location/dimension of each conceptual column, and the locations thereof, are stored in the storage device of the computing arrangement 100, and utilized by such computing arrangement 100 for controlling the translation of the translation stage 180 with respect to the beam pulse 164 and/or the firing of the beam 111 by the beam source 110 at those locations of the semiconductor thin film sample, or on other locations.

For example, the semiconductor thin film 175 can be irradiated by the beam pulse 164 whose profile is defined using the mask 150 according to a first exemplary embodiment of the present invention as shown in Fig. 3. The first exemplary mask 150 is sized such that its cross-sectional area is larger than that of the cross-sectional area of the masked beam pulse 164. In this manner, the mask 150 can pattern the pulsed beam to have a shape and profile directed by the open or transparent regions of the mask 150. This can be commonly referred to as a "two-dimensional projection", which generally the shape of the beam, and reduces such shape in all directions. Such projection is significantly different from a single axis projection which does not utilize a mask, and merely shapes and reduces the beam in one direction. Fig. 12 show a preferable profile 850 of the masked beam pulse 164 as the pulse 149 is passed through the mask 150. This profile 850 is well defined so as to minimize the edge regions provided at the peripheries of the irradiated portions of the semiconductor thin film 175.

In this exemplary embodiment shown in Fig. 3, the mask 150 includes a beam-blocking section 155 and an open or transparent section 157. The beam-blocking section 155 prevents those areas of the pulsed beam impinging such section 155 from being irradiated there-through, thus preventing the further entering the optics of the exemplary system of the present invention shown in Fig. 1A to irradiate the corresponding areas of the semiconductor thin film 175 provided on the sample 170. In contrast, the open or transparent section 157 allows the portion of the beam pulse 164 whose cross-section corresponds to that of the section 157 to enter the

optics of the system according to the present invention, and irradiate the corresponding areas of the semiconductor thin film 175. In this manner, the mask 150 is capable of patterning the beam pulse 164 so as to impinge the semiconductor thin film 175 of the sample 170 at predetermined portions thereof as shall be described in further detail below.

According to the present invention, the masked beam pulse 164 can have various energy fluences. For example, such fluence of the masked beam pulse 164 can small, but which promotes an explosive crystallization. The fluence of the beam pulse 164 can be higher than the small fluence to promote partial melting of the irradiated portions of the semiconductor thin film 175, and then crystallization of such portions. In addition, the fluence can be higher than the fluence promoting partial melting so as to allow a near-complete melting of the portions of the semiconductor thin film 175. Furthermore, the fluence of the masked beam pulse 164 can be high enough to completely melt the above-described irradiated portions of the thin film 175. In summary, the fluence should be large enough to allow the portions of the semiconductor thin film 175 to crystallize after being irradiated by the masked beam pulse 164.

A first exemplary embodiment of the process according to the present invention shall now be described with reference to the irradiation of the semiconductor thin film 175 of the sample 170 as illustrated in Figs. 4A-4F. In this exemplary process of the present invention, the beam pulse 149 is shaped by the exemplary mask 150 of Fig. 3, and the exemplary irradiation and/or impingement of the semiconductor thin film 175 of the sample 170 is shown in Fig. 2. For example, the sample 170 may be translated with respect to the beam pulse 164, either by moving the mask 150 or the sample translation stage 180, in order to irradiate selective areas of the semiconductor thin film 175 of the sample 170. For the purposes of the foregoing, the length and width of the laser beam 149 may be greater than 1 cm in the X-direction by ½ cm in the Y-direction (e.g., a rectangular shape) so that it can be shaped by the mask 150 of Fig. 3. However, it should be understood the pulsed laser beam 149 is not limited to such shape and size. Indeed, other shapes

and/or sizes of the laser beam 149 are, of course, achievable as is known to those having ordinary skill in the art (e.g., shapes of a square, triangle, circle, etc.).

After the sample 170 is conceptually subdivided into columns 205, 206, 207, etc., a pulsed laser beam 111 is activated (by actuating the beam source 110 using the computing device 100 or by opening the shutter 130), and produces the pulsed laser beamlets 164 which impinges on a first location 220 which is away from the semiconductor thin film 175. Then, the sample 170 is translated and accelerated in the forward X direction under the control of the computing arrangement 100 to reach a predetermined velocity with respect to the fixed position beamlets in a first beam path 225.

In one exemplary variation of the process of the present invention, the pulsed beamlets 164 can reach a first edge 210' of the sample 170 preferably when the velocity of the movement of the sample 170 with respect to the pulsed laser beam 149 reaches the predetermined velocity. Then, the sample 170 is continuously (i.e., without stopping) translated in the -X direction at the predetermined velocity so that the pulsed beamlets 164 continue irradiating successive portions of the sample 170 for an entire length of a second beam path 230.

After passing the first edge 210', the beam pulse 164 impinges and irradiates a first area 310 of the semiconductor thin film 175, preferably with enough intensity to irradiate such area so that the crystallization thereof is then promoted, as illustrated in Fig. 4A. The fluence of the masked beam pulse 164 should preferably be large enough to promote crystallization of the irradiated portions of the semiconductor thin film 175. Then, as shown in Fig. 4B, this first area 310 is allowed to crystallize, thereby forming two regions therein – a first center region 315 and a first minimized edge region 318. The first center region 315 is formed after the irradiation of the first area 310 by the masked beam pulse 164. The dimensions of this center region 315 are slightly smaller that the dimensions of the masked beam pulse 164 irradiating the first area 310, with the first center region 315 being surrounded by the first edge region 318 (the details of which are described herein below). Again, the size of the first edge region 318 is minimized due to the masking of the beam pulse 149 to become the

masked beam pulse 164 which preferably has the profile 850 illustrated in Fig. 12. It should be note that the characteristics of the grains (e.g., length, orientation, etc.) of the first center area 315 and the characteristics of the first edge area 318 are different; such differences is one of the main reasons for the reduction of the edge regions.

The first edge region 318 can formed by laterally growing the grains from the borders between the unirradiated portions of the semiconductor thin film 175 and the first irradiated area 310. This is the case when the masked beam pulse 164 has the fluence to completely melt the first area 310. The grains in the first center region 318 grown from these borders toward the center of the first melted area for a predetermined small distance, to reach the first center region 315, and form a border there between. Of course, it should be understood that if the masked beam pulse 164 does not have enough intensity to completely melt the first area, grains are formed in the first edge region in any event. Generally, the grains of the first center region 315 are larger than those in the first edge region 318. This is preferably because the intensity of the masked beam pulse 164 is greater in the center thereof than at the edges. The predetermined distance is small because the beam pulse 149 is irradiated through the mask 149 to form the masked beam pulse 164 which does not have large gradually decreasing edge portions (e.g., portions 820 of the conventional beam pulse 800 as shown in Figs. 11A and 11B), and in fact preferable has the intensity pattern 850 illustrated in Fig. 12. For example, the predetermined distance can be 1 μm, while the width of the first center region may be slightly less than 1 cm.. Therefore, the first edge region 318 is significantly smaller that the first center region 315 which it surrounds. For the purposes of the present invention, it is un-desirable to position the active regions of the TFT devices on such edge regions, so that the active regions (and possibly the entire TFT devices) are placed away from these edge regions.

Thereafter, as shown in Fig. 4C, the sample 170 is continued to be translated (or the mask 150 is configured to be adjusted) such that the beam pulse 164 irradiates a second area 320 of the semiconductor thin film 175 in the manner discussed herein above for the first area 310. This second area 320 which can be a subsequent area immediately following the first area 320 in the first conceptual column 205 along the +X direction.

Similarly to the first area 310, the second area 320 crystallizes into a second center region 325 and a second edge region 328, which correspond to the characteristics and dimensions of the first center region 315 and the first edge region 318, respectively. If, during the irradiation of the second area 320 (and in an exemplary case of complete melting thereof), the masked beam pulse 164 slightly overlaps the first edge region 318, then upon crystallization, the grains in this region 318 seed and laterally grow a portion of the completed melted second area 320 which is immediately adjacent to the first edge region 318. In this manner, the adjacent section of the second edge region 328 is seeded by the first laterally-grown region 318 to laterally grow grains therefrom. Nevertheless, the second edge region 328 is still very small (e.g., 1μm) as compared to the second center area 325. The resultant crystallized second area 320 is illustrated in Fig. 4D. It is also within the scope of the present invention for the second area 320 to be provided at a distance from the crystallized first area 310. In this manner and in case of the complete melting of the second area 320, the sections of the second edge region 328 which is situated closest to the crystallized first laterally-grown region 318 can be seeded by the grains from an un-irradiated section between the first area 310 and the second area.

The first edge area 318 and/or the second edge area 328 are preferably sized such that the cross-sectional area thereof is smaller that the distance between the TFT device (especially the active regions thereof) which is situated in the first center region 315 and the TFT device situated in the second center region 325.

The translation and irradiation of the first conceptual column 205 of the semiconductor thin film 175 continues until all areas 310, 320, ..., 380, 390 (and their respective center regions 315, 325, ..., 385, 395 and edge regions 318, 328, ..., 388, 398) in this first conceptual column 205 is continued until the pulsed beamlets 164 reach a second edge 210" of the sample 170, as illustrated in Fig. 4E. The crystallization of the areas 310, 320, ..., 380, 390 along the first conceptual column 205 is performed in a substantially repetitive manner. When the beam pulse 164 passes the second edge 210", the translation of the sample 170 may be slowed with respect to the masked beam pulse 164 (in a third beam path 235) to reach a second location 240 (see Fig. 2). It should be noted that it is not necessary to shut down the

pulsed beam 111 after the masked beam pulse 164 has crossed the second edge 210" of the sample 170 because it is no longer irradiating the sample 170.

While being away from the sample 170 and the second edge 210", the sample is translated in a -Y direction to a third location 247 via a fourth beam path 245 so as to be able to irradiate the sections of the semiconductor thin film 175 along the second conceptual column 206. Then, the sample 170 is allowed to settle at that location 247 to allow any vibrations of the sample 170 that may have occurred when the sample 170 was translated to the third location 247 to cease. Indeed, for the sample 170 to reach the second conceptual column 206, it is translated approximately ½ cm for the columns having a width (in the -Y direction) of ½ cm. The sample 170 is then accelerated to the predetermined velocity via a fourth beam path 250 in the –X direction so that the impingement of the semiconductor thin film 175 by the beam pulse 164 reaches, and then bypasses the second edge 210".

Thereafter, the sample 170 is translated along a fifth beam path 255, and the exemplary process described above with respect to the irradiation of the first column 205 may then be repeated for the second conceptual column 206 to irradiate further areas 410, 420, and their respective center regions 415, 425 and edge regions 418, 428 while translating the sample in the +X direction. In this manner, all conceptual columns of the sample 170 can be properly irradiated. Again, when the beam pulse 164 reaches the first edge 210', the translation of the sample 170 is decelerated along a sixth beam path 260 to reach a fourth location 265. At that point, the sample 170 is translated in the –Y direction along the seven beam path 270 for the beam pulse to be outside the periphery of the sample 170 to reach fifth location 272, and the translation of the sample 170 is allowed to be stopped so as to remove any vibrations from the sample 170. Thereafter, the sample 170 is accelerated along the eighth beam path 275 in the –X direction so that the beam pulse 164 reaches and passes the first edge 210' of the sample 170, and the beam pulse 164 irradiates (e.g., to partially or completely melt) certain areas in the third conceptual column 207 so that they can crystallize in substantially the same manner as described above for the areas 310, 320, ..., 380, 390 of the first conceptual column 205 and the areas 410, 420, ... of the second conceptual column 206.

This procedure may be repeated for all conceptual columns of the semiconductor thin film 175, for selective columns of particular sections of the thin film 175 which are not necessarily conceptually subdivided into columns. In addition, it is possible for the computing arrangement 100 to control the firing of the beam 111 by the beam source 110 based on the predefined location stored in the storage device of the computing arrangement 100 (e.g., instead of irradiating the semiconductor thin film 175 by setting predetermined time period between the beam pulses or setting pulse durations). For example, the computing arrangement 100 can control the beams source 110 to generate the beam 111 and irradiate only at the predetermined locations of certain areas of the thin film 175 with its corresponding beam pulse 164, such that these locations are stored and used by the computing arrangement 100 to initiate the firing of the beam 111 which results in the irradiation by the beam pulse only when the sample 170 is translated to situate those areas directly in the path of the beam pulse 164. The beam source 110 can be fired via the computing arrangement 100 based on the coordinates of the location in the X direction.

In addition, it is possible to translate the sample 170 in a manner which is not necessary continuous, when the path of the irradiation of the beam pulse 164 points to the areas on the semiconductor thin film 175 to be melted and crystallized. Thus, it is possible for the translation of the sample 170 to be stopped in the middle of the sample 170, with the area in the middle being irradiated and then crystallized. Thereafter, the sample 170 can be translated so that another section of the semiconductor thin film 175 is arranged in the path of the beam pulse 164, such that the translation of the sample is then stopped again and the particular section is irradiated and completely melted in accordance with the exemplary embodiment of the process described in great detail above, as well as the embodiments of the process which shall be described below.

According to the present invention, any mask described and shown herein and those described and illustrated in U.S. patent application serial no. 09/390,535, the entire disclosure of which is incorporated herein by reference, may be used for the process and system according to the present invention. For example, instead of using the mask shown in Fig. 3 which allows the semiconductor thin film

175 to be flood-irradiated, a second exemplary embodiment of the mask 150' illustrated in Fig. 5A can be utilized. In contrast to the mask 150 of Fig. 3 which has a single open or transparent region 157, the mask 150' has multiple open or transparent regions 450 which are separated from one another by beam-blocking regions 455. The open or transparent regions 450 of the mask 150' can also be referred to as "slits." These slits permit small beam pulses (or beamlets) to irradiate there-through and completely melt the areas of the semiconductor thin film 175 that they impinge. An enlarged illustration of one of the slits 450 is provided in Fig. 5B, which shows that the dimensions of the slits 450 can be 0.5 μm by 0.5 μm. It should be clearly understood that other dimensions of the slits are possible, and are within the scope of the present invention. For example, the slits can have a rectangular shape, a circular shape, a triangular shape, a chevron shape, a diamond-shaped shape, etc. According to the present invention, the slits should be sufficiently large so that when the pulsed beamlets 164 formed thereby irradiate and crystallize the particular areas of the semiconductor thin film 175, the center portions (i.e., not the edge regions) are formed so as to situate the TFT devices (or at least their active regions) therein. It is important that the active regions of such situated TFT devices have respective distances from one another which are greater that the edge regions of the beamlet-irradiated and crystallized areas.

Figs. 6A-6D show an exemplary progression of a second embodiment of the process according to the present invention in which a plurality of successive areas along the first conceptual column 205 of the semiconductor thin film 175 is irradiated by the masked beam pulse 164 (comprised of beamlets) which is shaped by the mask 150' of Fig. 5A. The translation of the sample 170 with respect to the impingement thereof by the beam pulse 164 is substantially the same as the translation described above with reference to Figs. 4A-4F. The difference between the irradiation of the areas 310, 320, ..., 380, 390, 410, 420 by the beam pulse 164 shaped by the mask 150 of Fig. 3 and the areas 460, 470 by the beam pulse 164 shaped by the mask 150' is that substantially the entire areas 310, 320, ... , 380, 390, 410, 420 are irradiated and crystallized, as opposed to only certain small portions 462 of the areas 460, 470 are irradiated and crystallized.

Similarly to the area 310 in Fig. 4A, the portions 462 of the area 460 are irradiated as illustrated in Fig. 6A. Thereafter, the portions 462 are crystallized to form the center regions 465, and the edge regions 468 as shown in Fig. 4B. Similarly to the first center regions 315, the center regions 465 of the respective portions 462 have grains therein which are different than the grains of the edge regions 468, and are sized such that at least an active region of the TFT device (and possible the entire TFT device) can be placed away from the edge regions 468. As shown in Fig. 6C, upon the translation of the sample 170 in the –X direction, portions 472 of the area 470 are irradiated and then crystallized in a substantially the same manner as the portions 462. Therefore, the center regions 475 and the edge regions 478 of the area 470 are formed.

In addition, it is possible to utilize a third embodiment of a mask 150" according to the present invention as shown in Fig. 7 which has a long and narrow open or transparent region 490 so as to pattern and shape the beam 149 into the beam pulse 164. For example, the length of the region 490 can be 0.5 cm and the width thereof may be 0.1 mm. In this manner, each conceptual column of the sample 170 illustrated in Fig. 2 can be irradiated by the beam pulse 164 shaped by this mask 150". In addition, it may be possible for the length of the region 490 to be 30 cm. Thus, instead of subdividing the semiconductor thin film 175 into a number of conceptual columns, and irradiating each column separately, it is possible to irradiate and crystallize selected portions of the semiconductor thin film 175 by translating the sample 170 in the –Y direction from one edge of the sample 170 to the opposite edge thereof. It is important that the center regions be formed using such processing technique such that it would be possible to keep the active regions of the respective TFT devices at a distance from the edge regions.

Fig. 8A shows an illustration of the first and second irradiated and crystallized areas 510 and 520 possibly corresponding to the first and second areas 310, 320 of Figs. 4D and/or the adjacent portions 462 of the area 460 of Fig. 6D. In particular, Fig. 8A shows that the entire TFT devices 610 and 620 can be situated away from the edge regions 518, 528, 650, and possibly within the respective center regions 515, 525 of the areas 510, 520. The first TFT device 610 situated in the

center region 515 of the area 510 includes a gate 612, a drain 614, a source 616 and an active region 618, all of which are situated away from the edge region 518. Similarly, for the second TFT device 610, its gate 622, drain 624, source 626, and especially active region 628 are also situated away from the edge regions 528, 650 such that they do not overlap the respective edge region 528 of the area 520, and the edge region 650 which is provided between the center regions 515, 525.

Fig. 8B shows an illustration of the first and second irradiated and crystallized areas 510 and 520 also possibly corresponding to the adjacent portions 462 of the area 460 of Fig. 6D with the respective TFT devices 610, 620' provided thereon. In this exemplary embodiment, only respective active regions 618', 628' of the areas 510, 520 are provided away from the edge regions 518, 528, 650, and are provided within the respective uniform center regions 515, 525 of the areas 510, 520, while other portions of the TFT devices 610', 620' are situated on the respective edge regions 518, 528 of the areas 510, 520, and the edge area provided there between. In particular, the first TFT device 610' includes an active region 618' which entirely situated in the center region 515 of the area 510, while a gate 612', a drain 614' and a source 616' of the TFT device 610' overlap the edge region 518. Similarly, for the second TFT device 610', an active region 628' thereof is entirely situated within the respective center region 525 of the area 520, while a gate 622', a drain 624' and a source 626 of the second TFT device 620' are provided directly on the respective edge regions 528 of the area 520. Also, the gate 622' is provided on a border region 500 (i.e., the edge region 650 between the areas 510, 520) between the center region 515 of the area 510 and the center region 525 of the area 520. It should be understood that any one of the gate 612, 612', 622, 622' drain 614, 614', 624, 624' and source 616, 616', 626, 626' can be provided on the edge regions 518, 528 and the border region 500.

By using this exemplary embodiment of the present invention, the edge region 500 and/or the width of the edge regions 518, 528 associated with such edge region 500 can be reduced to 1 µm, which is approximately 100 to 10,000 smaller than the edge regions obtained using the conventional systems and process. Therefore, it would be possible to achieve the placement of the entire TFT device 610, 620 in the

center regions 515, 525 such that the distance between which would be greater that the edge region 500, as illustrated in Fig. 8A. Similar applies for the placement of the TFT devices 610', 620' as shown in Fig. 8B, except that the distance between the active regions 618', 628' of the respective TFT devices 610', 620' would be greater than the width of the edge region 500.

Fig. 9 is a flow diagram representing a first exemplary processing procedure of the present invention under at least a partial control of a computing arrangement of Fig. 1A using the techniques of the present invention of Figs. 4A-4F and 6A-6D. In step 1000, the hardware components of the system of Fig. 1A, such as the beam source 110, the energy beam modulator 120, and the beam attenuator and shutter 130 are first initialized at least in part by the computing arrangement 100. The sample 170 is loaded onto the sample translation stage 1800 in step 1005. It should be noted that such loading may be performed either manually or automatically using known sample loading apparatus under the control of the computing arrangement 100. Next, the sample translation stage 180 is moved, preferably under the control of the computing arrangement 100, to an initial position in step 1010. Various other optical components of the system are adjusted and/or aligned either manually or under the control of the computing arrangement 100 for a proper focus and alignment in step 1015, if necessary. In step 1020, the irradiation/laser beam 111 is stabilized at a predetermined pulse energy level, pulse duration and repetition rate. In step 1024, it is preferably determined whether each beam pulse has sufficient energy to irradiate the portions of the semiconductor thin film so as to crystallize such portions thereafter. If that is not the case, the attenuation of the beam 111 is adjusted by the beams source 110 under the control of the computing arrangement 100 in step 1025, and step 1024 is executed again to determine if the there is sufficient energy to crystallize the portions of the semiconductor thin film.

In step 1027, the sample is positioned to point the beam pulse 164 to impinge the first column of the semiconductor thin film. Then, in step 1030, the portions of the semiconductor thin film are irradiated using a masked intensity pattern (e.g., the masked beam pulse 164). Thereafter, the irradiated portions of the semiconductor thin film are crystallized with the minimized edge regions therein so as

to allow at least the active regions of the TFT devices to be placed away from such edge regions. In step 1035, it is determined whether the irradiation for the current column by the beam pulse has been completed. If no, in step 1040, the sample is continued to be irradiated with the next beam pulse 164. However, if in step 1035, it is determined that the irradiation and crystallization of the current column is completed, then it is determined in step 1040 whether there are any further columns of the sample to be processed. If so, the process continues to step 1050 in which the sample is translated to that the beam pulse is pointed to the next column to be processed according to the present invention. Otherwise, in step 1055, the exemplary processing has been completed for the sample 170, and the hardware components and the beam 111 of the system shown in Fig. 1A can be shut off, along with the process terminating.

Fig. 10 is a flow diagram representing a second exemplary processing procedure of the present invention under at least a partial control of a computing arrangement of Fig. 1A using the techniques of the present invention of Figs. 4A-4F and 6A-6D, in which is preferable to mask the beam 111. Steps 1100-1120 of this exemplary procedure are substantially the same as the steps 1000-1020 of the procedure of Fig. 9 and thus shall not be described herein in further detail. In step 1024, however, it is determined whether each pulse has enough energy to irradiate at least portions of the semiconductor thin film 175 such that the irradiated portion crystallize. If not, in step 1125, the attenuation for the beam pulse is adjusted, and the energy fluence is verified again. Upon the verification of the energy fluence of the beam pulse, the sample is moved to impinge a first column of the sample 170.

Then, in step 1130, the resultant beam 149 is passed through a mask 159 to shape the beam pulse, and shape the edge portions of the resultant pulse. Then, the sample 170 is continuously translated along the current column in step 1135, In step 1140, during the translation of the sample 170, the portions of the semiconductor thin film are irradiated and at least partially melted using a masked intensity pattern beam pulse to allow the irradiated portions to crystallize. This irradiation of these portion of the semiconductor thin film 175 can be performed when the beam pulses reach particular locations on the sample, which are pre-assigned by the computing

arrangement 100. Thus, the beam source can be fired upon the sample reaching these locations with respect to the beam pulses. Thereafter, the irradiated portions of the semiconductor thin film are allowed to crystallize such that the certain areas of the solidified portions have been nucleated and include uniform material therein so as to allow the distance between at least the active regions of the TFT devices to be greater that the edge regions of such irradiated areas. Such processing is continued until the end of the current column on the semiconductor thin film 17 5 is reached. In step 1145, it is determined whether there are any further columns of the sample to be processed. If so, the process continues to step 1150 in which the sample is translated to that the beam pulse is pointed to the next column to be processed according to the present invention. Otherwise, in step 1155 is performed, which is substantially the same as that of step 1055 of Fig. 9.

The foregoing merely illustrates the principles of the invention. Various modifications and alterations to the described embodiments will be apparent to those skilled in the art in view of the teachings herein. For example, while the above embodiment has been described with respect to irradiation and crystallization of the semiconductor thin film, it may apply to other materials processing techniques, such as micro-machining, photo-ablation, and micro-patterning techniques, including those described in International patent application no. PCT/US01/12799 and U.S. patent application serial nos. 09/390,535, 09/390,537 and 09/526,585, the entire disclosures of which are incorporated herein by reference. The various mask patterns and intensity beam patterns described in the above-referenced patent application can also be utilized with the process and system of the present invention. It will thus be appreciated that those skilled in the art will be able to devise numerous systems and methods which, although not explicitly shown or described herein, embody the principles of the invention and are thus within the spirit and scope of the present invention.

What Is Claimed Is:

1. A method for processing a thin film sample, comprising the steps of:

(a) controlling a beam generator to emit at least one beam pulse;

(b) masking the at least one beam pulse to produce at least one masked beam pulse, wherein the at least one masked beam pulse is used to irradiate at least one portion of the thin film sample;

(c) with the at least one masked beam pulse, irradiating the at least one portion of the film sample with sufficient intensity for the at least one portion to later crystallize; and

(d) allowing the at least one portion of the film sample to crystallize, the crystallized at least one portion being composed of a first area and a second area, wherein, upon the crystallization thereof, the first area includes a first set of grains, and the second area includes a second set of grains whose at least one characteristic is different from at least one characteristic of the second set of grains,

wherein the first area surrounds the second area, and is configured to allow an active region of an electronic device to be provided at a distance therefrom.

2. The method according to claim 1, wherein the masked beam pulse has the intensity to completely melt the at least one portion of the thin film sample throughout its thickness.

3. The method according to claim 1, wherein the masked beam pulse has the intensity to partially melt the at least one portion of the thin film sample.

4. The method according to claim 1, wherein the active region of the TFT is situated within the second area.

5. The method according to claim 1, wherein the second area corresponds to at least one pixel.

6. The method according to claim 1, wherein the second area has a cross-section for facilitating thereon all portions of the TFT.

7. The method according to claim 1, wherein a size and a position of the first area with respect to the second area are provided such that the first area provides either no effect or a negligible effect on a performance of the TFT.

8. The method according to claim 1, further comprising the step of:

(e) after step (d), determining a location of the first area so as to avoid a placement of the active region of the TFT thereon.

9. The method according to claim 1, wherein the at least one beam pulse includes a plurality of beamlets, and wherein the first and second areas are irradiated by the beamlets.

10. The method according to claim 1, wherein the thin film sample is a silicon thin film sample.

11. The method according to claim 1, wherein the thin film sample is composed of at least one of silicon and germanium.

12. The method according to claim 1, wherein the thin film sample has a thickness approximately between 100Å and 10,000Å.

13. The method according to claim 1, wherein the first set of grains provided in the first area are laterally-grown grains.

14. The method according to claim 13, wherein the laterally-grown grains of the first area are equiaxed grains.

15. The method according to claim 1, wherein the electronic device is a thin-film transistor ("TFT").

16. The method according to claim 1, wherein the thin film sample is a semiconductor thin film sample.

17. A system for processing a thin film sample, comprising:

a processing arrangement which is configured to:

(a) control a beam generator to emit at least one beam pulse;

(b) mask the at least one beam pulse to produce at least one masked beam pulse, wherein the at least one masked beam pulse is used to irradiate at least one portion of the film sample; and

(c) with the at least one masked beam pulse, initiate an irradiation of the at least one portion of the film sample with sufficient intensity for the at least one portion to later crystallize

wherein the at least one portion of the film sample is allowed to crystallize, the crystallized at least one portion being composed of a first area and a second area, wherein, upon the crystallization thereof, the first area includes a first set of grains, and the second area includes a second set of grains whose at least one characteristic is different from at least one characteristic of the second set of grains,

wherein the first area surrounds the second area, and configured to allow an active region of an electronic device to be provided at a distance therefrom.

18. The system according to claim 17, wherein the masked beam pulse has the intensity to completely melt the at least one portion of the thin film sample throughout its thickness.

19. The system according to claim 18, wherein the masked beam pulse has the intensity to partially melt the at least one portion of the thin film sample.

20. The system according to claim 17, wherein the active region of the TFT is situated within the second area.

21. The system according to claim 17, wherein the second area corresponds to at least one pixel.

22. The system according to claim 17, wherein the second area has a cross-section for facilitating thereon all portions of the TFT.

23. The system according to claim 17, wherein a size and a position of the first area with respect to the second area are provided such that the first area provides either no effect or a negligible effect on a performance of the TFT.

24. The system according to claim 17, wherein the processing arrangement is further configured to, after procedure (d), determine a location of the first area so as to avoid a placement of the active region of the TFT thereon.

25. The system according to claim 17, wherein the at least one beam pulse includes a plurality of beamlets, and wherein the first and second areas are irradiated by the beamlets.

26. The system according to claim 17, wherein the thin film sample is a silicon the film sample.

27. The system according to claim 17, wherein the thin film sample is composed of at least one of silicon and germanium.

28. The system according to claim 17, wherein the thin film sample has a thickness approximately between 100Å and 10,000Å.

29. The system according to claim 17, wherein the first set of grains provided in the first area are laterally-grown grains.

30. The system according to claim 29, wherein the laterally-grown grains of the first area are equiaxed grains.

31. The system according to claim 17, wherein the electronic device is a thin-film transistor ("TFT").

32. The system according to claim 17, wherein the thin film sample is a semiconductor thin film sample.

33. A thin film sample, comprising:

at least one section irradiated by at least one masked beam pulse which is configured to irradiate the at least one section of the sample for a later crystallization thereof,

wherein the at least one portion of the film sample is crystallized to include a first area and a second area,

wherein, upon the crystallization thereof, the first area includes a first set of grains, and the second area includes a second set of grains whose at least one characteristic is different from at least one characteristic of the second set of grains,

wherein the first area surrounds the second area, and is configured to allow an active region of an electronic device to be provided at a distance therefrom.

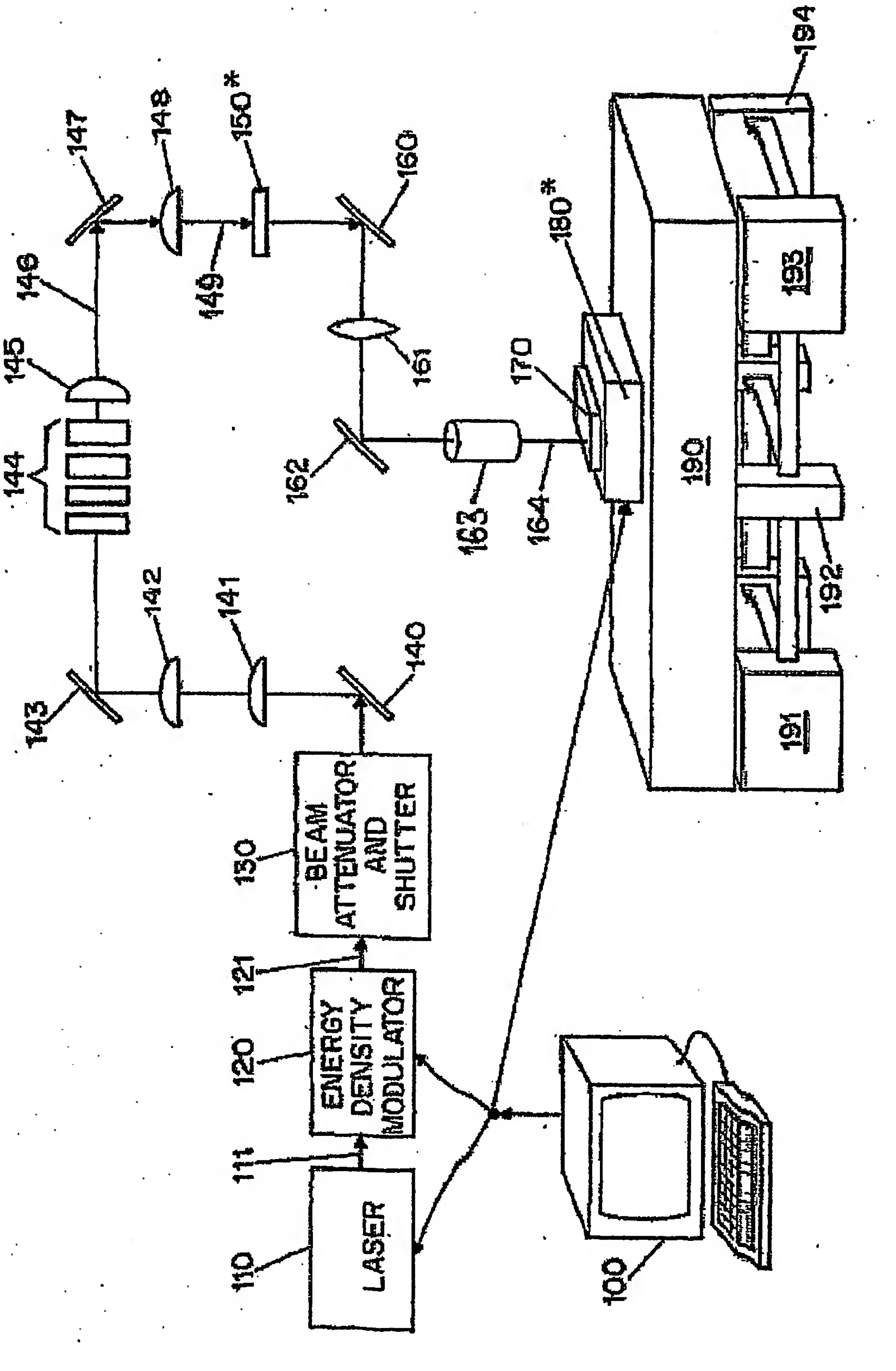

LASER
ENERGY DENSITY MODULATOR
BEAM ATTENUATOR AND SHUTTER
110
111
120
121
130
140
141
142
143
144
145
146
147
148
149
150*
160
161
162
163
164
170
180*
190
191
192
193
194
100

FIG. 1 A

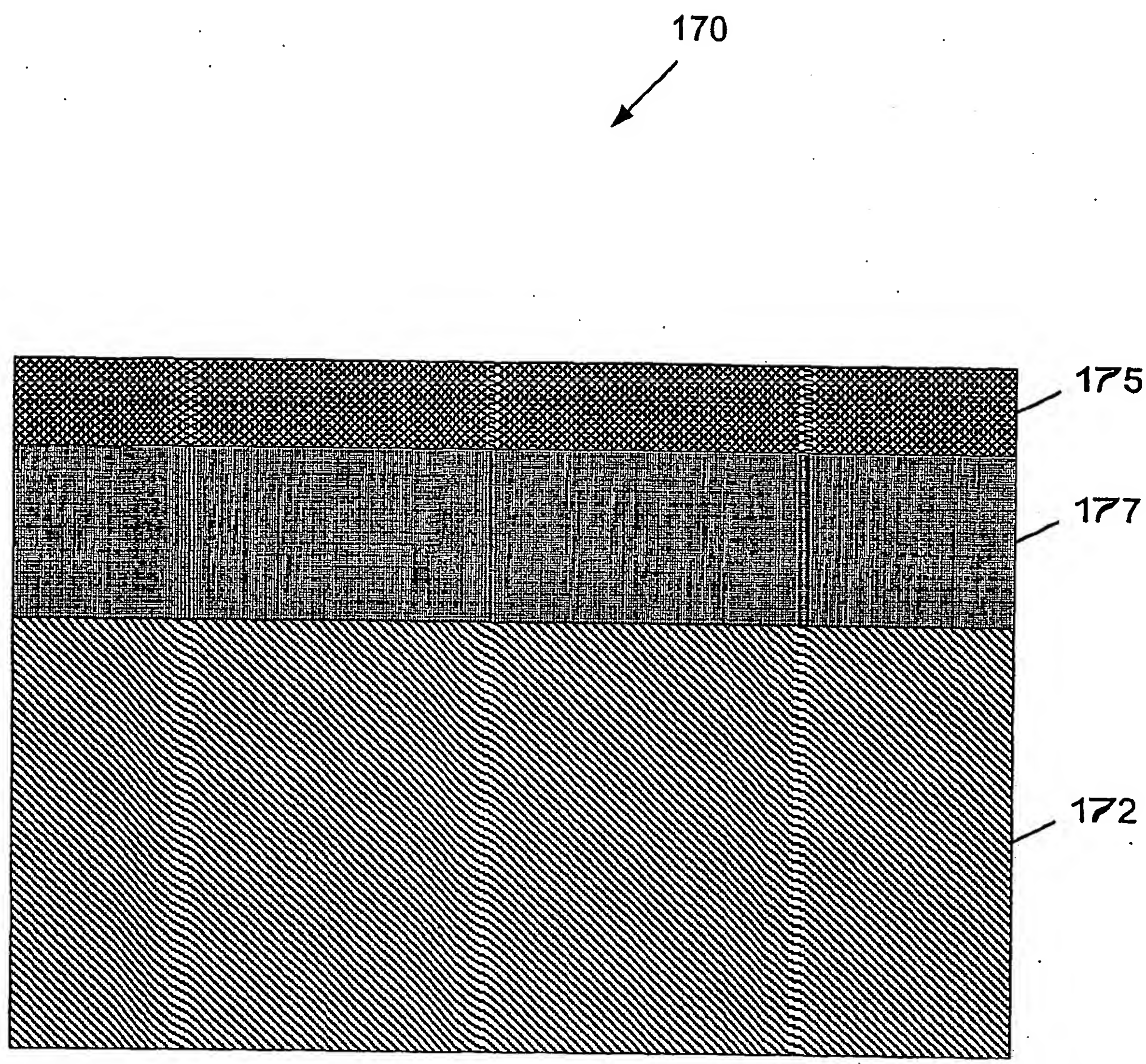


FIG. 1B

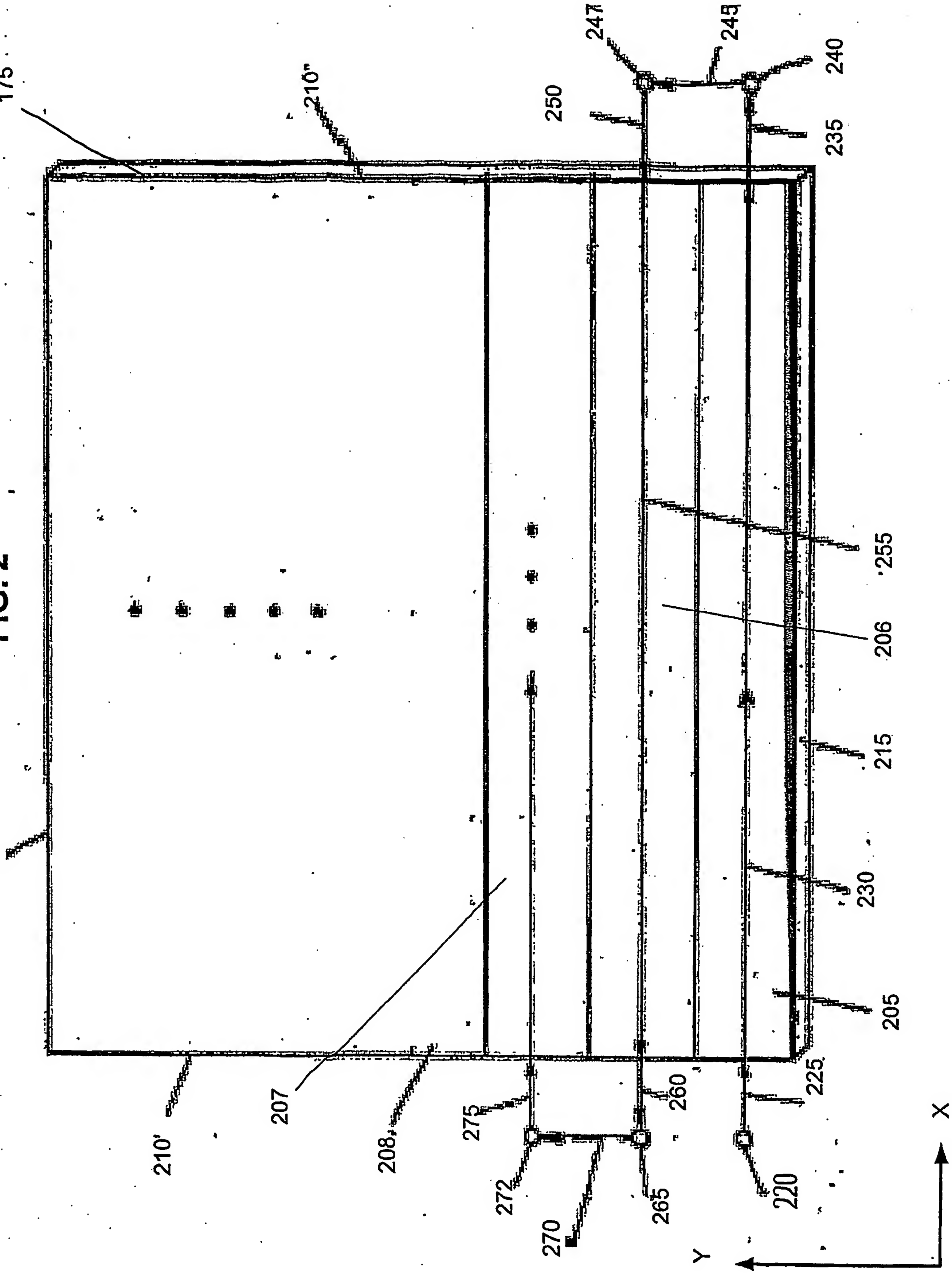

175
210"
250
247
245
240
235
255
206
215
230
205
225
260
220
265
270
272
275
208
207
210'
X
Y

FIG. 2

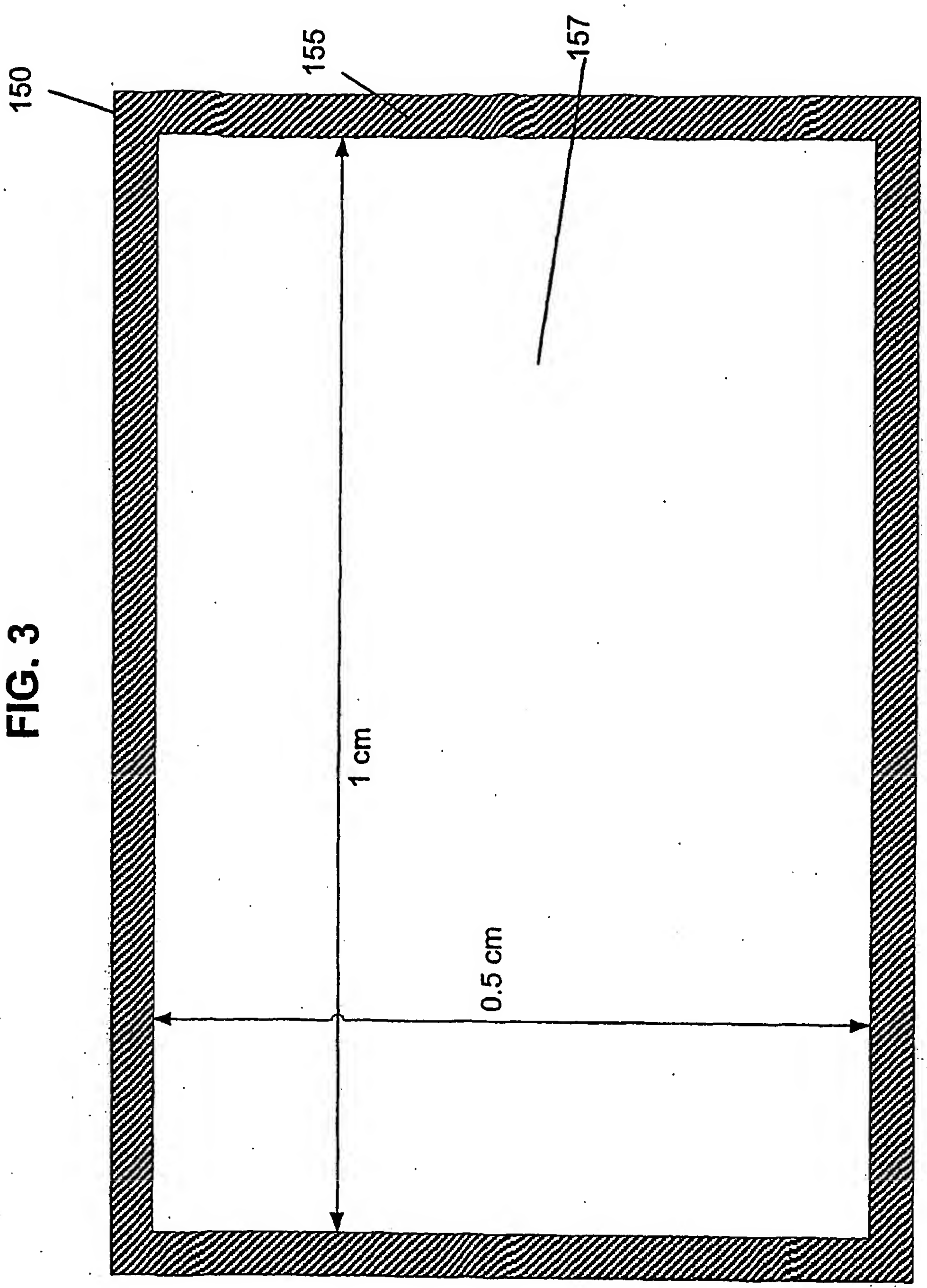


FIG. 3

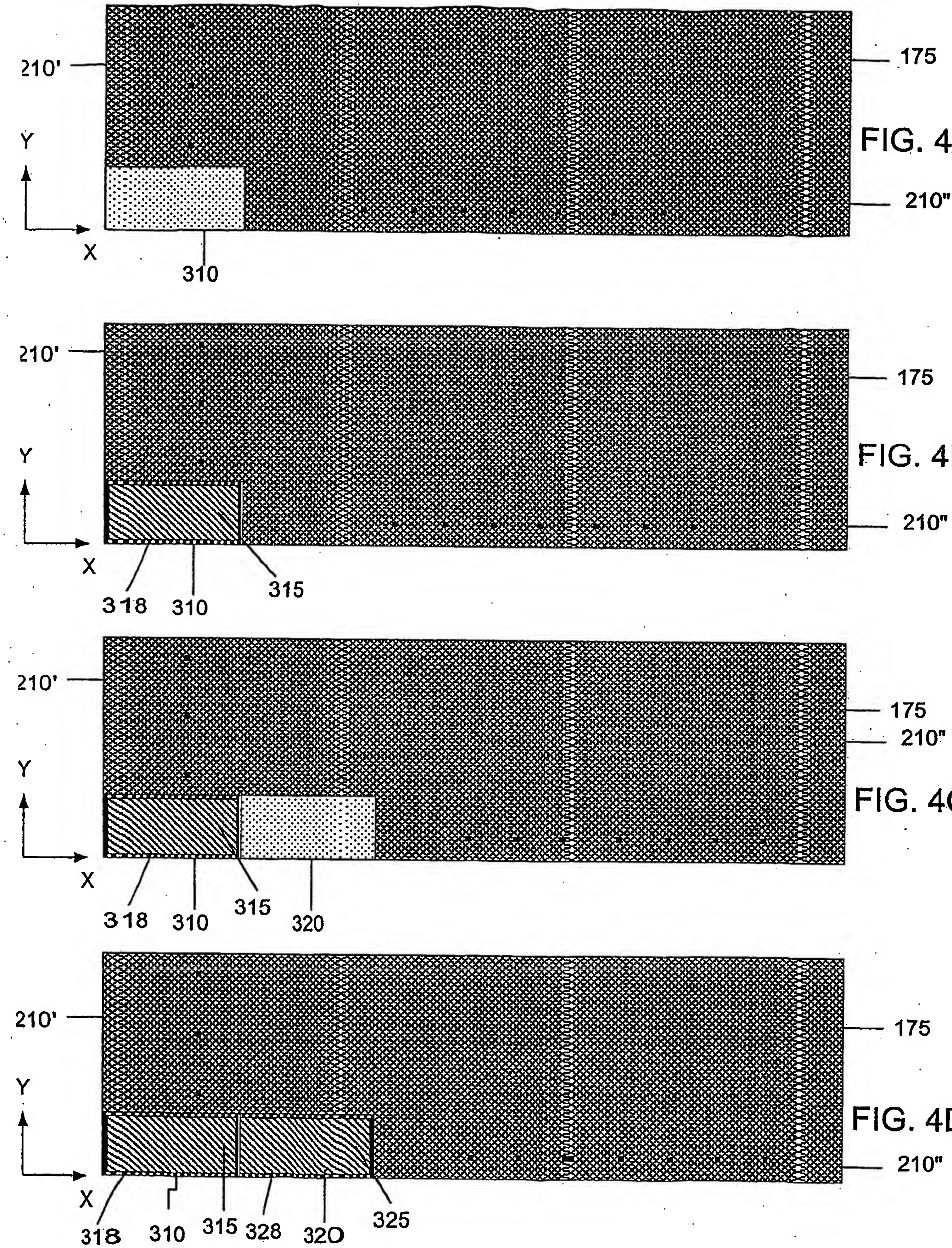


FIG. 4A

FIG. 4B

FIG. 4C

FIG. 4D

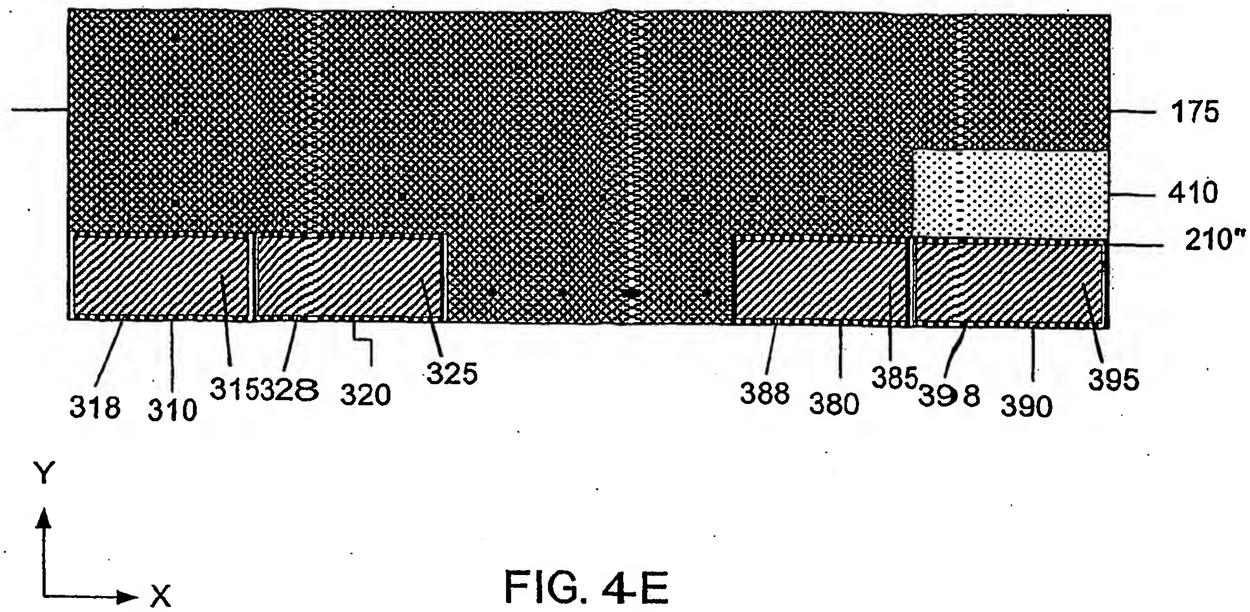

175
410
210"
318
310
315
328
320
325
388
380
385
398
390
395
Y
X

FIG. 4E

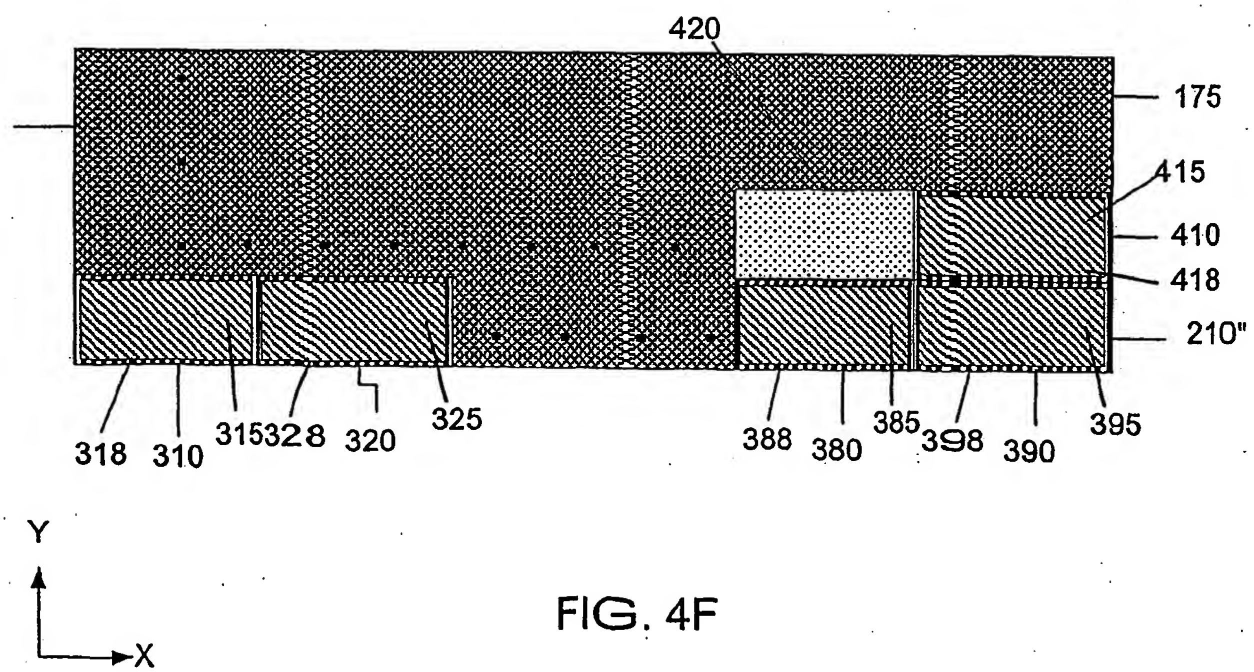
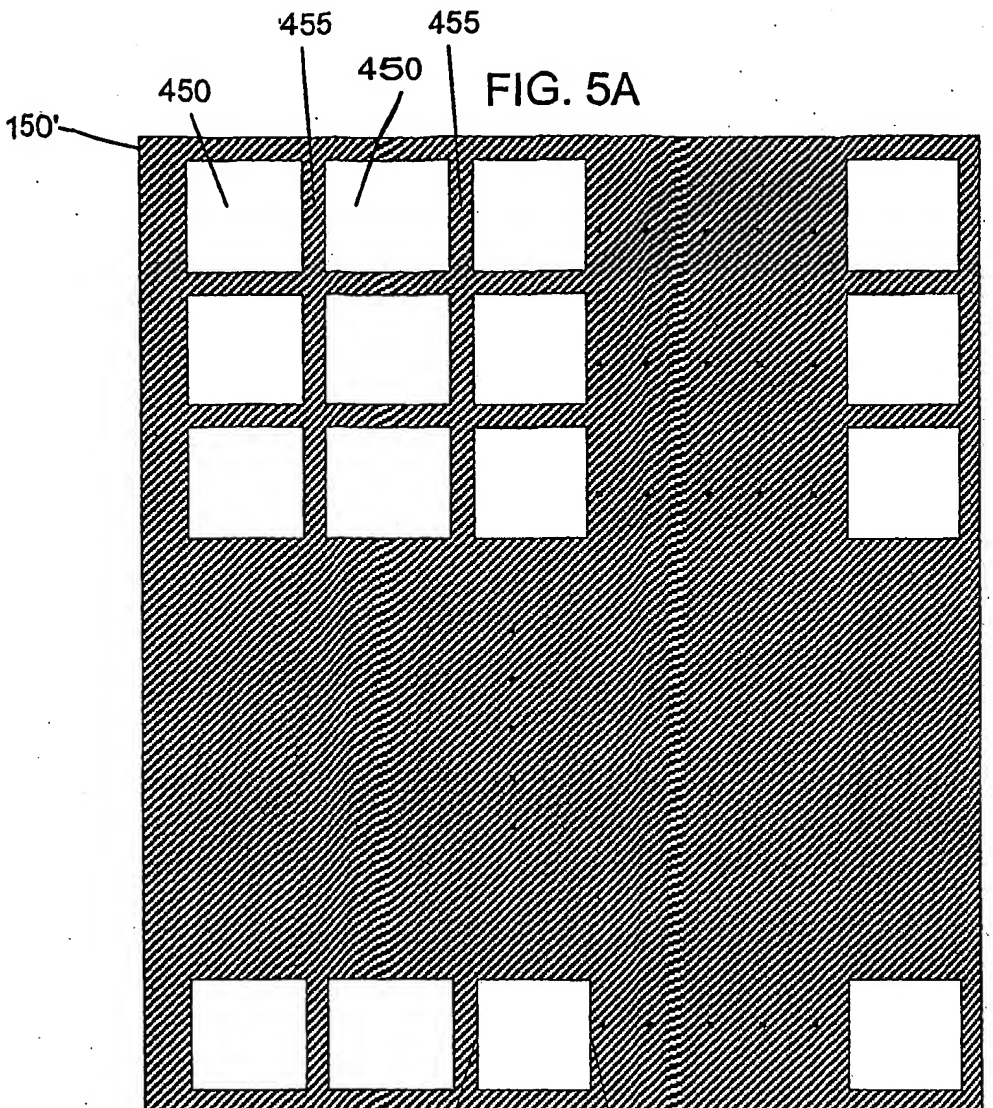

420
175
415
410
418
210"
318
310
315
328
320
325
388
380
385
398
390
395
Y
X

FIG. 4F

FIG. 5A



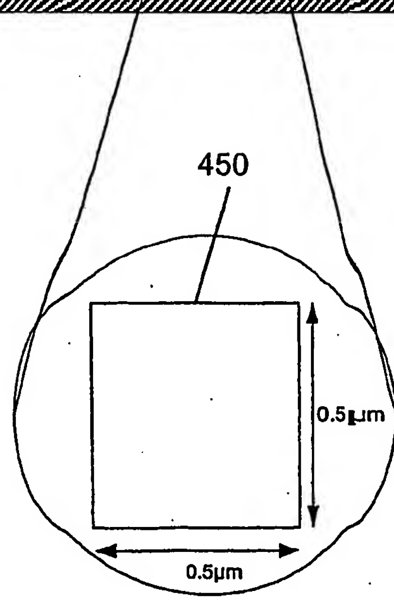


FIG. 5B

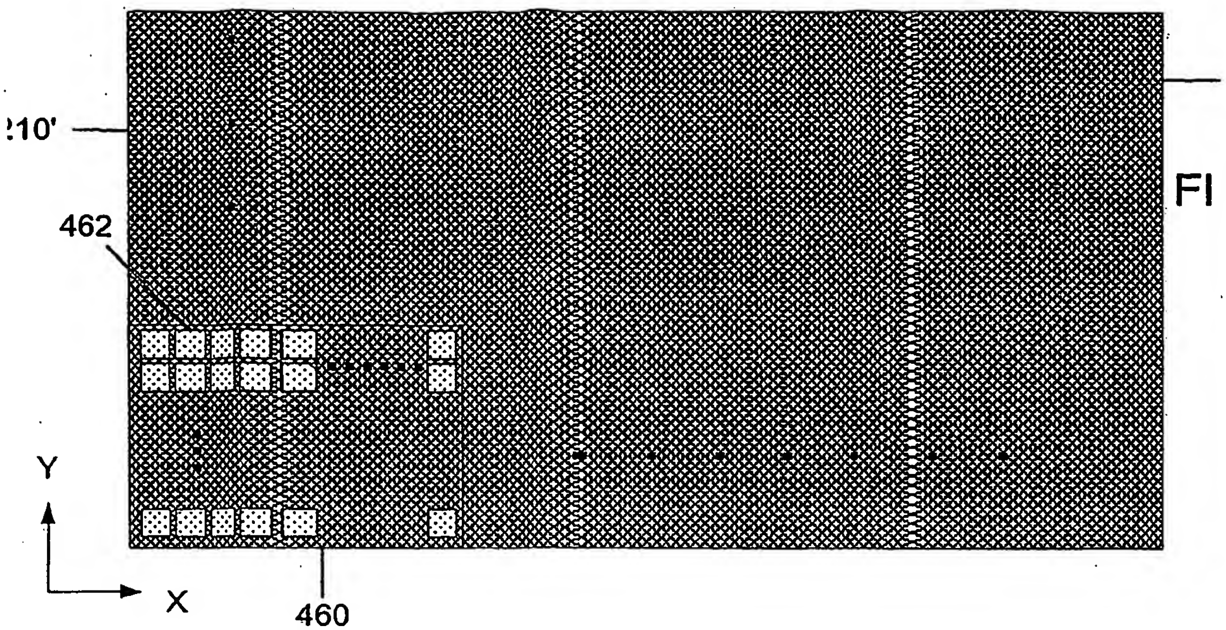


FIG. 6A

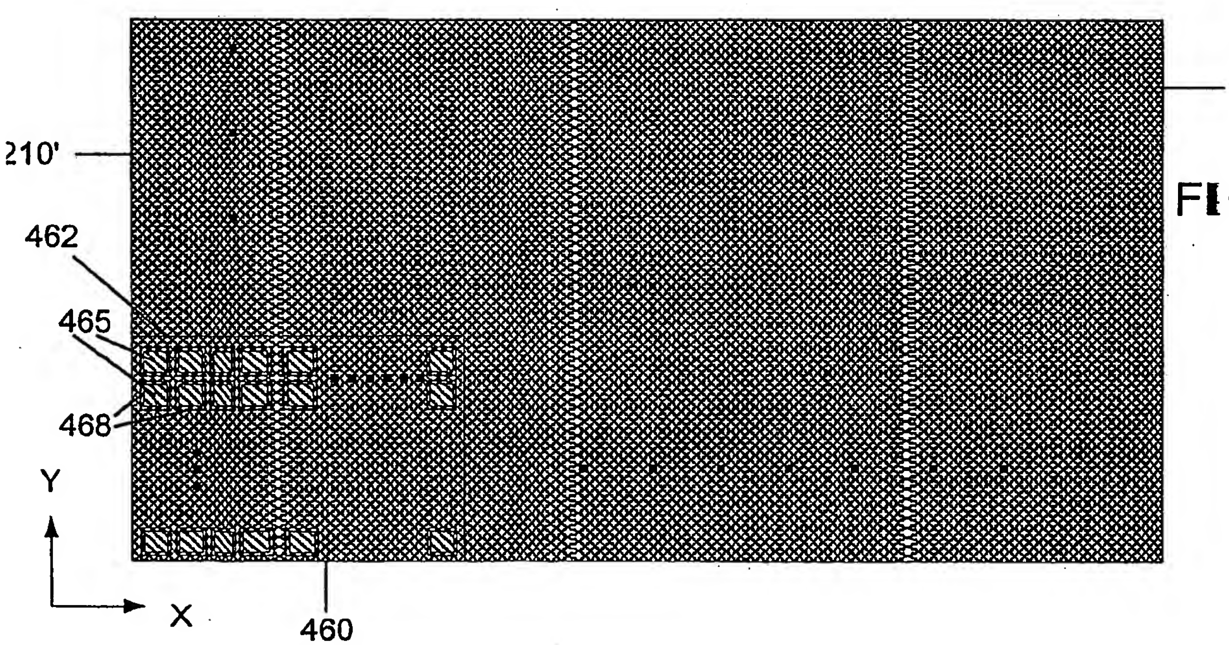


FIG. 6B

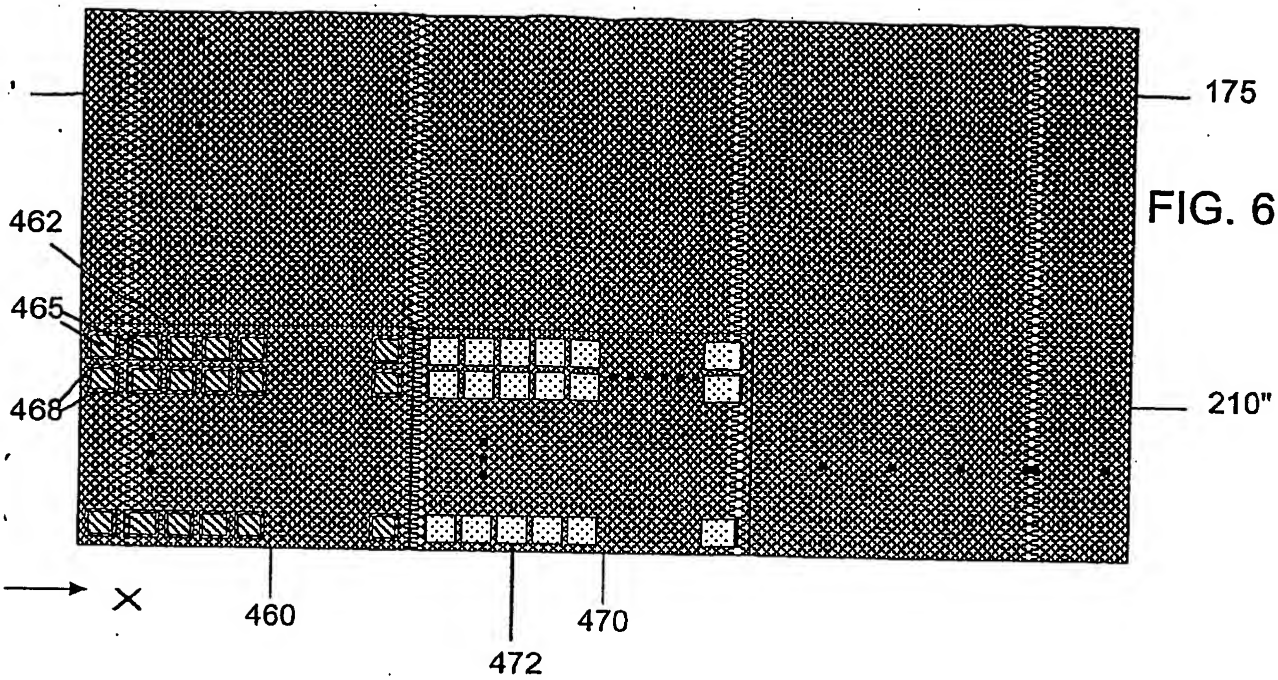

175
462
465
468
210"
X
460
472
470

FIG. 6C

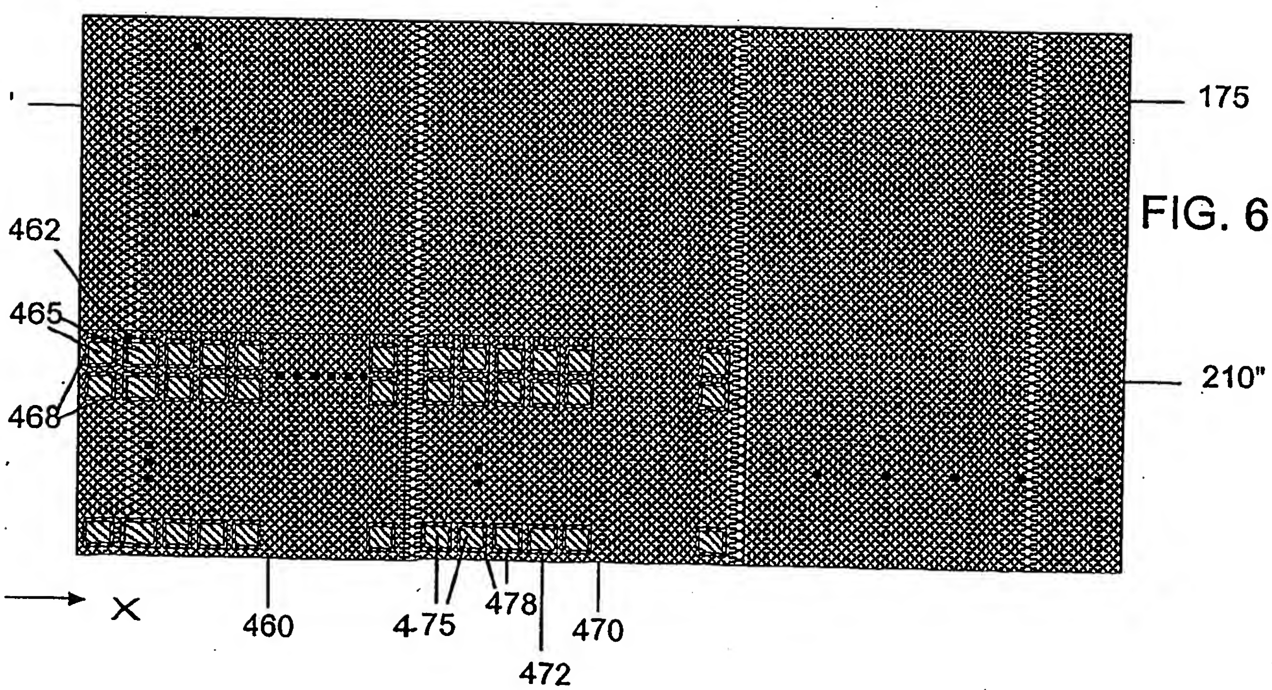

175
462
465
468
210"
X
460
475
478
472
470

FIG. 6D

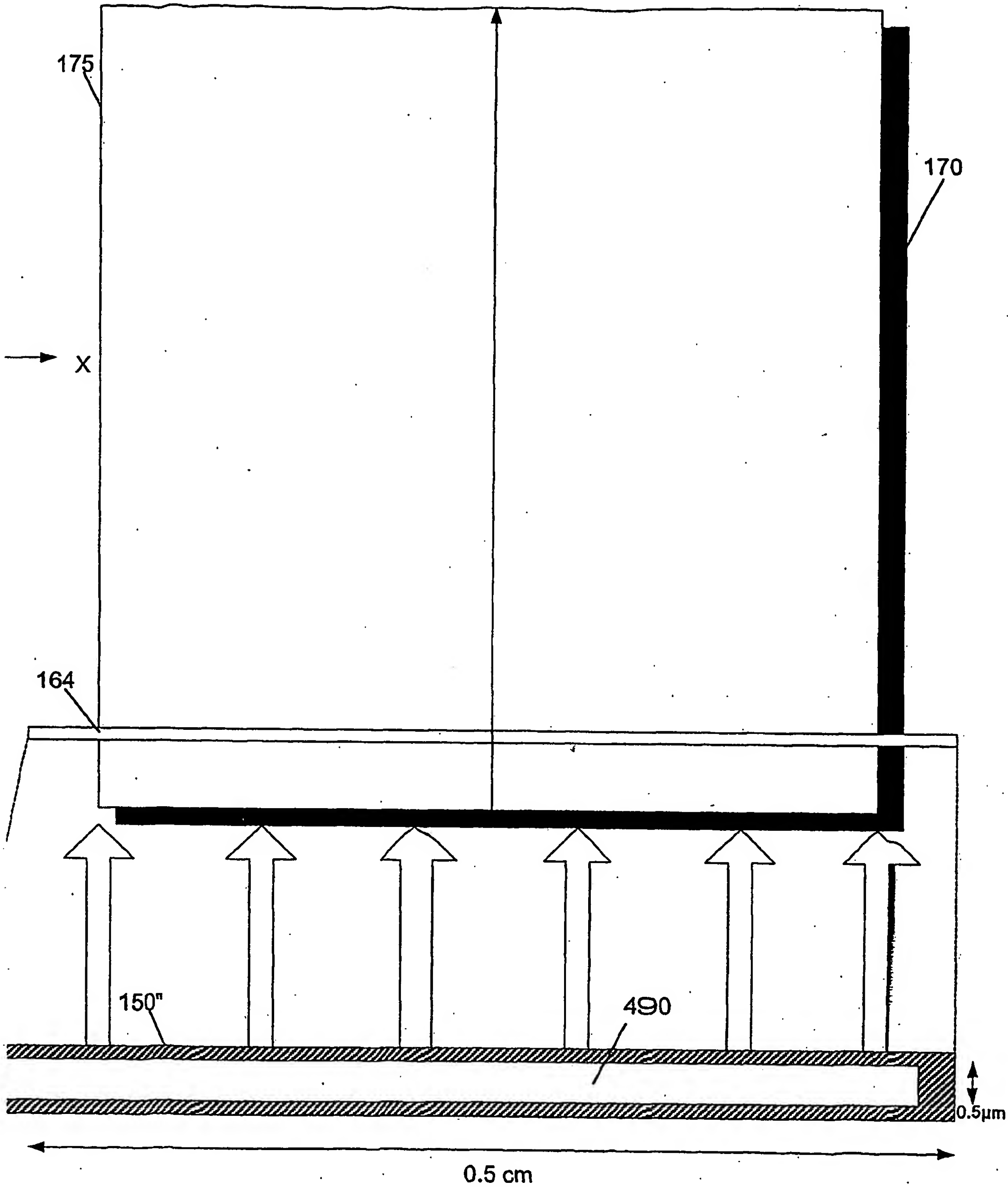


FIG. 7

FIG. 8A

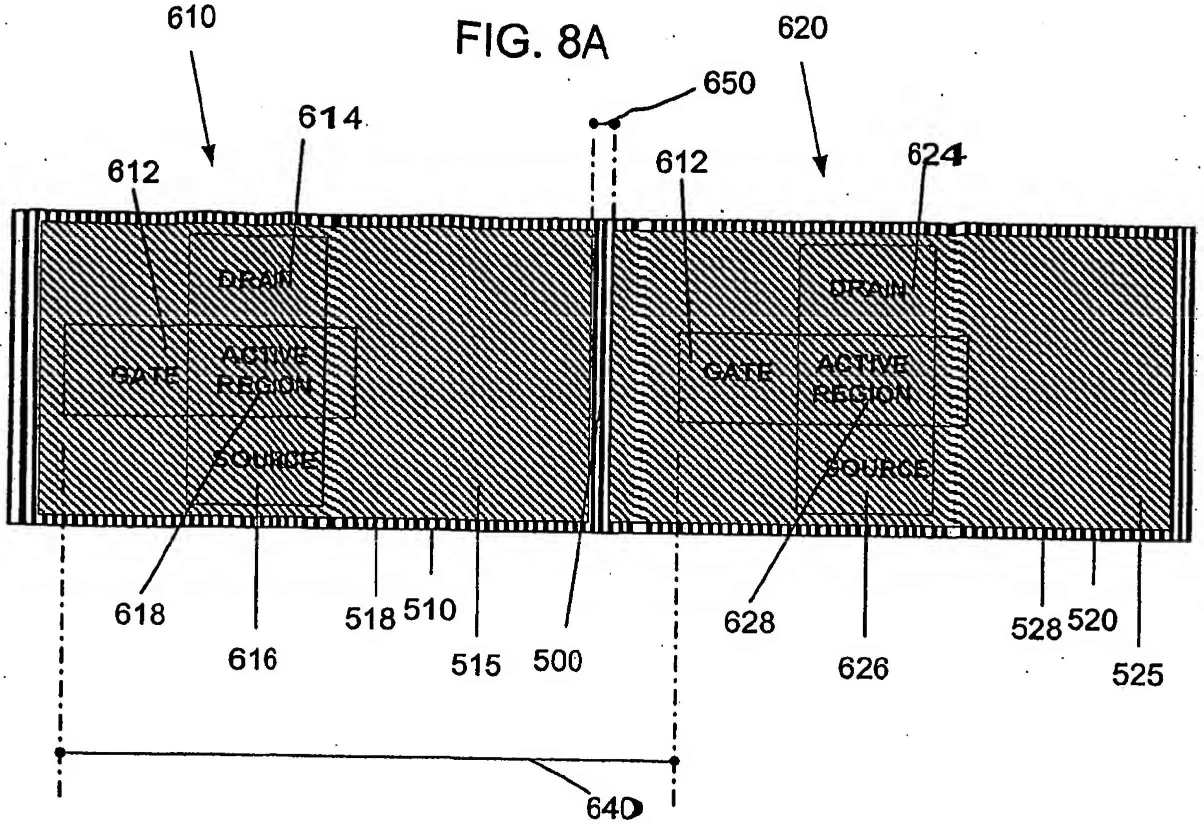

610
620
650
614
612
612
624
DRAIN
GATE
ACTIVE REGION
SOURCE
DRAIN
GATE
ACTIVE REGION
SOURCE
618
616
518
510
515
500
628
626
528
520
525
640

FIG. 8B

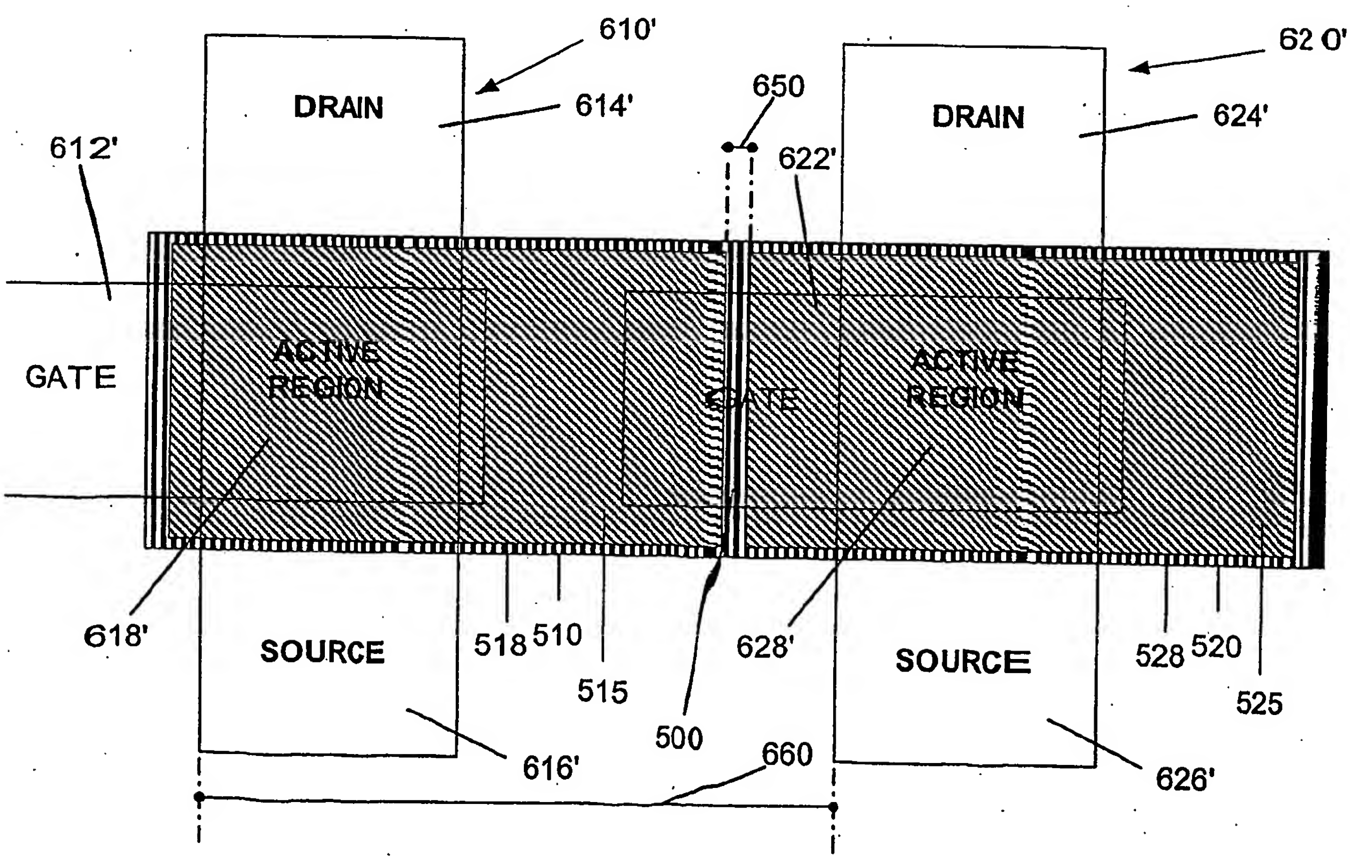

610'
62 0'
DRAIN
614'
650
DRAIN
624'
612'
622'
GATE
ACTIVE REGION
GATE
ACTIVE REGION
618'
SOURCE
518
510
515
500
628'
SOURCE
528
520
525
616'
660
626'

FIG. 9

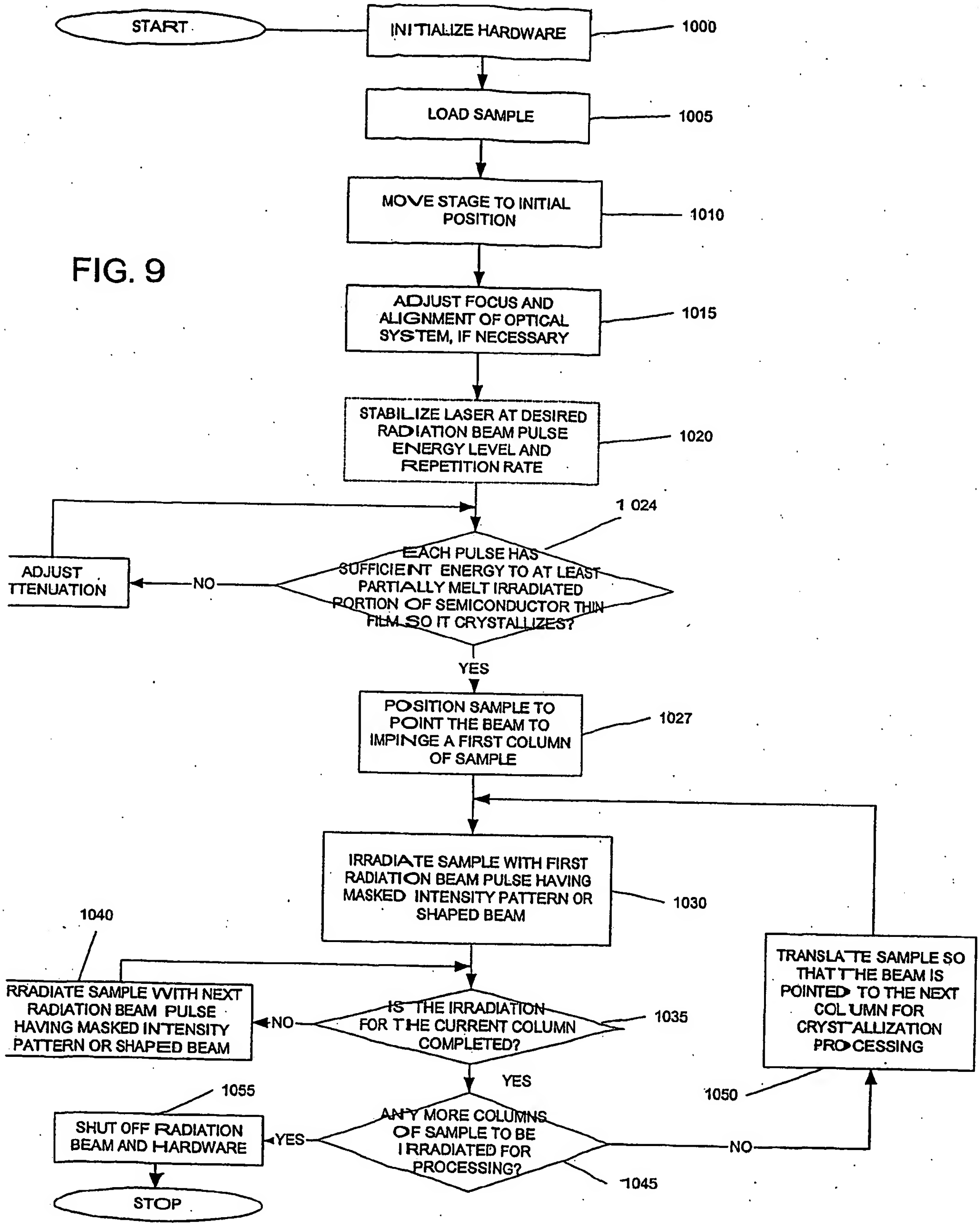
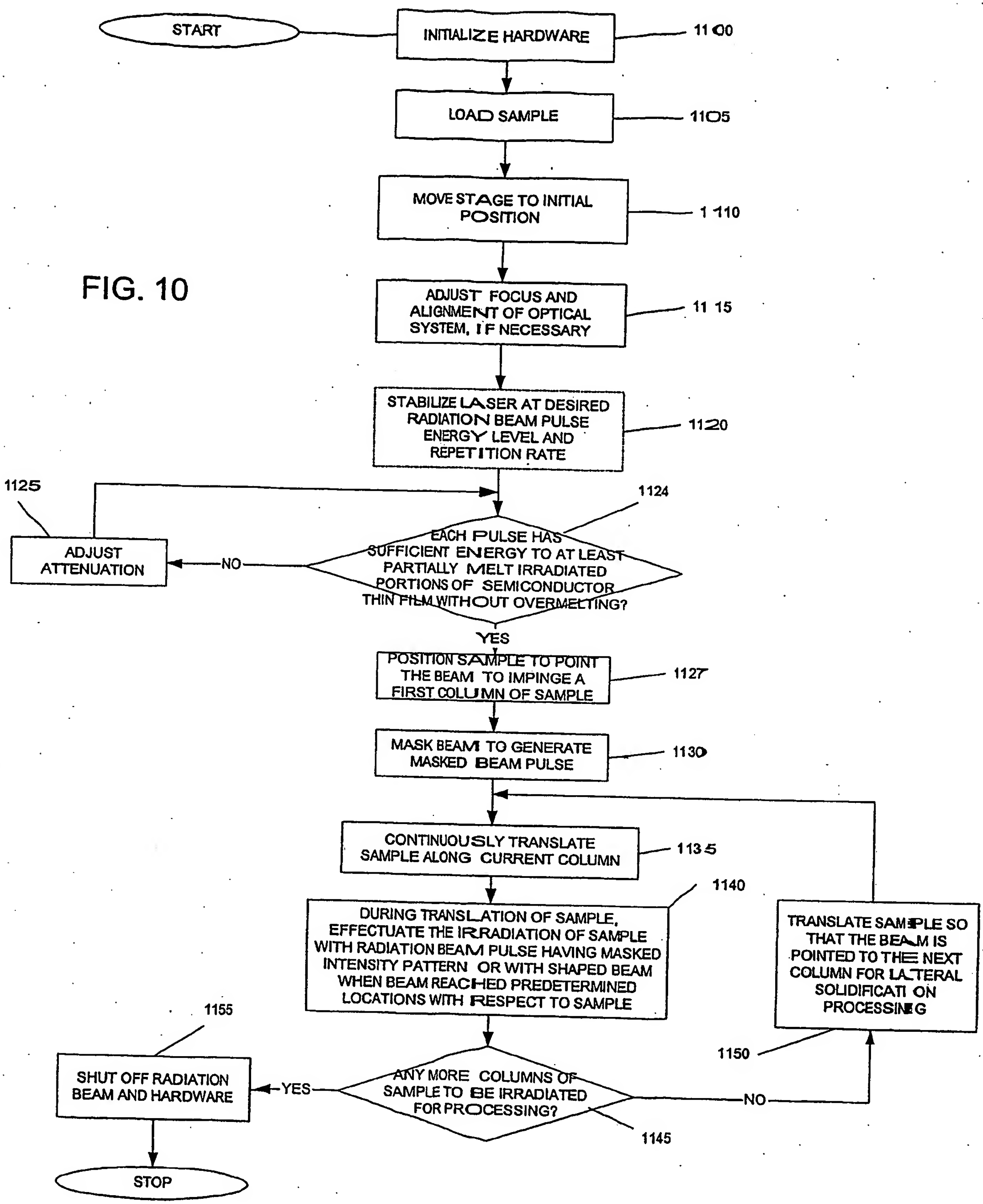

START
INITIALIZE HARDWARE
1000
LOAD SAMPLE
1005
MOVE STAGE TO INITIAL POSITION
1010
ADJUST FOCUS AND ALIGNMENT OF OPTICAL SYSTEM, IF NECESSARY
1015
STABILIZE LASER AT DESIRED RADIATION BEAM PULSE ENERGY LEVEL AND REPETITION RATE
1020
1024
EACH PULSE HAS SUFFICIENT ENERGY TO AT LEAST PARTIALLY MELT IRRADIATED PORTION OF SEMICONDUCTOR THIN FILM SO IT CRYSTALLIZES?
NO
ADJUST TTENUATION
YES
POSITION SAMPLE TO POINT THE BEAM TO IMPINGE A FIRST COLUMN OF SAMPLE
1027
IRRADIATE SAMPLE WITH FIRST RADIATION BEAM PULSE HAVING MASKED INTENSITY PATTERN OR SHAPED BEAM
1030
1040
RRADIATE SAMPLE WITH NEXT RADIATION BEAM PULSE HAVING MASKED INTENSITY PATTERN OR SHAPED BEAM
NO
IS THE IRRADIATION FOR THE CURRENT COLUMN COMPLETED?
1035
YES
TRANSLATE SAMPLE SO THAT THE BEAM IS POINTED TO THE NEXT COLUMN FOR CRYSTALLIZATION PROCESSING
1050
1055
SHUT OFF RADIATION BEAM AND HARDWARE
YES
ANY MORE COLUMNS OF SAMPLE TO BE IRRADIATED FOR PROCESSING?
NO
1045
STOP

FIG. 10


START
INITIALIZE HARDWARE
1100
LOAD SAMPLE
1105
MOVE STAGE TO INITIAL POSITION
1110
ADJUST FOCUS AND ALIGNMENT OF OPTICAL SYSTEM, IF NECESSARY
1115
STABILIZE LASER AT DESIRED RADIATION BEAM PULSE ENERGY LEVEL AND REPETITION RATE
1120
1125
ADJUST ATTENUATION
NO
1124
EACH PULSE HAS SUFFICIENT ENERGY TO AT LEAST PARTIALLY MELT IRRADIATED PORTIONS OF SEMICONDUCTOR THIN FILM WITHOUT OVERMELTING?
YES
POSITION SAMPLE TO POINT THE BEAM TO IMPINGE A FIRST COLUMN OF SAMPLE
1127
MASK BEAM TO GENERATE MASKED BEAM PULSE
1130
CONTINUOUSLY TRANSLATE SAMPLE ALONG CURRENT COLUMN
1135
1140
DURING TRANSLATION OF SAMPLE, EFFECTUATE THE IRRADIATION OF SAMPLE WITH RADIATION BEAM PULSE HAVING MASKED INTENSITY PATTERN OR WITH SHAPED BEAM WHEN BEAM REACHED PREDETERMINED LOCATIONS WITH RESPECT TO SAMPLE
TRANSLATE SAMPLE SO THAT THE BEAM IS POINTED TO THE NEXT COLUMN FOR LATERAL SOLIDIFICATION PROCESSING
1150
1155
SHUT OFF RADIATION BEAM AND HARDWARE
YES
ANY MORE COLUMNS OF SAMPLE TO BE IRRADIATED FOR PROCESSING?
NO
1145
STOP

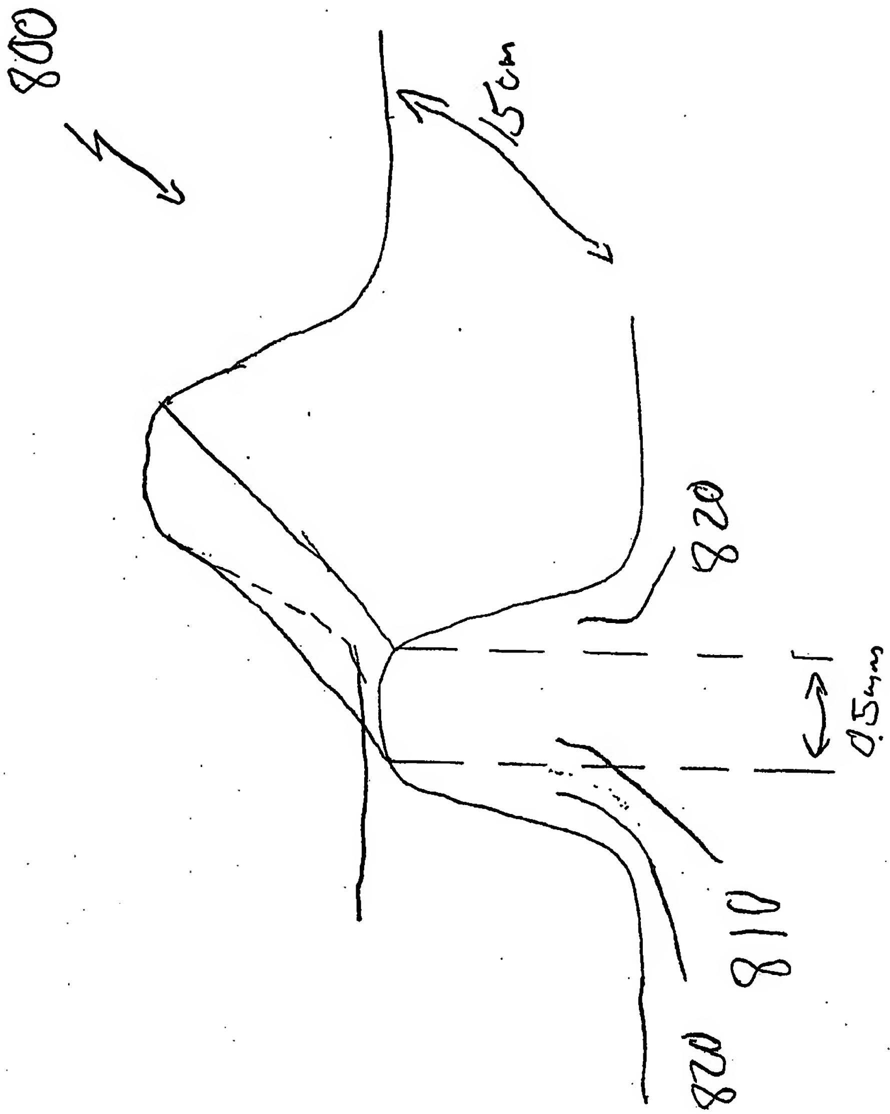


Fig. 11A
Prior Art

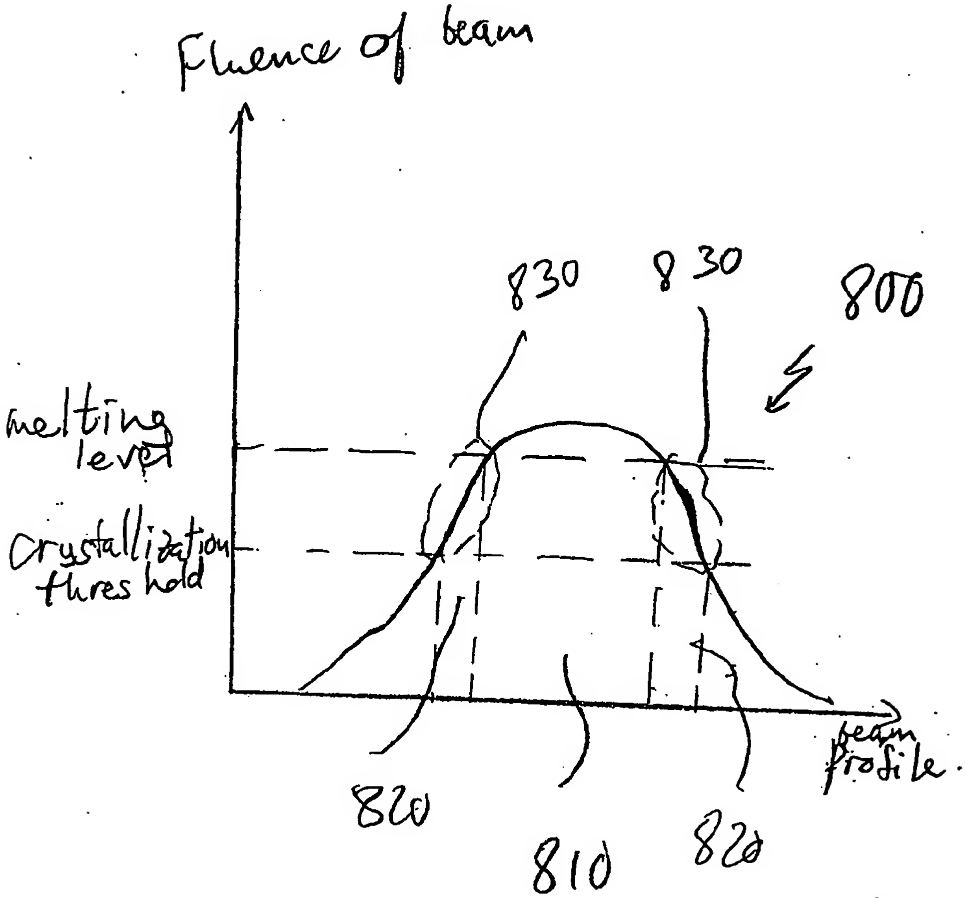


Fig. 11B Prior Art

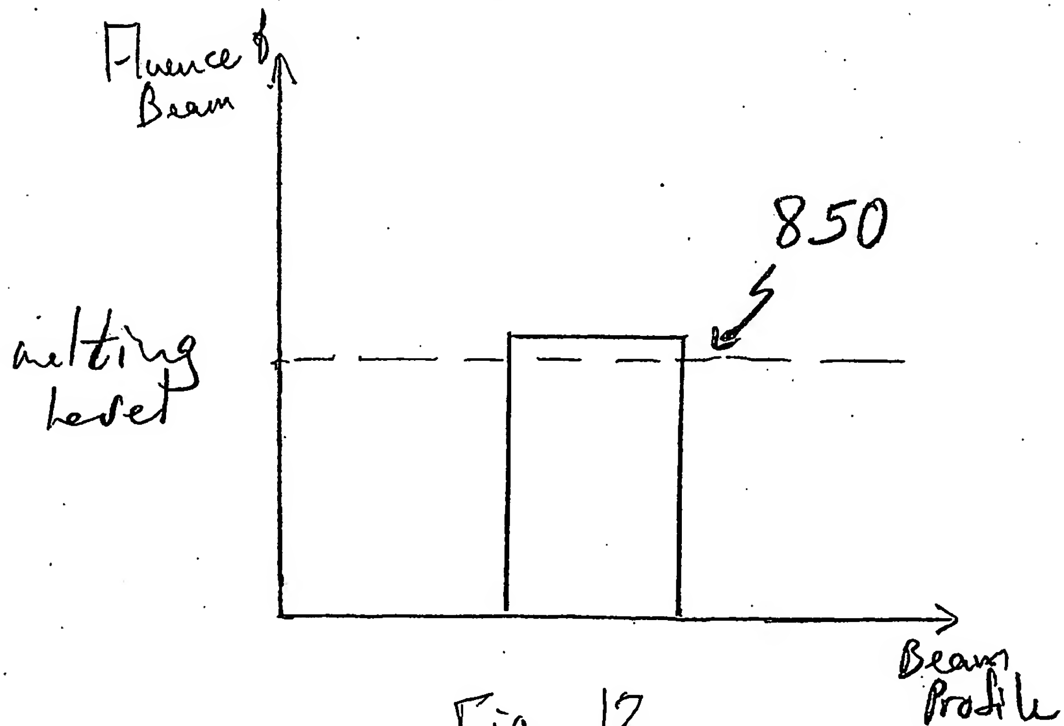


Fig. 12

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 February 2004 (26.02.2004)

PCT

(10) International Publication Number
WO 2004/017382 A2

(51) International Patent Classification[7]: H01L

(21) International Application Number: PCT/US2003/025972

(22) International Filing Date: 19 August 2003 (19.08.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/405,083 19 August 2002 (19.08.2002) US

(71) Applicant (*for all designated States except US*): THE TRUSTEES OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK [US/US]; 116th Street and Broadway, New York, NY 10027 (US).

(72) Inventor; and
(75) Inventor/Applicant (*for US only*): IM, James, S. [US/US]; 520 West 114th Street, Apt. 74, New York, NY 10025 (US).

(74) Agents: TANG, Henry et al.; Baker Botts L.L.P., 30 Rockefeller Plaza, New York, NY 10112-4498 (US).

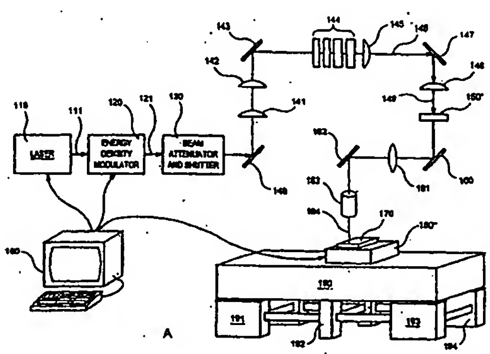
(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

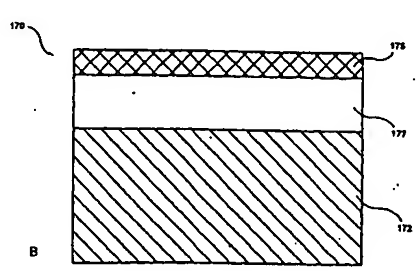
(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PROCESS AND SYSTEM FOR LASER CRYSTALLIZATION PROCESSING OF FILM REGIONS ON A SUBSTRATE TO PROVIDE SUBSTANTIAL UNIFORMITY WITHIN AREAS IN SUCH REGIONS AND EDGE AREAS THEREOF, AND A STRUCTURE OF SUCH FILM REGIONS





(57) Abstract: A process and system for processing a thin film sample, as well as the thin film structure are provided. In particular, a beam generator can be controlled to emit successive irradiation beam pulses at a predetermined repetition rate. Each irradiation beam pulse may be masked to define a first plurality of beamlets and a second plurality of beamlets. The first and second plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to at least partially melt irradiated portions of the section of the film sample. A particular portion of the section of the film sample is irradiated with the first beamlets of a first pulse of the irradiated beam pulses to melt first areas of the particular portion, the first areas being at least partially melted, leaving first unirradiated regions between respective adjacent ones of the first areas, and being allowed to resolidify and crystallize. After the irradiation of the particular portion with the first beamlets, the particular portion is again irradiated with the second beamlets of a second pulse of the irradiated beam pulses to melt second areas of the particular portion, the second areas being at least partially melted, leaving second unirradiated regions between respective adjacent ones of the second areas, and being allowed to resolidify and crystallize. The first irradiated and re-solidified areas and the second irradiated and re-solidified areas are intermingled with one another within the section of the film sample. In addition, the first areas correspond to first pixels, and the second areas correspond to second pixels.

WO 2004/017382 A2

PROCESS AND SYSTEM FOR LASER CRYSTALLIZATION PROCESSING OF FILM REGIONS ON A SUBSTRATE TO PROVIDE SUBSTANTIAL UNIFORMITY WITHIN AREAS IN SUCH REGIONS AND EDGE AREAS THEREOF, AND A STRUCTURE OF SUCH FILM REGIONS

SPECIFICATION

RELATED APPLICATION

This application claims priority to United States Provisional Application No. 60/405,083, which was filed on August 19, 2002, and is incorporated by reference.

NOTICE OF GOVERNMENT RIGHTS

The U.S. Government may have certain rights in this invention pursuant to the terms of the Defense Advanced Research Project Agency award number N66001-98-1-8913.

FIELD OF THE INVENTION

The present invention relates to techniques for processing of films, and more particularly to techniques for processing semiconductor films to spatially intermix multiple irradiations of areas of films of such thin films so as to obtain a substantial performance uniformity of electronic devices, such as thin-film transistor ("TFT") devices, situated therein.

BACKGROUND OF THE INVENTION

Films, such as silicon films or semiconductor films, are known to be used for providing pixels for liquid crystal display devices. Such films have previously been processed (i.e., irradiated by an excimer laser and then crystallized) via excimer laser annealing ("ELA") methods. Other more advantageous methods and systems for processing the semiconductor thin films for use in the liquid crystal displays and organic light emitting diode displays for fabricating large grained single crystal or polycrystalline silicon thin films using sequential lateral solidification

("SLS") techniques have been described. For example, U.S. Patent No. 6,322,625 issued to Im and U.S. patent application serial no. 09/390,537, the entire disclosures of which are incorporated herein by reference, and which are assigned to the common assignee of the present application, describe such SLS systems and processes. The patent documents describe certain techniques in which multiple areas on the semiconductor thin film are. e.g., sequentially irradiated.

The semiconductor films processed using the conventional system and processes often suffer from varying energy densities from one irradiated region of such thin film to the next. This primarily due to the fact that the laser beam fluence at least slightly varies from one shot to the next. For example, during the sequential irradiation of the neighboring regions of the thin film, the first region is irradiated by a first beam pulse (set of pulses) having a first energy fluence, the second region is irradiated by a second beam pulse (or set of pulses) having a second fluence which is at least slightly different that the fluence of the first beam pulse, and the third region is irradiated by a third beam pulse (or set of pulses) having a third fluence which is at least slightly different that the fluence of the second beam pulse, etc. Upon the irradiation of these areas, they can crystallize (e.g., due to at least partial melting). The resulting energy densities of the irradiated and crystallized first, second and third regions of the semiconductor thin film are all, at least to an extent, different from one another due to the varying fluences of the sequential beam pulses irradiating the neighboring regions.

The problem may arise after such fabrication of the semiconductor thin film, i.e., when thin-film transistor ("TFT") devices are placed in such areas irradiated and crystallized regions having differing energy densities. In particular, the performance of such TFT devices situated in the crystallized regions of the film may vary from one device to another because of their energy density differences. For example, while the TFT devices placed in each of the crystallized regions (which may be uniform therein) generally have uniform characteristics and operate in a substantially the same manner within each such region, the TFT devices do not operate in the uniform manner from one crystallized region to another. This manifests

itself in the fact that the same colors provided on the neighboring pixels of the display may appear different from one another.

Another problem of the unintended consequence of irradiating the neighboring regions of the semiconductor thin film with pulses each having a slightly differing fluences is that a transition from the one of these regions to the next consecutive region may be visible. This is due to the energy densities being different from one anther in the two neighboring regions, and because the transitions between the regions at the border regions thereof has a contrast from one to another because of such differing energy densities. Thus, it is possible that the transition between the first region to the next region is sharper than it may be intended.

Accordingly, it may be preferable to generate substrates which include the semiconductor films that reduce the effects of differing fluences of consecutive beam pulses irradiating neighboring regions of the semiconductor thin film, which later crystallize.

SUMMARY OF THE INVENTION

One of the objects of the present invention is to provide an improved process and system which can interpose crystallized areas from two sequential pulses (or set of pulses) on the substrate films such that the TFT devices can be situated in such areas so as to allow the neighboring regions of the thin film sample so as to have substantially the same performance of the TFT devices situated therein. Another object of the present invention is to interpose the crystallized areas of two sequential pulses (or set of pulses) in the border region between the neighboring regions of the sample so as to reduce a perception of having a visible border between the adjacent regions to reduce the contrast between the two neighboring regions.

In accordance with at least some of these objectives as well as others that will become apparent with reference to the following specification, it has now been determined that by specially dispersing the irradiation of one or more regions in the semiconductor thin film by portions of two or more different pulses (each of which has a differing fluence). It was also ascertained that dispersing the portions of

two sequential beam pulses in a border region between two adjacent regions of the semiconductor thin film reduces the perception of the border between the pixels.

In one exemplary embodiment of the present invention, a process and system for processing a semiconductor thin film sample are provided. In particular, a beam generator can be controlled to emit successive irradiation beam pulses at a predetermined repetition rate. Each irradiation beam pulse may be masked to define a first plurality of beamlets and a second plurality of beamlets. The first and second plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to at least partially melt irradiated portions of the section of the film sample. A particular portion of the section of the film sample is irradiated with the first beamlets of a first pulse of the irradiated beam pulses to melt first areas of the particular portion, the first areas being at least partially melted, leaving first unirradiated regions between respective adjacent ones of the first areas, and being allowed to resolidify and crystallize. After the irradiation of the particular portion with the first beamlets, the particular portion is again irradiated with the second beamlets of a second pulse of the irradiated beam pulses to melt second areas of the particular portion, the second areas being at least partially melted, leaving second unirradiated regions between respective adjacent ones of the second areas, and being allowed to resolidify and crystallize. The first irradiated and re-solidified areas and the second irradiated and re-solidified areas are intermingled with one another within the section of the film sample. In addition, the first areas correspond to first pixels, and the second areas correspond to second pixels.

In another exemplary embodiment of the present invention, respective positions of the first pixels are different than respective positions of the second pixels. Also, a location of at least one of the second irradiated areas is substantially the same as a location of at least one of the first unirradiated areas. The first unirradiated areas have substantially the same location as the second areas, and wherein the second unirradiated areas have substantially the same location as the first areas. The first and second irradiated and re-solidified areas form an entire cross-section of the section of the film sample. The locations of the first and second areas can be non-uniform, and

edges of the second irradiated and re-solidified areas are provided at a distance from the first irradiated and re-solidified areas.

In yet another exemplary embodiment of the present invention, the first beamlets have a first energy density, the second beamlets have a second energy density, and the first energy density is different from the second energy density. The masked irradiation beam pulses may further include a third plurality of beamlets which are provided for impinging the film sample. In addition, after the irradiation of the particular portion with the second beamlets, the particular portion is irradiated with the third beamlets to melt third areas of the particular portion. The third areas are melted throughout their thickness, leaving third unirradiated regions between respective adjacent ones of the third areas and being allowed to resolidify and crystallize. The third areas may correspond to the third pixels, and respective positions of the first and second pixels are different than respective positions of the third pixels. A location of at least one of the first and second areas can be substantially the same as (or different from) a location of at least one of the third unirradiated areas. Also, at least one of the first and second unirradiated areas have substantially the same locations as the third areas, and the third unirradiated areas have substantially the same locations as at least one of the first and second areas. The first, second and third resolidified areas may form an entire cross-section of the section of the film sample.

In still another exemplary embodiment of the present invention, edges of the first and second re-solidified areas are provided at a distance from the third re-solidified areas. In addition, the first beamlets may have a first energy density, the second beamlets may have a second energy density, and the third beamlets may have a third energy density such that the third energy density is different from at least one of the first energy density and the second energy density. The second beam pulse may immediately follow the first beam pulse, the first areas can be irradiated with the first beamlets when the film sample is provided at a first position of with respect to the irradiation beam pulses. The second areas can be irradiated with the second beamlets when the film sample is provided at a second position with respect to the irradiation beam pulses, the second position being closer to a center of the section of

the film sample than the second position. Further, the film sample may be translated relative to the irradiation beam pulses so that the impingement by the first beamlet of the film sample moves from the first position to the second position.

In a further exemplary embodiment of the present invention, the first areas are fully melted throughout their entire thickness, and the second areas are fully melted throughout their entire thickness. Also, the film sample may be translated so that the a further portion of the film sample is provided for irradiation by the first and second beamlets, the further portion being substantially adjacent to the particular portion of the film sample. The irradiation of the first and second areas can be repeated for processing the entire semiconductor thin film sample. A first edge of the further portion of the film sample can overlap a second edge of the particular portion of the film sample, and the irradiated and re-solidified areas in the first edge of the further portion may be intermingled with the re-solidified areas of the particular portion so as to prevent an overlap thereof.

The accompanying drawings, which are incorporated and constitute part of this disclosure, illustrate a preferred embodiment of the invention and serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a schematic block diagram of an exemplary embodiment of an irradiation system according to the present invention which allows the portions of sequential beam pulses (having different fluences) to irradiate regions of a semiconductor thin film provided on a sample such that these portions are interposed with one another these regions;

Fig. 1B is an enlarged cross-sectional side view of the sample which includes the semiconductor thin film;

Fig. 2 is a top exploded view of an exemplary embodiment of the sample conceptually subdivided, and having a semiconductor thin film thereon on which a process according to the present invention is performed for the entire surface area of a semiconductor thin film using the exemplary system of Fig. 1A;

Fig. 3 is a top view of a first exemplary embodiment of a mask according to the present invention which is divided into two areas such that respective set of beamlets being patterned by the first area and second areas are capable of irradiating the same region of the thin film, and the sections of the regions irradiated by each of the set of beamlets are dispersed throughout that region;

Figs. 4A-4H are sequential movements of the semiconductor film of a sample with respect to the pulsed beam as the beam pulse is patterned by the mask of Fig. 3 according to an exemplary embodiment of the present invention;

Figs. 5A-5H are irradiations, by the radiation beam pulse which is masked by the mask of Fig. 3 (which correspond to the movements of the sample illustrated in Figs. 4A-4H), and then re-solidifications and crystallizations of the particular portions of the semiconductor film provided on the sample at exemplary sequential stages of the processing according to the process of the present invention;

Fig. 6A is an illustration of the two particular areas irradiated, re-solidified and crystallized areas corresponding to the crystallized areas of Figs. 5G and 5H in which the entire TFT device is situated in the crystallized areas;

Fig. 6B is an illustration of the two particular areas irradiated, re-solidified and crystallized areas corresponding to the crystallized areas of Figs. 5G and 5H in which an active region of the TFT device is situated in the crystallized areas, while other regions are provided over border areas between the crystallized areas;

Fig. 7 is a top view of a second exemplary embodiment of a mask according to the present invention which is divided into three areas such that respective set of beamlets being patterned by the first, second and third areas are capable of irradiating the same region of the thin film, and the sections of the regions irradiated by each of the set of beamlets are dispersed throughout that region;

Figs. 8A-8H are sequential movements of the semiconductor film of a sample with respect to the pulsed beam as the beam pulse is patterned by the mask of Fig. 7 according to an exemplary embodiment of the present invention;

Figs. 9A-9H are irradiations, by the radiation beam pulse which is masked by the mask of Fig. 7 (which correspond to the movements of the sample illustrated in Figs. 8A-8H), and then re-solidifications and crystallizations of the particular portions of the semiconductor film provided on the sample at exemplary sequential stages of the processing according to the process of the present invention;

Fig. 10 is a top view of a third exemplary embodiment of a mask according to the present invention which is divided into four areas such that respective set of beamlets being patterned by the first and second areas are used to laterally grow grains in first irradiated sections of the irradiated, respective set of beamlets being patterned by the third and fourth areas are used to laterally grow grains in second irradiated sections of the irradiated region, and the first and second sections of the regions irradiated by the beamlets are dispersed throughout that region;

Figs. 11A-11H are sequential movements of the semiconductor film of a sample with respect to the pulsed beam as the beam pulse is patterned by the mask of Fig. 10 according to an exemplary embodiment of the present invention so as to promote a sequential lateral solidification ("SLS") of grains in certain areas of the same region of the semiconductor thin film;

Figs. 12A-12F are irradiations, by the radiation beam pulse which is masked by the mask of Fig. 10 (which correspond to the movements of the sample illustrated in Figs. 11A-11H), and then re-solidifications and crystallizations of the particular portions of the semiconductor film provided on the sample at exemplary sequential stages of the processing according to the process of the present invention based on SLS principles;

Fig. 13 is a top view of a fourth exemplary embodiment of a mask according to the present invention which is divided into a center area and border areas such that respective set of beamlets being patterned by the border areas irradiate a region so that they are interposed between the sections of the region irradiated by the beamlets patterned by the next sequential beam pulse irradiating the adjacent region, and the border sections of the neighboring regions irradiated by the beamlets of later beam pulses are dispersed throughout that border sections;

Figs. 14A-14D are irradiations, by the radiation beam pulse which is masked by the mask of Fig. 13 , and then re-solidifications and crystallizations of the particular portions of the semiconductor film provided on the sample at exemplary sequential stages of the processing according to the process of the present invention;

Fig. 15 is an illustration of the number of irradiations that the areas being irradiated by the beam pulse patterned by the mask of Fig. 13 are subjected to;

Fig. 16 is a flow diagram representing a first exemplary processing procedure of the present invention under at least partial control of a computing arrangement of Fig. 1A using the exemplary techniques of the present invention of Figs. 4A-4H, 5A-5H, 8A-8H, 9A-9H, 11A-11H and 12A-12F; and

Fig. 17 is a flow diagram representing a second exemplary processing procedure of the present invention under at least partial control of a computing arrangement of Fig. 1A using the exemplary techniques of the present invention of Figs. 14A-14D.

DETAILED DESCRIPTION

It should be understood that various systems according to the present invention can be utilized to generate, solidify and crystallize one or more areas on the semiconductor (e.g., silicon) thin film which have which can be interposed between previously crystallized areas of such semiconductor thin film. The exemplary embodiments of the systems and process to achieve such areas, as well as of the resulting crystallized semiconductor thin films shall be described in further detail below. However, it should be understood that the present invention is in no way limited to the exemplary embodiments of the systems, processes and semiconductor thin films described herein.

Certain systems for providing a continuous motion SLS are described in U.S. Patent Application Serial No. 09/526,585 (the "'585 application"), the entire disclosure of which is incorporated herein by reference. Substantially similar systems according to the exemplary embodiment of the present invention can be employed to generate the irradiated, solidified and crystallized portions of the semiconductor film

described above using which it is possible to disperse newly irradiated, solidified and crystallized areas with the previously crystallized portions. In particular, the system according to the present invention is used on a sample 170 which has an amorphous silicon thin film thereof that is being irradiated by irradiation beam pulses to promote the irradiation, subsequent solidification and crystallization of the particular areas of the semiconductor thin film. The exemplary system includes a beam source 110 (e.g., a Lambda Physik model LPX-315I XeCl pulsed excimer laser) emitting an irradiation beam (e.g., a laser beam), a controllable beam energy density modulator 120 for modifying the energy density of the laser beam, a MicroLas two plate variable attenuator 130, beam steering mirrors 140, 143, 147, 160 and 162, beam expanding and collimating lenses 141 and 142, a beam homogenizer 144, a condenser lens 145, a field lens 148, a projection mask 150 which may be mounted in a translating stage (not shown), a 4×-6× eye piece 161, a controllable shutter 152, a multi-element objective lens 163 for focusing a radiation beam pulse 164 onto the sample 170 having the semiconductor thin film to be processed mounted on a sample translation stage 180, a granite block optical bench 190 supported on a vibration isolation and self-leveling system 191, 192, 193 and 194, and a computing arrangement 100 (e.g., a general purpose computer executing a program according to the present invention or a special-purpose computer) coupled to control the beam source 110, the beam energy density modulator 120, the variable attenuator 130, the shutter 152 and the sample translation stage 180.

The sample translation stage 180 is preferably controlled by the computing arrangement 100 to effectuate translations of the sample 170 in the planar X-Y directions, as well as in the Z direction. In this manner, the computing arrangement 100 controls the relative position of the sample 40 with respect to the irradiation beam pulse 164. The repetition and the energy density of the irradiation beam pulse 164 are also controlled by the computer 100. It should be understood by those skilled in the art that instead of the beam source 110 (e.g., the pulsed excimer laser), the irradiation beam pulse can be generated by another known source of short energy pulses suitable for at least partially melting (and possibly fully melting throughout their entire thickness) selected areas of the semiconductor (e.g., silicon)

thin film of the sample 170 in the manner described herein below. Such known source can be a pulsed solid state laser, a chopped continuous wave laser, a pulsed electron beam and a pulsed ion beam, etc. Typically, the radiation beam pulses generated by the beam source 110 provide a beam intensity in the range of 10 mJ/cm^2 to 1J/cm^2, a pulse duration (FWHM) in the range of 10 to 103 nsec, and a pulse repetition rate in the range of 10 Hz to 104 Hz.

While the computing arrangement 100, in the exemplary embodiment of the system shown in Fig. 1A, controls translations of the sample 170 via the sample stage 180 for carrying out the processing of the semiconductor thin film of the sample 170 according to the present invention, the computing arrangement 100 may also be adapted to control the translations of the mask 150 and/or the beam source 110 mounted in an appropriate mask/laser beam translation stage (not shown for the simplicity of the depiction) to shift the intensity pattern of the irradiation beam pulses 164, with respect to the semiconductor thin film of the sample 170, along a controlled beam path. Another possible way to shift the intensity pattern of the irradiation beam pulse is to have the computer 100 control a beam steering mirror. The exemplary system of Fig. 1 may be used to carry out the processing of the silicon thin film of the sample 170 in the manner described below in further detail. The mask 150 should be used by the exemplary system of the present invention to well define the profile of the resulting masked beam pulse 164 and to reduce the non-uniformity of the adjacent portions and edge regions of the portions of the semiconductor thin film when these portions are irradiated by such masked beam pulse 164 and then crystallized.

As illustrated in Fig. 1B, the semiconductor thin film 175 of the sample 170 can be directly situated on e.g., a glass substrate 172, and may be provided on one or more intermediate layers 177 there between. The semiconductor thin film 175 can have a thickness between 100Å and 10,000Å (1μm) so long as at least certain necessary areas thereof can be completely melted throughout their entire thickness. According to an exemplary embodiment of the present invention, the semiconductor thin film 175 can be composed of silicon, germanium, silicon germanium (SeGe), all of which preferably have low levels of impurities. It is also possible to utilize other elements or semiconductor materials for the semiconductor thin film 175. The

intermediary layer 177, which is situated immediately underneath the semiconductor thin film 175, can be composed of silicon oxide (SiO_2), silicon nitride (Si_3N_4), and/or mixtures of oxide, nitride or other materials that are suitable for promoting grain growth within the designated areas of the semiconductor thin film 175 of the sample 170. The temperature of the glass substrate 172 can be between room temperature and 800°C. Higher temperatures of the glass substrate 172 can be accomplished by preheating the substrate 172 which would effectively allow larger grains to be grown in the irradiated, re-solidified, and then crystallized areas of the semiconductor thin film 175 of the sample 170 due to the proximity of the glass substrate 172 to the thin film 175.

Fig. 2 shows an enlarged view of an exemplary embodiment of the semiconductor thin film 175 (e.g., an amorphous silicon thin film) of the sample 170, and the relative translation paths of the beam pulse 164 with respect to the locations on the sample 170. This exemplary sample 170 has exemplary dimensions of 40 cm in the Y direction by 30 cm in the X direction. The sample 170 can be conceptually subdivided into a number of columns (e.g., a first conceptual column 205, a second conceptual column 206, a third conceptual column 207, etc.). The location/size of each conceptual column may be stored in a storage device of the computing arrangement 100, and utilized by the computing arrangement 100 for later controlling the translation of the sample 170, and/or firing of the beam by the beam source 110 on these locations of the semiconductor thin film 175, or on other locations that are based on the stored locations. Each of the columns 205, 206, 207, etc. is dimensioned, e.g., ½ cm in the Y direction by 30 cm in the X direction. Thus, if the sample 170 is sized 40 cm in the Y direction, the sample 150 may be conceptually subdivided into eighty (80) columns. The sample 170 may also be conceptually subdivided into such columns having other dimensions (e.g., 1 cm by 30 cm columns, 2 cm by 30 cm columns, 2 cm by 30 cm columns, etc.). In fact, there is absolutely no restrictions on the dimensions of the conceptual columns of the sample 170 so long as the beam pulse 164 is capable of irradiating and completely melting certain areas of the semiconductor thin film 175 in such columns so as to promote small grain growth within such areas for forming uniform areas on the film sample 175 to allow the

interposition of the areas irradiated by two different (e.g., sequential) beam pulses which generally have differing fluences between one another in the same region of the semiconductor thin film. The location/dimension of each column, and the locations thereof, are stored in the storage device of the computing arrangement 100, and utilized by such computing arrangement 100 for controlling the translation of the translation stage 180 with respect to the beam pulse 164 and/or the firing of the beam 111 by the beam source 110.

The semiconductor thin film 175 can be irradiated by the beam pulse 164 which is patterned using the mask 150 according to a first exemplary embodiment of the present invention as shown in Fig. 3. The first exemplary mask 150 is sized such that its cross-sectional area is larger than that of the cross-sectional area of the beam pulse 164. In this manner, the mask 150 can pattern the pulsed beam to have a shape and profile directed by the open or transparent regions of the mask 150. The mask 150 is subdivided into a first section A 300 and a second section B 350. The first section A 300 has multiple open or transparent regions 310 which are separated from one another by beam-blocking regions 320. The second section B 350 has multiple open or transparent regions 360 which are separated from one another by beam-blocking regions 370. The open or transparent regions 310, 360 of first and second sections 300, 350 the mask 150, respectively, can also be referred to as "slits." These slits permit small beam pulses (or beamlets) to irradiate there-through and completely melt the areas of the semiconductor thin film 175 that they impinge. The dimensions of the slits 310, 360 can be 0.1 μm by 0.5 μm, 0.5 μm by 0.5 μm, etc. It should be clearly understood that other dimensions of the slits are possible, and are within the scope of the present invention. For example, the slits can have a rectangular shape, a circular shape, a triangular shape, a chevron shape, a diamond shape, etc. In this manner, the mask 150 is capable of patterning the beam pulse 164 so as to impinge the semiconductor thin film 175 of the sample 170 at predetermined portions thereof as shall be described in further detail below.

A first exemplary embodiment of the process according to the present invention illustrated in Fig. 4A-4H and 5A-5H shall now be described below with reference to the relative movement of the sample 170 with respect to the impingement

of the sections of the semiconductor thin film 175 by the beam pulse 164 patterned by the mask of Fig. 3. Exemplary translation of the sample 170 as it relates to the direction of the masked beam pulse 164 shall be described below also with reference to Fig. 2. The sample 170 may be either by moving the mask 150 or the sample translation stage 180, in order to irradiate selective areas of the semiconductor thin film 175 of the sample 170. For the purposes of the foregoing, the length and width of the masked beam pulse 164 may be 0.1 cm x 0.5 cm. However, it should be understood the masked beam pulse 164 is not limited to such shape and size. Indeed, other shapes and/or sizes of the beam pulse 164, which is patterned and dimensioned by the mask 150.

After the sample 170 is conceptually subdivided into columns 205, 206, 207, etc., a pulsed laser beam 111 is activated (by actuating the beam source 110 using the computing device 100 or by opening the shutter 130), and produces the pulsed laser beamlets 164 which impinges on a first location 220 which is away from the semiconductor thin film 175. Then, the sample 170 is translated and accelerated in the forward X direction under the control of the computing arrangement 100 to reach a predetermined velocity with respect to the fixed position beamlets in a first beam path 225.

In one exemplary variation of the process of the present invention, the pulsed beamlets 164 can reach a first edge 210' of the sample 170 preferably when the velocity of the movement of the sample 170 with respect to the pulsed laser beam 149 reaches the predetermined velocity. Then, the sample 170 can be continuously (e.g., without stopping) translated in the -X direction at the predetermined velocity so that the pulsed beamlets 164 continue irradiating successive portions of the sample 170 for an entire length of a second beam path 230.

Upon the passing the first edge 210', the beam pulse 149 is passed through the first section A 300 and the section B 350 of the mask 150 which patterns the beam pulse 149 to become the masked beam pulse 164. As shown in Fig. 5A, the masked beam pulse 164 patterned by the first section A 300 of the mask 150 impinges a first region 410 on the first conceptual column 205 of the semiconductor thin film

sample 170, while the masked beam pulse 164 patterned by the second section B 350 of the mask 150 irradiates an area away from the edge 210' of the semiconductor thin film 170. Therefore, as shown in Figs. 4A and 5A, the first region 410 of the semiconductor thin film is irradiated only by the beam pulse 164 masked by the first section A 300 of the mask 150. As shown in Fig. 5A, the irradiated first region 410 is composed of irradiated first portions 415 which are provided at a distance from one another, and substantially match the positions and orientations of the slits 310 of the first section A 300 of the mask 150. In particular, the irradiated first portions 415 are provided such that the portions between these irradiated first portions 415 can be irradiated with another beam pulse (e.g., a subsequent masked beam pulse). In a preferred embodiment of the present invention, such portions provided between irradiated first portions 415 are sufficiently large to enable the entire new portions having an approximately the same size as the first portions 415 to be irradiated therein by another beam pulse (e.g., without overlapping any portion of the irradiated first portions 415). It is possible that the masked beam pulse 164 has sufficient fluence or intensity to completely melt the first portions 415 being irradiated throughout their entire thickness. In addition, these portions 415 can be partially melted by the masked beam pulse 164.

Thereafter, as shown in Figs. 4B and 5B, the sample 170 is continued to be translated in the –X direction relative to the masked beam pulse 164, and the beam pulse is masked by the first section A 300 and the second section B 350 of the mask 150 such that the first half portion of the masked beam pulse 164 patterned by the first section A 300 irradiates a second region 420 on the conceptual first column 205 of the semiconductor thin film 175, and the second half portion of the masked beam pulse 164 patterned by the second section B 350 irradiates the first region 410. Thus, first areas 425 of the second region 420 are positioned and irradiated in a substantially the same manner as the first areas 415 of the first region 410. It should be noted that prior to the irradiation of the first region 410 by the second half portion of the masked beam pulse 164 which is patterned by the second section B 350, the first portions 415 which were irradiated by the previous beam pulse (as shown in Fig. 5A) are allowed to solidify and crystallize. In addition, second portions 418 of the

first region 410 which were irradiated by the second half portion of the beam pulse 164 masked by the second section B 350 of the mask 150 are interposed between the crystallized first portions 415. It is noted that the fluence used by the half portion of the masked beam pulse 164 to irradiate the first areas 415 is different from the fluence used to by a half portion of another masked beam pulse 164 to irradiate the second areas 418. Due to the fact that the first and second areas 415, 418 are interposed between one another, the performance of the TFT devices placed on such crystallized areas 415, 418 is preferably uniform throughout the first region 410.

Next, as shown in Figs. 4C and 5C, the sample 170 is continued to be translated in the –X direction relative to the masked beam pulse 164, and the beam pulse 149 is again masked by the first section A 300 and the second section B 350 of the mask 150 such that the half portion of the masked beam pulse 164 patterned by the first section A 300 irradiates a third region 430 on the conceptual first column 205 of the semiconductor thin film 175, and the second half portion of the masked beam pulse 164 patterned by the second section B 350 irradiates the second (previously partially irradiated) region 420. First areas 435 of the third region 430 are positioned and irradiated in a substantially the same manner as the first areas 415 of the first region and the first areas 425 of the second region 420. Similar to the discussion above regarding the crystallization of the first irradiated areas 415 of the first region 410, the first areas 425 which were irradiated by the previous beam pulse (as shown in Fig. 5B) are allowed to solidify and crystallize. Further, second areas 428 of the second region 420 which were irradiated by the second half portion of the beam pulse 164 masked by the second section B 350 of the mask 150 are interposed between the crystallized first portions 425. In addition, the first areas 415 and the second areas 418 (and in particular all areas) of the first region 410 are crystallized.

Figs. 4D and 5D show the sample 170 being translated in the –X direction relative to the masked beam pulse 164, and the beam pulse is again masked by the first section A 300 and the second section B 350 of the mask 150 such that the half portion of the masked beam pulse 164 patterned by the first section A 300 irradiates a further region 430 on the conceptual first column 205 of the semiconductor thin film 175, and the second half portion of the masked beam pulse

164 patterned by the second section B 350 irradiates the third (previously partially irradiated) region 430. Thus, second portions 438 of the third region 430 that are irradiated by the half portion of the masked beam pulse 164 are interposed between the crystallized first portions 435.

This translation continues until all regions 410, 420, 430, ..., 490 are completed such that all of the respective first and second portions thereof are crystallized in the first conceptual column 205, i.e., until the pulsed beamlets 164 reach a second edge 210" of the sample 170, as illustrated in Figs. 4E and 5E. When the beam pulse 164 passes the second edge 210", the translation of the sample 170 may be slowed with respect to the beam pulse 164 (in a third beam path 235) to reach a second location 240 (see Fig. 2). It should be noted that it is not necessary to shut down the pulsed beam 111 after the beam pulse 164 has crossed the second edge 210" of the sample 170 because it is no longer irradiating the sample 170.

While being away from the sample 170 and the second edge 210", the sample 170 is continued to be translated in a -Y direction to a third location 247 via a fourth beam path 245 so as to be able to irradiate the sections of the semiconductor thin film 175 along the second conceptual column 206. Then, the sample 170 is allowed to settle at that location 247 to allow any vibrations of the sample 170 that may have occurred when the sample 170 was continued to be translated to the third location 247 to cease. Indeed, for the sample 170 to reach the second conceptual column 206, it is continued to be translated approximately ½ cm for the columns having a width (in the -Y direction) of ½ cm. The sample 170 is then accelerated to the predetermined velocity via a fourth beam path 250 in the –X direction so that the impingement of the semiconductor thin film 175 by the beam pulse 164 reaches, and then bypasses the second edge 210".

Thereafter, the sample 170 is continued to be translated along a fifth beam path 255, and the exemplary process described above with respect to the irradiation of the first column 205 may then be repeated for the second conceptual column 206 to irradiate further areas 410, 420, and their respective small-grained regions 415, 425 and laterally-grown regions 418, 428 while translating the sample in

the +X direction. However, instead of using the first section A 300 as providing the half beam pulse to first irradiate a first region 510 of the second conceptual column 205 of the semiconductor thin film 175, the second section B 350 of the mask is used for the patterning of the beam pulse, and irradiating the first region 510 of the second conceptual column 206.

In particular, Figs. 4F and 5F show that the masked beam pulse 164 patterned by the second section B 350 of the mask 150 impinges the first region 510 on the second conceptual column 206 of the semiconductor thin film sample 170, while the masked beam pulse 164 patterned by the first section A 300 of the mask 150 irradiates an area away from the semiconductor thin film 175. Therefore, the first region 410 of the semiconductor thin film 175 is irradiated only by the beam pulse 164 masked by the second section B 350 of the mask 150. As shown in Fig. 5F, the irradiated first region 510 of the second conceptual column 206 is composed of irradiated first portions 515 which are provided at a distance from one another, and substantially match the positions and orientations of the slits 360 of the second section B 350 of the mask 150. Figs. 4G, 4H, 5G, 5H show that the regions of the second conceptual column 206 of the semiconductor thin film 175 are irradiated by the beam pulses patterned by the mask 150, such that the second half portion of the masked beam pulse 164 lead the first half portion of the masked beam pulse 164 in their irradiation of all of the regions of the second conceptual column 206 of the semiconductor thin film 175.

In this manner, all conceptual columns of the sample 170 can be properly irradiated. In particular, when the beam pulse 164 reaches the first edge 210', the translation of the sample 170 is decelerated along a sixth beam path 260 to reach a fourth location 265. At that point, the sample 170 is continued to be translated in the –Y direction along the seven beam path 270 for the beam pulse to be outside the periphery of the sample 170 to reach fifth location 272, and the translation of the sample 170 is allowed to be stopped so as to remove any vibrations from the sample 170. Thereafter, the sample 170 is accelerated along the eighth beam path 275 in the –X direction so that the beam pulse 164 reaches and passes the first edge 210' of the sample 170, and the beam pulse 164 irradiates and at least partially melts certain areas

in the third conceptual column 207 so that they can crystallize in substantially the same manner as described above for the areas 410, 420, 430, ..., 490 of the first conceptual column 205 and shown in Figs. 5A-5E.

This procedure may be repeated for all conceptual columns of the semiconductor thin film 175, or for selective columns of particular sections of the thin film 175 which are not necessarily conceptually subdivided into columns. With this exemplary procedure according to the present invention, because the first and second crystallized areas of all regions in the semiconductor thin film 175 are interposed between one another, the performance of the TFT devices placed on such crystallized areas is approximately uniform throughout the TFT device situated on such crystallized areas.

In addition, it is possible for the computing arrangement 100 to control the firing of the beam 111 by the beam source 110 based on the predefined location stored in the storage device of the computing arrangement 100 (e.g., instead of irradiating the semiconductor thin film 175 by setting predetermined pulse durations). For example, the computing arrangement 100 can control the beams source 110 to generate the beam 111 and irradiate only at the predetermined locations of certain areas of the thin film 175 with its corresponding beam pulse 164, such that these locations are stored and used by the computing arrangement 100 to initiate the firing of the beam 111 which results in the irradiation by the beam pulse only when the sample 170 is continued to be translated to situate those areas directly in the path of the beam pulse 164. The beam source 110 can be fired via the computing arrangement 100 based on the coordinates of the location in the X direction.

In addition, it is possible to translate the sample 170 in a manner which is not necessary continuous, when the path of the irradiation of the beam pulse 164 points to the areas on the semiconductor thin film 175 to be melted and crystallized. Thus, it is possible for the translation of the sample 170 to be stopped in the middle of the sample 170, with the area in the middle being irradiated, at least partially melted, and then re-solidified and crystallized. Thereafter, the sample 170 can be moved so that another section of the semiconductor thin film 175 is arranged in the path of the

beam pulse 164, such that the translation of the sample is then stopped again and the particular section is irradiated and at least partially melted in accordance with the exemplary embodiment of the process described in great detail above, as well as the embodiments of the process which shall be described below.

Fig. 6A shows an illustration of the first and second irradiated, re-solidified and crystallized areas 415 and 418 of the first region 410 illustrated in Figs. 5C-5H. In particular, Fig. 8A shows that the entire TFT devices 610, 620 can be situated within the respective first and second areas 415, 418 of the first region. The first TFT device 610 situated in the first area 415 of the first region 410 includes a gate 612, a drain 614, a source 616 and an active region 618, all of which are provided away from the border area of the first area 415. Similarly, for the second TFT device 610, its gate 622, drain 624, source 626, and especially active region 628 are also situated such that that they do not overlap the second are 418 of the first region 410.

Fig. 6B shows an illustration of the first and second irradiated, re-solidified and crystallized areas 415 and 418 of the first region 410 illustrated in Figs. 5C-5H with the respective TFT devices 610', 620' provided thereon. In this exemplary embodiment, only respective active regions 618', 628' of the TFT devices 610', 620' are provided within the respective first and second crystallized areas 415, 418, while other portions of the TFT devices 610', 620' are situated on the borders of the these areas 415, 418. In particular, the first TFT device 610' includes an active region 618' which entirely situated in the first area 415 of the first region 410, while a gate 612', a drain 614' and a source 616' of this TFT device 610' overlap the borders of the first area 415. Also, for the second TFT device 610', an active region 628' thereof is entirely situated within the respective second area 418 of the first region 410, while a gate 622', a drain 624' and a source 626' of the second TFT device 620' are provided directly on the borders of such second area 418. It should be understood that any one of the gate 612, 612', 622, 622', drain 614, 614', 624, 624' and source 616, 616', 626, 626' can be provided on the first and second areas 415, 418 and the border regions thereof. In addition, according to still another embodiment of the present invention, it is possible to situate a small portion of the active regions 618', 628' of the respective TFT devices 610', 620' on the border regions of the first area 415 and/or the second

area 418, while still having the major portions of these active regions 618', 628' provided within such first and second areas 415, 418.

Fig. 7 is a top view of a second exemplary embodiment of the mask 150' according to the present invention which is divided into a first section A' 710, a second section B' 720 and a third section C' 730 such that respective set of beamlets being patterned by the first, second and third sections 710, 720, 730 are capable of irradiating the same region of the thin film, and the sections of the regions irradiated by each of the set of beamlets are dispersed throughout that region. Similar to the first exemplary mask 150 illustrated in Fig. 3, the first, second and third sections 710, 720, 730 have respective multiple open or transparent regions 715, 725, 735 which are separated from one another by beam-blocking regions, and can be referred to as slits. These slits permit small beam pulses (or beamlets) to irradiate there-through and at least partially melt the areas of the semiconductor thin film 175 that they impinge.

A second exemplary embodiment of the process according to the present invention is described below with reference Figs. 8A-8H and 9A-9H. as for the first embodiment of the process, the relative translation of the sample 170 is accelerated until the beam pulse 164 reaches the first edge 210'. Upon the passing the first edge 210', the beam pulse 149 is passed through the first section A' 710, the second section B' 720 and the third section C' 730 of the mask 150' which patterns the beam pulse 149 to become the masked beam pulse 164 in the substantially the same patterns as that of the mask 150'. As shown in Figs. 8A and 9A, the masked beam pulse 164 patterned by the first section A' 710 of the mask 150' so as to impinge and irradiate a first region 810 on the first conceptual column 205 of the semiconductor thin film sample 170, while the masked beam pulse 164 patterned by the second section B' 720 and the third section C' 730 of the mask 150' irradiates an area away from the edge 210' of the semiconductor thin film 170. Therefore, as shown in Figs. 8A and 9A, the first region 810 of the semiconductor thin film is irradiated only by the beam pulse 164 masked by the first section A' 710 of the mask 150'. As shown in Fig. 9A, the irradiated first region 810 is initially composed of irradiated first portions 815 which are provided at a distance from one another, and substantially match the positions and orientations of the slits 715 of the first section

A' 710 of the mask 150'. As with the first embodiment shown in Figs. 4A-4H and 5A-5H, the irradiated first portions 815 of the first region 810 are provided such that the portions between these irradiated first portions 815 can be irradiated with another beam pulse (e.g., a subsequent masked beam pulse).

Thereafter, as shown in Figs. 8B and 9B, the sample 170 is continued to be translated in the –X direction relative to the masked beam pulse 164, and the beam pulse is masked by the first section A' 710 and the second section B' 720 of the mask 150' such that the first one-third portion of the beam pulse 164 (i.e., patterned by the first section A' 710) irradiates a second region 820 on the conceptual first column 205 of the semiconductor thin film 175, and the second one-third portion of the masked beam pulse 164 (i.e., patterned by the second section B' 720) irradiates the first region 810. The third one-third portion of the masked beam pulse 164 which is patterned by the third section C' 730 of the mask 150' is irradiated away from the semiconductor thin film 175 (i.e., outside of the edge 210'). Thus, first areas 825 of the second region 820 are irradiated and situated in a substantially the same manner as the first areas 815 of the first region 810. It should be noted that prior to the irradiation of the first region 810 by the second one-third portion of the masked beam pulse 164 which is patterned by the second section B' 720, the first portions 815 which were irradiated by the previous beam pulse (as shown in Fig. 9A) are allowed to solidify and crystallize. In addition, second portions 817 of the first region 810 which were irradiated by the second one-third portion of the beam pulse 164 masked by the second section B' 720 of the mask 150' are interposed between the crystallized first portions 815. Based on the configuration of the first, second and third sections 710, 720, 730 of the mask 150', at such point, there are still unirradiated portions provided in the first region 810, even though first and second portions 815, 817 have been irradiated by the first one-third portion of the first masked beam pulse 164 and the second one-third portion of the subsequent masked beam pulse 164.

Then, as shown in Figs. 8C and 9C, the sample 170 is again continued to be translated in the –X direction relative to the masked beam pulse 164, and the beam pulse is masked by the first, second and third sections 710, 720, 730 of the mask 150' such that the first one-third portion of the beam pulse 164 (i.e., patterned by the

first section A' 710) irradiates a third region 830 on the conceptual first column 205 of the semiconductor thin film 175, the second one-third portion of the masked beam pulse 164 (i.e., patterned by the second section B' 720) irradiates the second region 820, and the third one-third portion of the masked beam pulse 164 (i.e., patterned by the third section C' 730) irradiates the first region 810. Thus, first areas 835 of the second region 820 are irradiated and situated in a substantially the same manner as the first areas 815, 825 of the first and second regions 810, 820, respectively. Also, second areas 827 of the second region 820 are irradiated and situated in a substantially the same manner as the second areas 817 of the first region 810. Prior to the irradiation of the first region 810 by the third one-third portion of the masked beam pulse 164 which is patterned by the third section C' 730, the first and second portions 815, 817 which were irradiated by two previous beam pulses (as shown in Figs. 9A and 9B) are allowed to solidify and crystallize. Also, before the irradiation of the first region 820 by the second one-third portion of the masked beam pulse 164 which is patterned by the second section B' 720, the first portions 825 which were irradiated by the first previous beam pulse (as shown in Figs. 9A) are also allowed to solidify and crystallize.

Further, the third portions 818 of the first region 810 which were irradiated by the third one-third portion of the beam pulse 164 masked by the third section C' 730 of the mask 150' are interposed between the crystallized first and second portions 815, 817. Also, the second portions 827 of the second region 820 which were irradiated by the second one-third portion of the beam pulse 164 masked by the second section B' 730 of the mask 150' are interposed between the crystallized first portions 825. Based on the configuration of the first, second and third sections 710, 720, 730 of the mask 150', there are no longer any unirradiated portions provided in the first region 810 after the irradiation thereof by the third one-third portion of the masked beam pulse 164. Figs. 8D and 9D illustrate that upon the translation of the sample 170 in the –X direction and irradiating the first conceptual row 205 of the semiconductor thin film 175 by the fourth sequential masked beam pulse 164, the first region 810 has all portions 815, 817, 818 thereof irradiated and crystallized.

Similar to the discussion above with reference to the embodiment of the present invention illustrated in Figs. 4A-4H and 5A-5H, the fluence used by the first one-third portions of the masked beam pulse 164 to irradiate the first areas 815 is different from each of the second and third one-third portions of the masked beam pulse 164 used to irradiate the second and third areas 817, 818, respectively. Due to the fact that the first, second and third areas 815, 817, 818 are interposed between one another, the performance of the TFT devices placed on such crystallized areas 815, 817, 818 is uniform throughout the first region 810. This procedure is repeated in the same manner for the entire first conceptual column 205 of the semiconductor thin film 175 until all regions thereof are irradiated and crystallized substantially in the same manner as provided above for with reference to the first region 810 of the semiconductor thin film 175, and as shown in Fig 8D, 8E, 9D, 9E.

Then, when the second conceptual column 206 is started to be processed, the first one-third portion of the beam which impinges and irradiates first portions 915 of the first region 910 of this second conceptual column 206 of the semiconductor thin film 175 which were masked by the third section C' 730 of the mask 150' (see Figs. 8F, 9F). Thus, Figs. 8G, 8H, 9G, 9H show that the regions of the second conceptual column 206 of the semiconductor thin film 175 is irradiated by the beam pulses patterned by the mask 150', such that the third one-third portion of the masked beam pulse 164 leads the second one-third portion of the masked beam pulse 164, which then lead the third one-third portion of the masked beam pulse 164 in their irradiation of all of the regions of the second conceptual column 206 of the semiconductor thin film 175 according to the second embodiment of the present invention.

In this manner, all conceptual columns of the sample 170 can be properly irradiated by the beam pulses 164 that are patterned by the mask 150'. The translation and irradiation of the third conceptual column 207 is substantially the same as the irradiation of the first conceptual column 205, and shall not be described in further detail below.

Fig. 10 shows a top view of a third exemplary embodiment of the mask 150'' according to the present invention which is divided into four sections (i.e., the first top section 1000, a first bottom section 1020, a second top section 1050 and a second bottom section 1070). In particular, the respective set of beamlets being patterned by the slits 1010, 1030 of the first top and bottom sections 1000, 1020 are used to laterally grow grains in first irradiated portions of irradiated regions. The slits 1030 of the first bottom section 1020 are provided at an vertical offset 1040 from the slits 1010 of the first top section 1000. In addition, the respective set of beamlets being patterned by the slits 1060, 1080 of the second top and bottom sections 1050, 1170, respectively, are used to laterally grow grains in second irradiated portions of the same irradiated regions. The slits 1080 of the second bottom section 1070 are provided at an vertical offset 1090 from the slits 1060 of the second top section 1050. The first and second portions of these regions irradiated and laterally grown by the beamlets in this manner are dispersed throughout that region between one another. It is noted that using this exemplary third mask 150'', the layout of the resulting crystallized portions of the semiconductor thin film 175 is substantially similar as that of the first exemplary embodiment of the mask 150 illustrated in Fig. 3. However, the first portions 415, 425, etc. and the second portions 418, 428, etc. of the regions 410, 420, etc. in the semiconductor thin film 175 of Figs. 5A-5H are somewhat smaller than the first and second portions in the regions of the semiconductor thin film 175 as shall be described herein below with reference to Figs. 11A-11H and 12A-12F according to the third exemplary embodiment of the present invention. This is because the first and second portions of the semiconductor thin film 164 that are crystallized using the third exemplary embodiment of the process according to the present invention undergo lateral grain growth as provided in further detail below.

As shown in Figs. 11A and 12A, the masked beam pulse 164 patterned by the first top section X 1000 of the mask 150'' so as to impinge and irradiate a first region 810 on the first conceptual column 205 of the semiconductor thin film sample 170, while the masked beam pulse 164 patterned by the first bottom section X' 1030, the second top section Y 1050, and the second bottom section Y' 1070 of the mask 150'' irradiate an area away from the edge 210' of the semiconductor thin film 170.

Therefore, as shown in Figs. 11A and 12A, the first region 1110 of the semiconductor thin film is irradiated only by the beam pulse 164 masked by the first top section X 1000 of the mask 150''. As shown in Fig. 12A, the irradiated first region 1110 is initially composed of irradiated first portions 1112 which are provided at a distance from one another, and substantially match the positions and orientations of the slits 1010 of the first top section X 1000 of the mask 150''. As with the first embodiment shown in Figs. 4A-4H and 5A-5H, the irradiated first portions 1112 of the first region 1110 are provided such that the portions between these irradiated first portions 1112 can be irradiated with another beam pulse (e.g., a later-applied masked beam pulse).

Thereafter, as shown in Figs. 11B and 12B, the sample 170 is continued to be translated in the –X direction relative to the masked beam pulse 164, and the beam pulse is masked by the first top section X 1000 and the first bottom section X' 1020 of the mask 150'' such that the first one-fourth portion of the beam pulse 164 (i.e., patterned by the first top section X 1000) irradiates a second region 1120 on the conceptual first column 205 of the semiconductor thin film 175, and the second one-fourth portion of the masked beam pulse 164 (i.e., patterned by the first bottom section X' 1020) irradiates the first region 1110. The second top and bottom one-fourth portions of the masked beam pulse 164 which are patterned by the second top section Y 1050 and the second bottom section Y' 1070 of the mask 150', respectively. is irradiated away from the semiconductor thin film 175 (i.e., outside of the edge 210'). First areas 1122 of the second region 1120 are irradiated and situated in a substantially the same manner as the first areas 1112 of the first region 1110.

It should be noted that prior to the irradiation of the first region 1110 by the second one-fourth portion of the masked beam pulse 164 which is patterned by the first bottom section X' 1020, the first portions 1112 which were irradiated by the previous beam pulse (as shown in Fig. 12A) are allowed to solidify and crystallize. With respect to the irradiation of the first area 1110 by the second one-fourth portion of the masked beam pulse 164 (i.e., patterned by the first bottom section X' 1020), this second one-fourth portion irradiates second portions 1114 in the first region 1110 such that the second irradiated portions 1114 overlap an area of the first crystallized portions 1112 of the first region 1110. The second portions 1114 are preferably

provided at a vertical offset from the first crystallized portions 1112 of the first region substantially corresponding to the offset 1040 between the slits 1010 of the first top section X 1000 and the slits 1030 of the first bottom section X' 1020. In this manner, the grains provided in the first crystallized portions 1112 would likely grow into the second portions 1114 which overlap them upon cooling and crystallization thereof. In this manner, it is possible to increase the grains size in the first portions 1112 so that the grains therein grow into the second crystallizing portion. Such processing utilizes the principles of the sequentially lateral solidification ("SLS") techniques as described in further detail in the '535 application. In the preferred embodiment of the present invention, the grain growth is even further promoted is the intensity of the masked beam pulse 164 is high enough to at least partially melt the first and second portions 1112, 1114 of the first region 1110 throughout their thickness.

Thereafter, as shown in Figs. 11C and 12C, the sample 170 is continued to be translated in the –X direction relative to the masked beam pulse 164, and the beam pulse is masked by the first top and bottom sections 1000, 1020 and the second top and bottom sections 1050, 1070 of the mask 150'' such that the first one-fourth portion of the beam pulse 164 (i.e., patterned by the first top section X 1000) irradiates a third region 1130 on the first conceptual column 205 of the semiconductor thin film 175, the second one-fourth portion of the masked beam pulse 164 (i.e., patterned by the first bottom section X' 1020) irradiates the second region 1120, and the third one-fourth portion of the masked beam pulse 164 (i.e., patterned by the second top section Y' 1050) irradiates the first region 1110. The fourth one-fourth portion of the masked beam pulse 164 which is patterned by the second bottom section Y' 1070 of the mask 150'' is irradiated away from the semiconductor thin film 175 (i.e., outside of the edge 210'). Thus, first areas 1135 of the third region 1130 are irradiated and situated in a substantially the same manner as the first areas 1122 of the second region 1120. It should again be noted that prior to the irradiation of the second region 1120 by the second one-fourth portion of the masked beam pulse 164 which is patterned by the first bottom section X' 1020, the first portions 1122 which were irradiated by the previous beam pulse (as shown in Fig. 12B) are allowed to solidify and crystallize, and then the second portions 1124 overlap an area of the first

crystallized portions 1122 of the second region 1120, and the lateral growth of the grains from the first portions 1122 into the irradiated and crystallizing second portions 1124 in a substantially similar manner as described above with reference to the first and second portions 1112, 1114 of the first region 1110 of the semiconductor thin film 175.

In addition, third portions 1116 of the first region 1110 which were irradiated by the third one-third portion of the beam pulse 164 masked by the second top section Y 1050 of the mask 150'' are interposed between the first crystallized laterally-grown portions 1112' (created due to the lateral growth of the grains from the first portions 1112 into the second irradiated portions 1114 which overlap the first portions 1112). The third portions 1116 are interposed between the first laterally-grown portions 1112' of the first region 1110.

Further, as shown in Figs. 11D and 12D, the sample 170 is continued to be translated in the –X direction relative to the masked beam pulse 164, and the beam pulse is patterned by the all sections 1000, 1020, 1050, 1070 of the mask 150'' such that the first one-fourth portion of the beam pulse 164 (i.e., patterned by the first top section X 1000) irradiates a fourth region 1140 on the first conceptual column 205 of the semiconductor thin film 175, the second one-fourth portion of the masked beam pulse 164 (i.e., patterned by the first bottom section X' 1020) irradiates the third region 1130, the third one-fourth portion of the masked beam pulse 164 (i.e., patterned by the second top section Y 1050) irradiates the second region 1120, and the fourth one-fourth portion of the masked beam pulse 164 (i.e., patterned by the second bottom section X' 1070) irradiates the first region 1110. The first areas 1142 of the fourth region 1140 are irradiated and situated in a substantially the same manner as the first areas 1132 of the third region 1130, and the third areas 1126 of the second region 1120 are irradiated and situated in a substantially the same manner as the third areas 1116 of the first region 1110. Similarly to the description of the lateral growth prompted by the overlapping of the second irradiated portion 1114 over the first crystallized portion 1112 of the first region 1110, the fourth one-fourth portion of the beam pulse 164 masked by the second bottom section Y' 1070 of the mask 150'' irradiates fourth portions 1118 in the first region 1110 such that the fourth irradiated

portions 1118 overlap an area of the third crystallized portions 1116 of the first region 1110. The second portions 1118 are preferably provided at a vertical offset from the first crystallized portions 1116 of the first region 1110 substantially corresponding to the offset 1090 between the slits 1060 of the second top section Y 1050 and the slits 1080 of the second bottom section Y' 1070. In this manner, the grains provided in the third crystallized portions 1116 would likely grow into the fourth portions 1118 which overlap them upon cooling and crystallization thereof to form third crystallized laterally-grown portions 1116'. Figs. 11E and 12E illustrate that upon the translation of the sample 170 in the –X direction, and irradiating the first conceptual row 205 of the semiconductor thin film 175 by the fourth sequential masked beam pulse 164, the first region 1110 has all portions thereof irradiated, laterally grown and crystallized.

This procedure is repeated in the same manner for the entire first conceptual column 205 of the semiconductor thin film 175 until all regions thereof are irradiated and crystallized substantially in the same manner as provided above for with reference to the first region 810 of the semiconductor thin film 175, and as shown in Figs. 11F, 12F. The conceptual columns 206, 207,... can be irradiated, laterally-grown and crystallized in the same manner, except that when the sample is translated in the +X direction, the first one-fourth portion of the beam pulse 164 is masked by the second bottom section Y' 1070 of the mask 150'', followed by the second one-fourth portion of the beam pulse masked by the second top section Y 1050 of the mask 150'', then followed by third one-fourth portion of the beam pulse masked by the first bottom section X 1020, and finally by the fourth one-fourth portion of the beam pulse masked by the first top section Y 1000 of the mask 150''.

It should be understood that for all exemplary embodiments of the process according to the present invention, the number of pulses irradiating and interposing irradiated arias between previously crystallized areas can be more than four such irradiations for the same regions of the semiconductor thin film 164 as described herein above. In addition, the lateral grain growth can be promoted by more than one portion offset from and overlapping the previously crystallized portions of the regions so as to promote a longer grain growth. Furthermore, it is possible to re-irradiate the portions of the previously irradiated portions by irradiating these already

crystallized areas with corresponding portions of later beam pulses. Indeed, the processes according to the present invention allow the previously crystallized portions of the regions of the semiconductor thin film 175 to be re-irradiated and re-crystallized.

Fig. 10 shows a Fig. 13 is a top view of a fourth exemplary embodiment of the mask 150* according to the present invention which is divided a center region section CR, an east edge section E, a south edge section S, a west edge section W and a north edge section N. In addition, at the corner edge portions thereof, the mask 150* includes a south east edge section SE, a south west edge section SW, a north west edge section NW and a north east edge section NE. The center region section CR includes a set of slits 1210 which can be provided substantially close to one another. The edge sections of the mask 150* each have their respective slits. While the illustration of the edge sections of the mask 150* provided in Fig. 13 may show one slit therein (or even no slits), its should be understood that the edge regions mat have more or less of the slits than shown in Fig. 13. In particular, the east edge section E has slits 1250, the south east edge section has at least one slit 1245, the south edge region S has slits 1240, the south west edge section SW may have no slits or at least one slit 1235, the west edge section W has slits 1230, the north west edge section NW includes at least one slit 1225, the north edge section N has slits 1220 and the north east edge section NE SW may have no slits or at least one slit 1255. each of the edge sections of the masked can have a width of approximately 1 mm, and the width and length of the center regions section CR can be 1 cm x 1 cm. Accordingly, the east, south, west and north edge sections can be sized 1 cm x 1 mm, while the corner edge sections may be sized 1 mm x 1 mm.

The border sections of the mask 150* are provided such that respective set of beamlets being patterned thereby irradiate an edge area of a region of the semiconductor thin film 175 so that they are later interposed between the edge areas of this region such that this edge area is irradiated by the beamlets of another (e.g., next sequential) beam pulse masked by the same mask 150* as well as the adjacent region of such previously irradiated and now crystallized region. In this manner, the border areas of the neighboring regions irradiated by the beamlets of later beam

pulses are dispersed throughout that border areas between the adjacent regions of the semiconductor thin film 175. The details of such positioning and irradiation are provided below.

Figs. 14A-14D show irradiations, by the radiation beam pulse which is masked by the mask 150* of Fig. 13 , and then re-solidifications and crystallizations of the particular portions of the semiconductor film provided on the sample at exemplary sequential stages of the processing according to the process of the present invention. As shown in Fig. 14A, the masked beam pulse 164 patterned by the center region section CR, as well as by the north and east edge sections N, E (and the corner north west edge section NE there between) of the mask 150* so as to impinge and irradiate a first region 1310 on the first conceptual column 205 of the semiconductor thin film sample 170. Therefore, as shown in Figs. 14A, the first region 1310 of the semiconductor thin film is irradiated only by the beamlets of the masked beam pulse 164 corresponding to the slits 1210, 1220, 1250, 1255 of these center region section CR and edge sections of the mask 150*. The masked beam pulse 164 patterned by the south edge section S, the west edge section W, the south east edge section SE, the north west edge section NW and the south west edge section SW of the mask 150* irradiate an area away from the edge of the semiconductor thin film 170. As shown in Fig. 12A, the irradiated first region 1310 of the semiconductor thin film 164 is initially composed of irradiated first areas 1310', 1320', 1350', 1355' which have been irradiated and preferably completely (and at least partially) melted by the beamlets generated by the slits 1210, 1220, 1250, 1255 of the mask 150*. At the edge areas 1320', 1355' and 1350' of the first region 1310, the irradiated portions are provided at a distance from one another, and substantially match the positions and orientations of the slits 1220, 1255 and 1250 of the mask 150*, respectively. The irradiated first portions in the areas 13320', 1355', 1350' of the first region 1310 are provided such that the portions between these irradiated portions can be irradiated with another beam pulse (e.g., a later-applied masked beam pulse) in the unirradiated areas thereof so that the irradiation portions in these border regions by two distinct beam pulses can be dispersed throughout such border regions.

Thereafter, as shown in Fig. 14B, the sample 170 is continued to be translated in the –X direction relative to the masked beam pulse 164, and the beam pulse is masked again by the mask 150*. In the meantime, the irradiated portions of the first region 1310 solidify and crystallize. In this relative position of the sample 170 with respect to the direction of the irradiation of the masked beam pulse 164, the masked beam pulse 164 irradiates a second region 1320 on the first conceptual column 205 of the semiconductor thin film 175. The west border area of the second region 1320 overlaps the east border region VB1 of the first region 1310 composed of the areas 1350', 1355'. In particular, the beam pulse 164 is masked by the west edge section W and the north west edge section NW of the mask 150* such that the beamlets of the masked beam pulses 164 produced by such edge sections of the mask 150* irradiate the unirradiated portions on the border region VB1 that are dispersed between the crystallized portions 1350', 1355' previously irradiated by the masked beam pulse 164 for the first region's 1310 irradiation and then crystallization. Similarly to the irradiation of the first regions 1310, the portions of the masked beam pulse 164 intended for the second region 1320 patterned by the south edge section S, the south west edge section SW and the south east edge section SE of the mask 150* irradiate an area away from the edge of the semiconductor thin film 170 and do not irradiate any portion of the second region 1320.

Thereafter, as shown in Fig. 14C, the sample 170 is continued to be translated in the –X direction relative to the masked beam pulse 164 to irradiate a third region 1330 of the semiconductor thin film 164 (which is adjacent to the second region 1320), and the beam pulse is masked by the mask 150* to generate the beamlet pattern which is substantially the same as the beamlet pattern generated during the irradiation of the second region 1320. Before the irradiation of the third region 1330, the irradiated portions of the second region 1320 solidify and crystallize. Thereafter, the masked beam pulse 164 irradiates the third region 1330 on the first conceptual column 205 of the semiconductor thin film 175. Similarly to the description above with reference to the irradiation of the border region VB1 of the first region 1310, the west border area of the third region 1330 overlaps the east border region VB2 of the second region 1320. Again, the beam pulse 164 is masked by the west edge section

W and the north west edge section NW of the mask 150* such that the beamlets of the masked beam pulses 164 produced by such edge sections of the mask 150* irradiate the unirradiated portions on the border region VB2 that are dispersed between the crystallized portions of the border region VB2 previously irradiated by the masked beam pulse for the second region's 1320 irradiation and then crystallization. Also, the portions of the masked beam pulse 164 intended for the third region 1330 patterned by the south edge section S, the south west edge section SW and the south east edge section SE of the mask 150* irradiate an area away from the edge of the semiconductor thin film 170, and do not irradiate any portion of the third region 1320.

This processing continues until all regions 1310, 1320, 1330, ..., 1390 of the first conceptual column 206 are irradiated and crystallized in substantially the same manner as provided above, with the border regions between such first, second, third, etc. regions 1310, 1320, 1330, ..., 1390 (having crystallized portions that have been irradiated by separate and distinct masked beam pulses 164) being dispersed between one another. The conceptual columns 206, 207, ... can be irradiated, laterally-grown and crystallized in the same manner, except that when the sample is translated in the +X direction, the beamlets generated by the west edge section W of the mask 150* lead the irradiation of the regions of the second conceptual column 206 before the irradiation by all beamlets patterned by the other sections of the mask 150*.

In particular, as shown in Fig. 14D, the first region 1410 of the second conceptual column 206 is irradiated to have the irradiated portions thereof substantially match the irradiated portions of the last region 1390 of the first conceptual column 205, but provided at an offset from such last region 1390 which approximately equals to slightly less than the distance between the first conceptual column 205 and the second conceptual column. In addition, the beamlets of the beam pulse 164 being patterned by the south edge section S and the south west edge section SW of the mask 150* irradiate the unirradiated portions on a north horizontal border region HB1 between the last region 1390 of the first conceptual column 205 that it has with the first region 1410 of the second conceptual column. The portions in this border region HB1 irradiated by the beamlets generated by the south edge section S

and the south west section SW of the mask 150* are dispersed between the crystallized portions of the horizontal border region HB1 that were previously irradiated by the beamlets generated by the north edge section N and the north west edge section NW of the mask 150* which are crystallized. This processing of the regions in the second conceptual column 206 is continued until the portions of all regions in this column 206 are irradiated and crystallized. The processing of the third conceptual column 207 and other conceptual columns continues until the processing of the entire semiconductor thin film 164 (or a selected portion thereof) is completed.

As shown in Figs. 4A-4D, the border regions between the irradiated regions include portions of the crystallized portions therein which have been irradiated by separate and distinct beam pulses that are likely to have differing fluences. These irradiated and then crystallized portions are dispersed throughout the edge regions so as to have portions irradiated by one beam pulse interdisposed between the portions irradiated by another beam pulse. Also, turning back to Fig. 14D, the portion in the north west corner of the last region 1390 of the first conceptual column 205 is irradiated four times. This is because the neighboring last and next to last regions 1380, 1390 of the first conceptual column 205 of the semiconductor thin film 164 each irradiate this area, and the first and second regions 1410, 1420 of the second conceptual column 206 irradiate this portion as well. This is due to the fact that this north west portion is provided on the vertical border VB8 and the horizontal border HB1.

This fact is evident in Fig. 15 which illustrates that substantially all corner portions of the irradiated regions (i.e., irradiated by the respective corner sections of the mask 150*) are impinged by the respective beamlets at least four times during the processing of the semiconductor thin film 164. The edge areas irradiated by the beamlets patterned by the north, east, west and south edge sections N, E, W, S of the mask 150* are processed two times due such areas being either on the horizontal or vertical edge regions between the adjacent regions. The portions of the regions irradiated by the center region section of the mask 150* is irradiated once, since irradiation and crystallization of the center region does not need to be intermixed with the irradiation and crystallization of the neighboring regions. This is

because what is achieved by the exemplary embodiment of the present invention is that the contrast between the border regions (and not the center regions) is reduced by interleaving the areas irradiated by the separate and distinct beam pulse having differing fluence levels in these border regions. This is done by placing the TFT devices in such specifically arranged and interleaved areas in the border regions (as well as in the center areas of the regions) so that sharp contrast that may be generated by such TFT devices is reduced. In particular, the intensity distribution on the border regions varies in a preferably smooth and continuous manner so that there is no abrupt variation encountered between the adjacent regions. It should be understood that the portion of the regions irradiated by the portions of the beam pulse 164 masked by the center region section CR of the mask 150* can be reduced or even eliminated so as to smooth the transitions between the border regions without taking consideration of any such center region between the border regions. For example, the following irradiations of the regions irradiated by the beam pulse 164 patterned by the corresponding sections of the mask 150* upon the removal of such center region:

4 Irradiations (NW)	4 Irradiations (NE)
4 Irradiations (SW)	4 Irradiations (SE)

and

4 Irradiations (NW)	4 Irradiations (NE)
2 Irradiations (W)	2 Irradiations (E)
4 Irradiations (SW)	4 Irradiations (SE)

Fig. 16 shows a flow diagram representing a first exemplary processing procedure of the present invention under at least a partial control of a computing arrangement of Fig. 1A which uses the techniques of the present invention of Figs. 4A-4H, 5A-5H, 8A-8H, 11A-11F and 12A-12F. In step 2000, the hardware components of the system of Fig. 1A, such as the beam source 110, the energy beam modulator 120, and the beam attenuator and shutter 130 are first initialized at least in part by the computing arrangement 100. The sample 170 is loaded onto the sample translation stage 180 in step 2005. It should be noted that such loading may be performed either manually or automatically using known sample loading apparatus under the control of the computing arrangement 100. Next, the sample translation stage 180 is moved, preferably under the control of the computing arrangement 100, to an initial position in step 2010. Various other optical components of the system are adjusted and/or aligned either manually or under the control of the computing arrangement 100 for a proper focus and alignment in step 2015, if necessary. In step 2020, the irradiation/laser beam 111 is stabilized at a predetermined pulse energy level, pulse duration and repetition rate. In step 2024, it is preferably determined whether each beam pulse 164 has sufficient energy to fully melt the irradiated portions of the semiconductor thin film 175 without over-melting them. If that is not the case, the attenuation of the beam 111 is adjusted by the beams source 110 under the control of the computing arrangement 100 in step 2025, and step 2024 is executed again to determine if the there is sufficient energy to melt the portions of the semiconductor thin film.

In step 2027, the sample 170 is positioned to point the beam pulse 164 to impinge the first column of the semiconductor thin film. Then, in step 2030, the portions of the semiconductor thin film 175 are irradiated and at least partially melted using a masked intensity pattern (e.g., using the masks 150, 150', 150''). Thereafter, the irradiated portions of the semiconductor thin film 175 are allowed to solidify and crystallize. In step 2035, it is determined whether the irradiation for the current conceptual column by the beam pulse has been completed. If no, in step 2040, the next region of the same column of the sample 170 is irradiated with the beamlet pattern substantially corresponding to the beam pattern which was used to irradiate

the previous region. In addition, the previously irradiated and crystallized region of the semiconductor thin film 175 is irradiated using the current beam pulse 164 which has a pattern such that the beamlets of the current masked beam pulse irradiate the unirradiated portions within the previously processed region (either adjacent or otherwise). The newly irradiated portions in the previously processed region are interposed between the crystallized areas.

However, if in step 2035, it is determined that the irradiation and crystallization of the current conceptual column is completed, then it is determined in step 2045 whether there are any further conceptual columns of the sample 170 to be processed. If so, the process continues to step 2050 in which the sample 170 is translated to that the beam pulse 164 is pointed to the next conceptual column to be processed according to the present invention. Otherwise, in step 2055, the exemplary processing has been completed for the sample 170, and the hardware components and the beam 111 of the system shown in Fig. 1A can be shut off, and the process is terminated. In another variation of the embodiment of the process according to the present invention, the

Fig. 17 shows a flow diagram representing a second exemplary processing procedure of the present invention under at least a partial control of a computing arrangement of Fig. 1A using the techniques of the present invention of Figs. 14A-14D in which the sections of the border areas of the adjacent irradiated regions are dispersed throughout such border regions. Steps 2100-2135 of this exemplary procedure are substantially the same as the steps 2000-2035 of the procedure of Fig. 16, and thus shall not be described herein in further detail. In step 2140, the next region of the same column of the sample 170 is irradiated with the beamlet pattern that can substantially correspond to the beam pattern which was used to irradiate the previous region. In addition, the border region of the previously irradiated region is overlapped with the irradiations of the next pattern of beamlets of the subsequent beam pulse 164. This pattern is arranged such that the beamlets of the current masked beam pulse irradiate the unirradiated portions within the border area of the previously processed adjacent region. The newly irradiated portions in the previously processed region are interposed in the border regions of the previous and

adjacent regions, between the previously crystallized areas of the previously irradiated region the crystallized areas. According to this exemplary embodiment of the present invention, all borders of the adjacent regions are overlapped by the subsequent or other irradiations of the masked beam pulse 164. The processing of this second exemplary embodiment in steps 2145-2155 continues in substantially the same manner as the processing of steps 2045-2055 described above with reference to Fig. 16.

Furthermore, the irradiation of the regions of the semiconductor thin film 175 can be performed (e.g., initiated by the processor) when the beam pulses 164 reach particular locations on the sample 170. These locations can be pre-assigned by the computing arrangement 100 and stored in the storage device thereof. Thus, the beam source 110 can be fired upon the sample 170 reaching these locations with respect to the beam pulses 164.

The foregoing merely illustrates the principles of the invention. Various modifications and alterations to the described embodiments will be apparent to those skilled in the art in view of the teachings herein. For example, while the above embodiment has been described with respect to at least partial lateral solidification and crystallization of the semiconductor thin film, it may apply to other materials processing techniques, such as micro-machining, photo-ablation, and micro-patterning techniques, including those described in International patent application no. PCT/US01/12799 and U.S. patent application serial nos. 09/390,535, 09/390,537 and 09/526,585, the entire disclosures of which are incorporated herein by reference. The various mask patterns and intensity beam patterns described in the above-referenced patent application can also be utilized with the process and system of the present invention. It will thus be appreciated that those skilled in the art will be able to devise numerous systems and methods which, although not explicitly shown or described herein, embody the principles of the invention and are thus within the spirit and scope of the present invention.

What Is Claimed Is:

1. A method for processing at least one section of a thin film sample on a substrate, comprising the steps of:

(a) controlling an irradiation beam generator to emit successive irradiation beam pulses at a predetermined repetition rate;

(b) masking each of the irradiation beam pulses to define a first plurality of beamlets and a second plurality of beamlets, the first and second plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to at least partially melt irradiated portions of the at least one section of the film sample;

(c) irradiating a particular portion of the at least one section of the film sample with the first beamlets of a first pulse of the irradiated beam pulses to melt first areas of the particular portion, the first areas being at least partially melted, leaving first unirradiated regions between respective adjacent ones of the first areas and being allowed to resolidify and crystallize; and

(d) after step (c), irradiating the particular portion with the second beamlets of a second pulse of the irradiated beam pulses to melt second areas of the particular portion, the second areas being at least partially melted, leaving second unirradiated regions between respective adjacent ones of the second areas and being allowed to resolidify and crystallize,

wherein the first irradiated and re-solidified areas and the second irradiated and resolidified areas are intermingled with one another within the at least one section of the film sample, and

wherein the first areas correspond to first pixels, and the second areas correspond to second pixels.

2. The method according to claim 1, wherein respective positions of the first pixels are different than respective positions of the second pixels.

3. The method according to claim 1, wherein a location of at least one of the second areas is substantially the same as a location of at least one of the first unirradiated areas.

4. The method according to claim 3, wherein the first unirradiated areas have substantially the same location as the second areas, and wherein the second unirradiated areas have substantially the same location as the first areas.

5. The method according to claim 4, wherein the first and second resolidified areas form an entire cross-section of the at least one section of the film sample.

6. The method according to claim 3, wherein the locations of the first and second areas are non-uniform.

7. The method according to claim 1, wherein edges of the second irradiated and re-solidified areas are provided at a distance from the first re-solidified areas.

8. The method according to claim 1, wherein the first beamlets have a first energy density, wherein the second beamlets have a second energy density, and wherein the first energy density is different from the second energy density.

9. The method according to claim 1, wherein the masked irradiation beam pulses further include a third plurality of beamlets which are provided for impinging the film sample and which have an intensity that is sufficient to at least partially melt irradiated portions of the at least one section of the film sample, and further comprising the step of:

(e) after step (d), irradiating the particular portion with the third beamlets to melt third areas of the particular portion, the third areas being at least partially melted to leave third unirradiated regions between respective adjacent ones of the third areas and being allowed to resolidify and crystallize.

10. The method according to claim 9, wherein the third areas correspond to the third pixels, and wherein respective positions of the first and second pixels are different than respective positions of the third pixels.

11. The method according to claim 9, wherein a location of at least one of the first and second areas is substantially the same as a location of at least one of the third unirradiated areas.

12. The method according to claim 11, wherein the location of the first and second areas are different that the location of the third areas.

13. The method according to claim 12, wherein at least one of the first and second unirradiated areas have substantially the same locations as the third areas, and wherein the third unirradiated areas have substantially the same locations as at least one of the first and second areas.

14. The method according to claim 13, wherein the first, second and third resolidified areas form an entire cross-section of the at least one section of the film sample.

15. The method according to claim 9, wherein edges of the first and second re-solidified areas are provided at a distance from the third re-solidified areas.

16. The method according to claim 9, wherein the first beamlets have a first energy density, wherein the second beamlets have a second energy density, wherein the third beamlets have a third energy density, and wherein the third energy density is different from at least one of the first energy density and the second energy density.

17. The method according to claim 1, where the second beam pulse immediately follows the first beam pulse, wherein the first areas are irradiated with the first beamlets when the film sample is provided at a first position of with respect to the

irradiation beam pulses, wherein the second areas are irradiated with the second beamlets when the film sample is provided at a second position with respect to the irradiation beam pulses, the second position being closer to a center of the at least one section of the film sample than the second position.

18. The method according to claim 17, further comprising the step of:

(f) after step (c) and before step (d), translating the film sample relative to the irradiation beam pulses so that the impingement by the first beamlet of the film sample moves from the first position to the second position.

19. The method according to claim 1, wherein, in step (c), the first areas are fully melted, and wherein in step (d), the second areas are fully melted throughout their entire thickness.

20. The method according to claim 1, further comprising the steps of:

(g) translating the film sample so that the a further portion of the film sample is provided for irradiation by the first and second beamlets, the further portion being substantially adjacent to the particular portion of the film sample; and

(h) repeating steps (c) and (d) on for the further portion of the film sample,

wherein a first edge of the further portion of the film sample overlaps a second edge of the particular portion of the film sample, and

wherein the re-solidified areas in the first edge of the further portion are intermingled with the re-solidified areas of the particular portion so as to prevent an overlap thereof.

21. The method according to claim 1, wherein at least one of the first and second areas are configured to situate therein at least one thin-film transistor.

22. A method for processing at least one section of a thin film sample on a substrate, comprising the steps of:

(a) controlling an irradiation beam generator to emit successive irradiation beam pulses at a predetermined repetition rate;

(b) masking each of the irradiation beam pulses to define a plurality of beamlets, the plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to at least partially melt irradiated portions of the at least one section of the film sample;

(c) at a first location of the film sample with respect to the irradiation beam pulses, irradiating a first portion of the at least one section of the film sample with the beamlets of a first pulse of the irradiated beam pulses to at least partially melt first areas of the at least one section, the first areas leaving first unirradiated regions between respective adjacent ones of the first areas on at least one first edge thereof, and being allowed to resolidify and crystallize; and

(d) after step (c), translating the film sample from the first location to a second location with respect to the irradiation beam pulses;

(e) after step (d) and at the second location, irradiating a second portion of the at least one section of the film sample with the beamlets of a second pulse of the irradiated beam pulses to at least partially melt second areas of the at least one section, the second areas leaving second unirradiated regions between respective adjacent ones of the second areas on at least one second edge thereof, and being allowed to resolidify and crystallize,

wherein the at least one first edge of the first portion of the at least one section of the film sample is overlapped by the at least one second edge of the second portion of the at least one section of the film sample, and wherein the first re-solidified areas and the second re-solidified areas are intermingled with one another within the at least one first edge and the at least one second edge.

23. The method according to claim 22, wherein the overlapping of the first and second resolidied areas collectively smooth a spatial distribution of a border between the first portion and the second portion of the at least one section of the film sample.

24. The method according to claim 23, wherein due to the border between the first and second portions being smoothed, a visible contrast between the first portion and the second portion of the at least one section of the film sample.

25. The method according to claim 24, the combined densities of the at least one first edge and the at least one second edge provide an adequate pixel density at the border between the first and second portions of the at least one section of the film sample.

26. The method according to claim 22,

wherein, in step (e), the second areas further leave further unirradiated regions in the second portion between respective adjacent ones of the second areas on at least one further edge thereof, and being allowed to resolidify and crystallize, and

wherein the at least one further edge is provided adjacent to the at least one second edge.

27. The method according to claim 26, wherein the at least one section is a first row of the thin film sample, wherein the first row is irradiated by the beamlets of the first and second beam pulses when the film sample is translated in a first direction with respect to the first and second beam pulses, and further comprising the steps of:

(f) positioning the film sample for irradiating a further section of the film sample, the further section being a second row of the film sample; and

(g) at a third location of the film sample with respect to the irradiation beam pulses, irradiating a first portion of the further section of the film sample with the beamlets of a third pulse of the irradiated beam pulses to at least partially melt third areas of the further section, the third areas of the further section leaving third unirradiated regions between respective adjacent ones of the third areas on at least one third edge thereof, and being allowed to resolidify and crystallize,

wherein the at least one further edge of the second portion of the at least one section of the film sample is overlapped by the at least one third edge of the second portion of the further section of the film sample, and wherein the further re-solidified

areas and the third re-solidified areas are intermingled with one another within the at least one further edge and the at least one third edge.

28. The method according to claim 22, wherein, in step (c), the first areas include additional unirradiated regions between respective adjacent ones of the first areas which are away from the at least one edge, and further comprising the steps of

(h) after step (c) and before step (d), irradiating the first portion of the at least one section of the film sample with further beamlets of the first pulse of the irradiated beam pulses to melt further areas of the first portion, the further areas being at least partially melted, leaving further unirradiated regions between respective adjacent ones of the further areas and being allowed to resolidify and crystallize,

wherein the first re-solidified areas and the further re-solidified areas are intermingled with one another within the first portion of the film sample.

29. The method according to claim 28, wherein a location of at least one of the further areas is substantially the same as a location of at least one of the additional unirradiated areas.

30. The method according to claim 29, wherein the additional unirradiated areas have substantially the same location as the further areas, and wherein the further unirradiated areas have substantially the same location as the first areas.

31. The method according to claim 30, wherein the first and further resolidified areas form an entire cross-section of the first portion of the at least one section of the film sample.

32. The method according to claim 22, wherein the at least one first edge and the at least one second edge are overlapped to form an edge area the entire surface of which is crystallized.

33. A system for processing at least one section of a thin film sample on a substrate, comprising:

a processing arrangement, which when executing a computer program, is configured to perform the following steps:

(a) controlling an irradiation beam generator to emit successive irradiation beam pulses at a predetermined repetition rate;

(b) masking each of the irradiation beam pulses to define a first plurality of beamlets and a second plurality of beamlets, the first and second plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to at least partially melt irradiated portions of the at least one section of the film sample;

(c) irradiating a particular portion of the at least one section of the film sample with the first beamlets of a first pulse of the irradiated beam pulses to melt first areas of the particular portion, the first areas being at least partially melted, leaving first unirradiated regions between respective adjacent ones of the first areas and being allowed to resolidify and crystallize; and

(d) after step (c), irradiating the particular portion with the second beamlets of a second pulse of the irradiated beam pulses to melt second areas of the particular portion, the second areas being at least partially melted, leaving second unirradiated regions between respective adjacent ones of the second areas and being allowed to resolidify and crystallize,

wherein the first re-solidified areas and the second re-solidified areas are intermingled with one another within the at least one section of the film sample, and

wherein the first areas correspond to first pixels, and the second areas correspond to second pixels.

34. The system according to claim 33, wherein respective positions of the first pixels are different than respective positions of the second pixels.

35. The system according to claim 33, wherein a location of at least one of the second areas is substantially the same as a location of at least one of the first unirradiated areas.

36. The system according to claim 35, wherein the first unirradiated areas have substantially the same location as the second areas, and wherein the second unirradiated areas have substantially the same location as the first areas.

37. The system according to claim 35, wherein the first and second resolidified areas form an entire cross-section of the at least one section of the film sample.

38. The system according to claim 35, wherein the locations of the first and second areas are non-uniform.

39. The system according to claim 33, wherein edges of the second re-solidified areas are provided at a distance from the first re-solidified areas.

40. The system according to claim 33, wherein the first beamlets have a first energy density, wherein the second beamlets have a second energy density, and wherein the first energy density is different from the second energy density.

41. The system according to claim 33, wherein the masked irradiation beam pulses further include a third plurality of beamlets which are provided for impinging the film sample and which have an intensity that is sufficient to at least partially melt irradiated portions of the at least one section of the film sample, and wherein the processing arrangement, when executing the computer program, is further configured to perform the step of:

(e) after step (d), irradiating the particular portion with the third beamlets to melt third areas of the particular portion, the third areas being at least partially melted leaving third unirradiated regions between

respective adjacent ones of the third areas and being allowed to resolidify and crystallize.

42. The system according to claim 41, wherein the third areas correspond to the third pixels, and wherein respective positions of the first and second pixels are different than respective positions of the third pixels.

43. The system according to claim 41, wherein a location of at least one of the first and second areas is substantially the same as a location of at least one of the third unirradiated areas.

44. The system according to claim 43, wherein the location of the first and second areas are different that the location of the third areas.

45. The system according to claim 44, wherein at least one of the first and second unirradiated areas have substantially the same locations as the third areas, and wherein the third unirradiated areas have substantially the same locations as at least one of the first and second areas.

46. The system according to claim 45, wherein the first, second and third resolidified areas form an entire cross-section of the at least one section of the film sample.

47. The system according to claim 41, wherein edges of the first and second re-solidified areas are provided at a distance from the third re-solidified areas.

48. The system according to claim 41, wherein the first beamlets have a first energy density, wherein the second beamlets have a second energy density, wherein the third beamlets have a third energy density, and wherein the third energy density is different from at least one of the first energy density and the second energy density.

49. The system according to claim 33, where the second beam pulse immediately follows the first beam pulse, wherein the first areas are irradiated with the first beamlets when the film sample is provided at a first position of with respect to the irradiation beam pulses, wherein the second areas are irradiated with the second beamlets when the film sample is provided at a second position with respect to the irradiation beam pulses, the second position being closer to a center of the at least one section of the film sample than the second position.

50. The system according to claim 49, wherein the processing arrangement, when executing the computer program, is further configured to perform the step of:

(f) after step (c) and before step (d), translating the film sample relative to the irradiation beam pulses so that the impingement by the first beamlet of the film sample moves from the first position to the second position.

51. The system according to claim 33, wherein, in step (c), the first areas are fully melted throughout their entire thickness, and wherein in step (d), the second areas are fully melted throughout their entire thickness.

52. The system according to claim 33, wherein the processing arrangement, when executing the computer program, is further configured to perform the steps of:

(g) translating the film sample so that the a further portion of the film sample is provided for irradiation by the first and second beamlets, the further portion being substantially adjacent to the particular portion of the film sample; and

(h) repeating steps (c) and (d) on for the further portion of the film sample,

wherein a first edge of the further portion of the film sample overlaps a second edge of the particular portion of the film sample, and

wherein the re-solidified areas in the first edge of the further portion are intermingled with the re-solidified areas of the particular portion so as to prevent an overlap thereof.

53. A system for processing at least one section of a thin film sample on a substrate, comprising:

a processing arrangement, which when executing a computer program, is configured to perform the following steps:

(a) controlling an irradiation beam generator to emit successive irradiation beam pulses at a predetermined repetition rate;

(b) masking each of the irradiation beam pulses to define a plurality of beamlets, the plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to at least partially melt irradiated portions of the at least one section of the film sample;

(c) at a first location of the film sample with respect to the irradiation beam pulses, irradiating a first portion of the at least one section of the film sample with the beamlets of a first pulse of the irradiated beam pulses to at least partially melt first areas of the at least one section, the first areas leaving first unirradiated regions between respective adjacent ones of the first areas on at least one first edge thereof, and being allowed to resolidify and crystallize;

(d) after step (c), translating the film sample from the first location to a second location with respect to the irradiation beam pulses; and

(e) after step (d) and at the second location, irradiating a second portion of the at least one section of the film sample with the beamlets of a second pulse of the irradiated beam pulses to at least partially melt second areas of the at least one section, the second areas leaving second unirradiated regions between respective adjacent ones of the second areas on at least one second edge thereof, and being allowed to resolidify and crystallize,

wherein the at least one first edge of the first portion of the at least one section of the film sample is overlapped by the at least one second edge of the second portion of the at least one section of the film sample, and wherein the first re-solidified areas

and the second re-solidified areas are intermingled with one another within the at least one first edge and the at least one second edge.

54. The system according to claim 53, wherein the overlapping of the first and second resolidied areas collectively smooth a spatial distribution of a border between the first portion and the second portion of the at least one section of the film sample.

55. The system according to claim 54, wherein due to the border between the first and second portions being smoothed, a visible contrast between the first portion and the second portion of the at least one section of the film sample.

56. The system according to claim 55, wherein the combined densities of the at least one first edge and the at least one second edge provide an adequate pixel density at the border between the first and second portions of the at least one section of the film sample.

57. The system according to claim 53,

wherein, in step (e), the second areas further leave further unirradiated regions in the second portion between respective adjacent ones of the second areas on at least one further edge thereof, and being allowed to resolidify and crystallize, and

wherein the at least one further edge is provided adjacent to the at least one second edge.

58. The system according to claim 57, wherein the at least one section is a first row of the thin film sample, wherein the first row is irradiated by the beamlets of the first and second beam pulses when the film sample is translated in a first direction with respect to the first and second beam pulses, wherein the processing arrangement, when executing the computer program, is further configured to perform the steps of:

(f) positioning the film sample for irradiating a further section of the film sample, the further section being a second row of the film sample; and

(g) at a third location of the film sample with respect to the irradiation beam pulses, irradiating a first portion of the further section of the film sample with the beamlets of a third pulse of the irradiated beam pulses to at least partially melt third areas of the further section, the third areas of the further section leaving third unirradiated regions between respective adjacent ones of the third areas on at least one third edge thereof, and being allowed to resolidify and crystallize,

wherein the at least one further edge of the second portion of the at least one section of the film sample is overlapped by the at least one third edge of the second portion of the further section of the film sample, and

wherein the further re-solidified areas and the third re-solidified areas are intermingled with one another within the at least one further edge and the at least one third edge.

59. The system according to claim 53, wherein, in step (c), the first areas include additional unirradiated regions between respective adjacent ones of the first areas which are away from the at least one edge, wherein the processing arrangement, when executing the computer program, is further configured to perform the step of:

(h) after step (c) and before step (d), irradiating the first portion of the at least one section of the film sample with further beamlets of the first pulse of the irradiated beam pulses to melt further areas of the first portion, the further areas being at least partially melted, leaving further unirradiated regions between respective adjacent ones of the further areas and being allowed to resolidify and crystallize, and

wherein the first re-solidified areas and the further re-solidified areas are intermingled with one another within the first portion of the film sample.

60. The system according to claim 59, wherein a location of at least one of the further areas is substantially the same as a location of at least one of the additional unirradiated areas.

61. The system according to claim 60, wherein the additional unirradiated areas have substantially the same location as the further areas, and wherein the further unirradiated areas have substantially the same location as the first areas.

62. The system according to claim 61, wherein the first and further resolidified areas form an entire cross-section of the first portion of the at least one section of the film sample.

63. The system according to claim 53, wherein the at least one first edge and the at least one second edge are overlapped to form an edge area the entire surface of which is crystallized.

64. A method for processing at least one section of a thin film sample on a substrate, comprising the steps of:

(a) controlling an irradiation beam generator to emit successive irradiation beam pulses at a predetermined repetition rate;

(b) masking each of the irradiation beam pulses to define a first plurality of beamlets and a second plurality of beamlets, the first and second plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to at least partially melt irradiated portions of the at least one section of the film sample;

(c) irradiating a particular portion of the at least one section of the film sample with the first beamlets of a first pulse of the irradiated beam pulses to melt and crystallize first areas of the particular portion; and

(d) after step (c), irradiating the particular portion with the second beamlets of a second pulse of the irradiated beam pulses to melt and crystallize second areas of the particular portion,

wherein the first irradiated areas and the second irradiated areas are intermingled with one another within the at least one section of the film sample,

wherein a pulse irradiation history of the first irradiated areas is different than a pulse history of the second irradiated areas, and

wherein the first areas correspond to first pixels, and the second areas correspond to second pixels.

65. A method for processing at least one section of a thin film sample on a substrate, comprising the steps of:

(a) controlling an irradiation beam generator to emit successive irradiation beam pulses at a predetermined repetition rate;

(b) masking each of the irradiation beam pulses to define a plurality of beamlets, the plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to at least partially melt irradiated portions of the at least one section of the film sample;

(c) at a first location of the film sample with respect to the irradiation beam pulses, irradiating a first portion of the at least one section of the film sample with the beamlets of a first pulse of the irradiated beam pulses to at least partially melt and crystallize first areas of the at least one section; and

(d) after step (c), translating the film sample from the first location to a second location with respect to the irradiation beam pulses;

(e) after step (d) and at the second location, irradiating a second portion of the at least one section of the film sample with the beamlets of a second pulse of the irradiated beam pulses to at least partially melt and crystallize second areas of the at least one section,

wherein the at least one first edge of the first portion of the at least one section of the film sample is overlapped by the at least one second edge of the second portion of the at least one section of the film sample,

wherein a pulse irradiation history of the first irradiated areas is different than a pulse history of the second irradiated areas, and

wherein the first irradiated areas and the second irradiated areas are intermingled with one another within the at least one first edge and the at least one second edge.

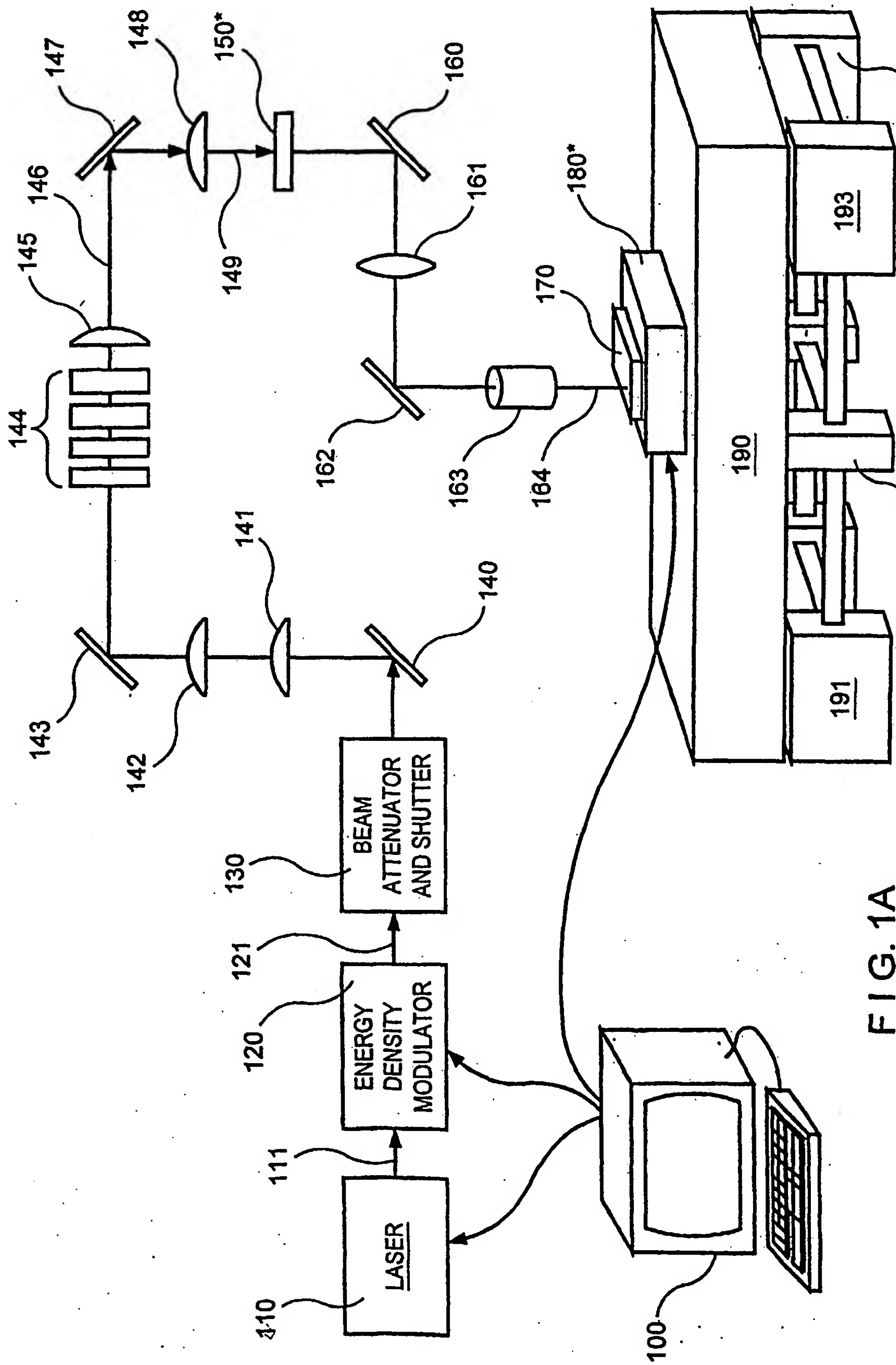

LASER
ENERGY DENSITY MODULATOR
BEAM ATTENUATOR AND SHUTTER
110
111
120
121
130
140
141
142
143
144
145
146
147
148
149
150*
160
161
162
163
164
170
180*
190
191
192
193
194
100

FIG. 1A

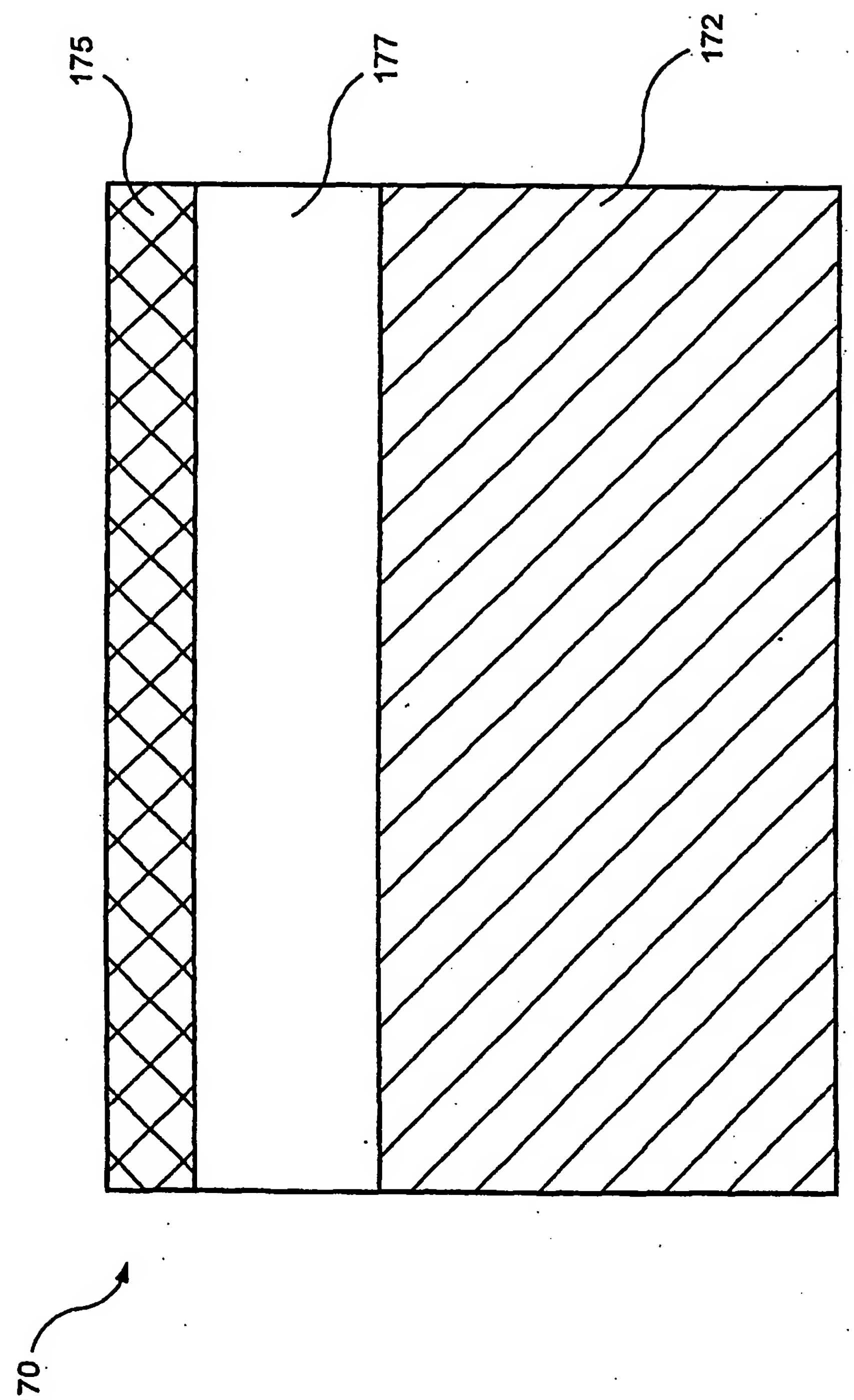


FIG. 1B

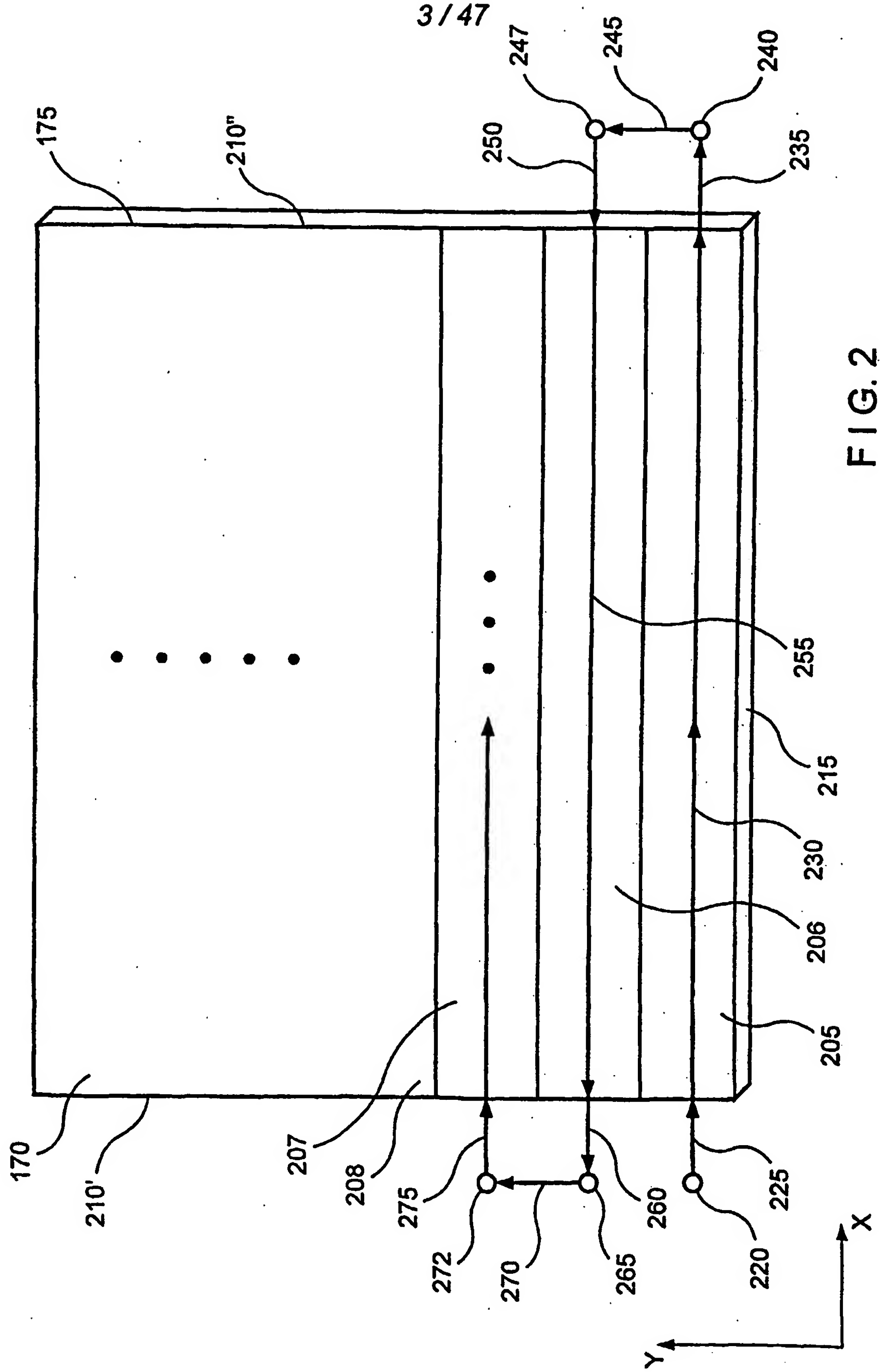

175
210"
250
247
245
240
235
255
215
230
206
205
170
210'
207
208
275
272
270
265
260
220
225
X
Y

FIG. 2

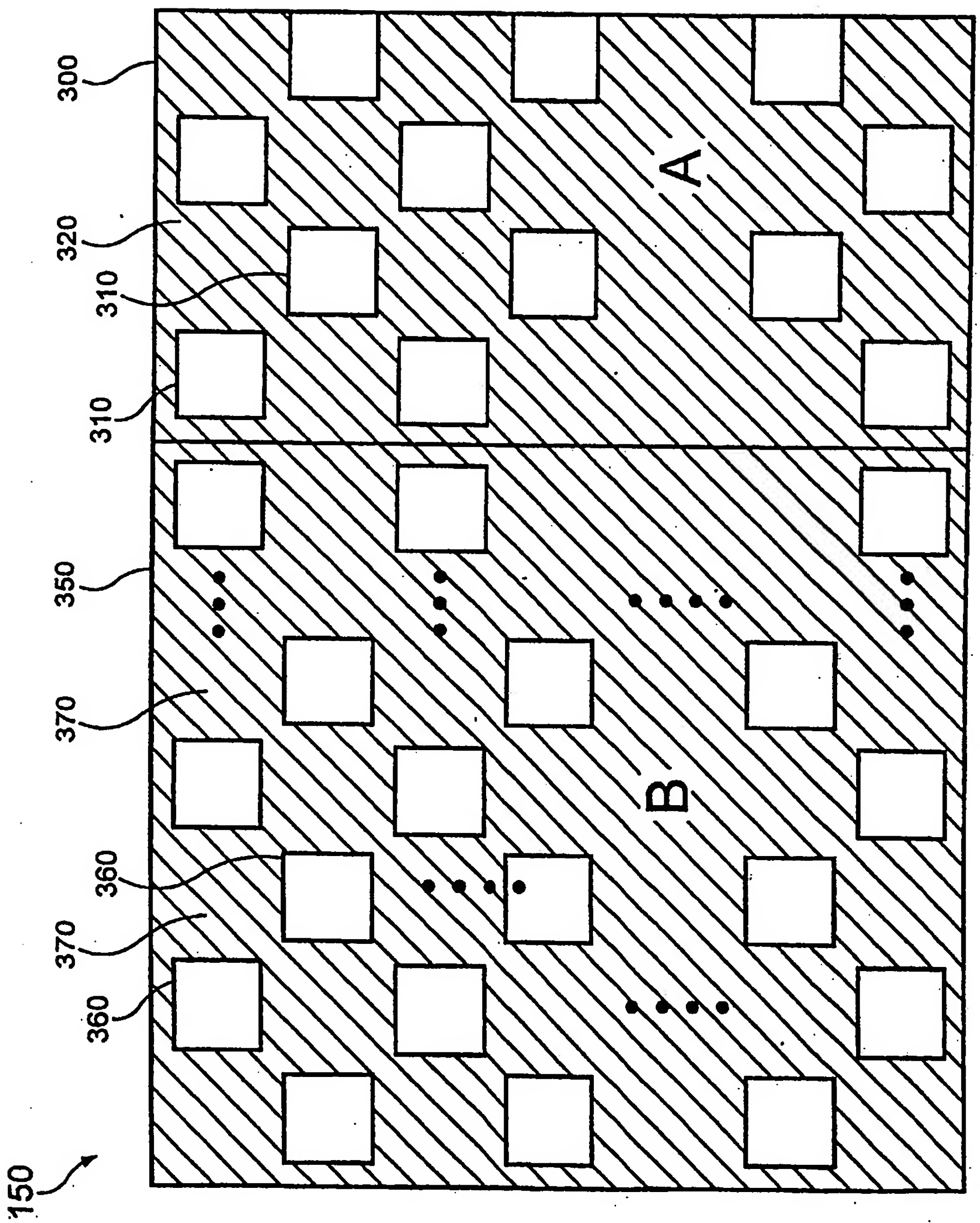
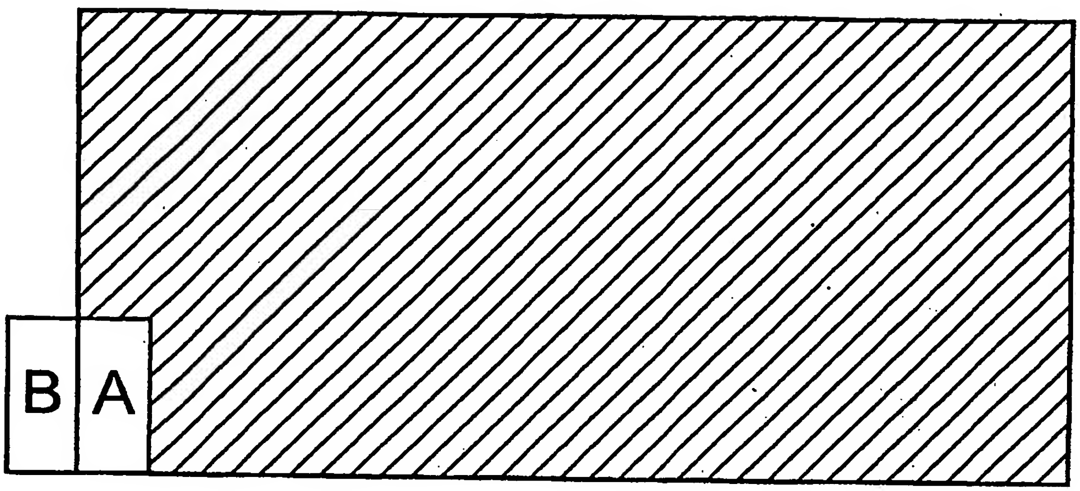
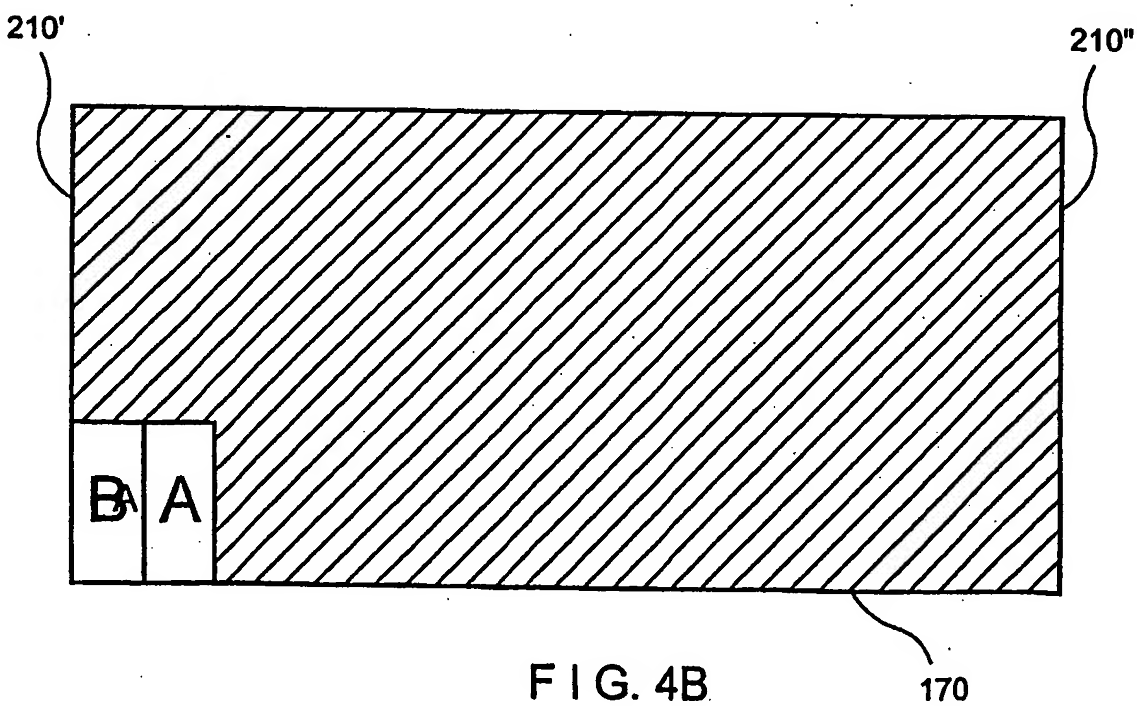


FIG. 3



F I G. 4A



F I G. 4B

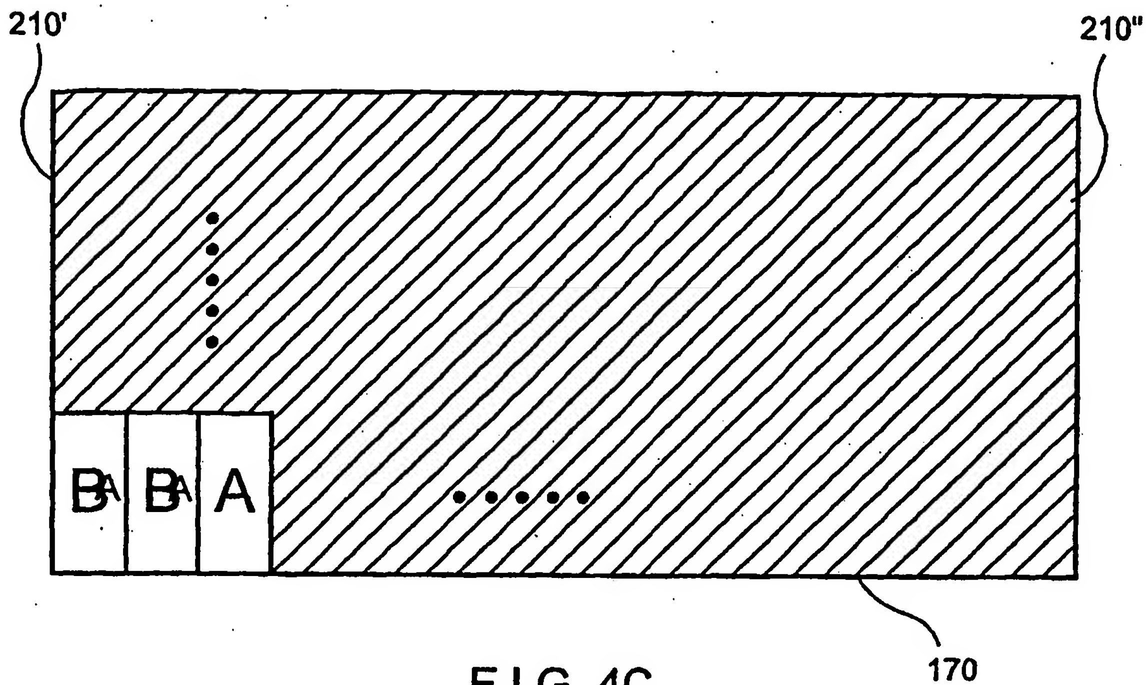


FIG. 4C

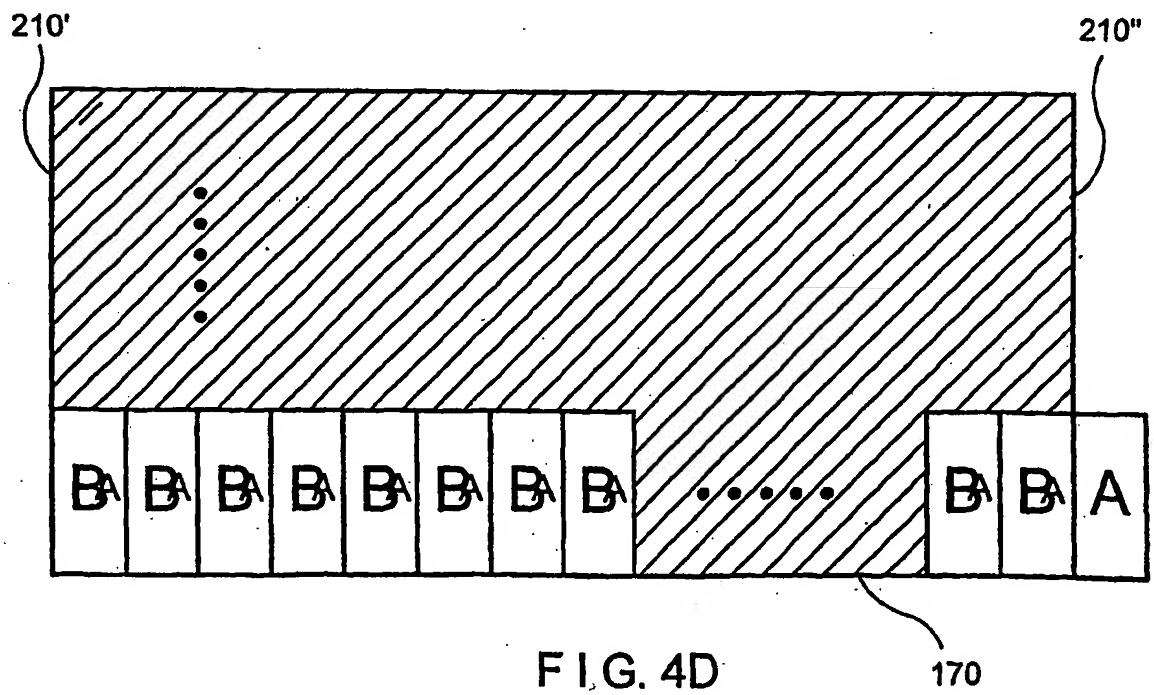
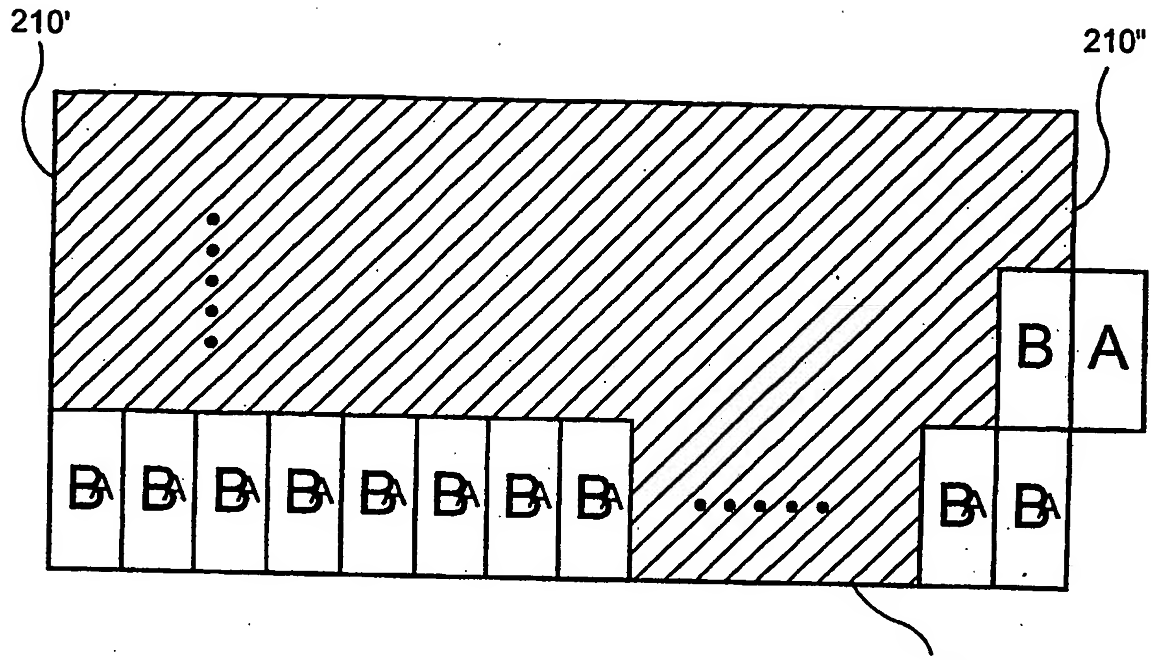
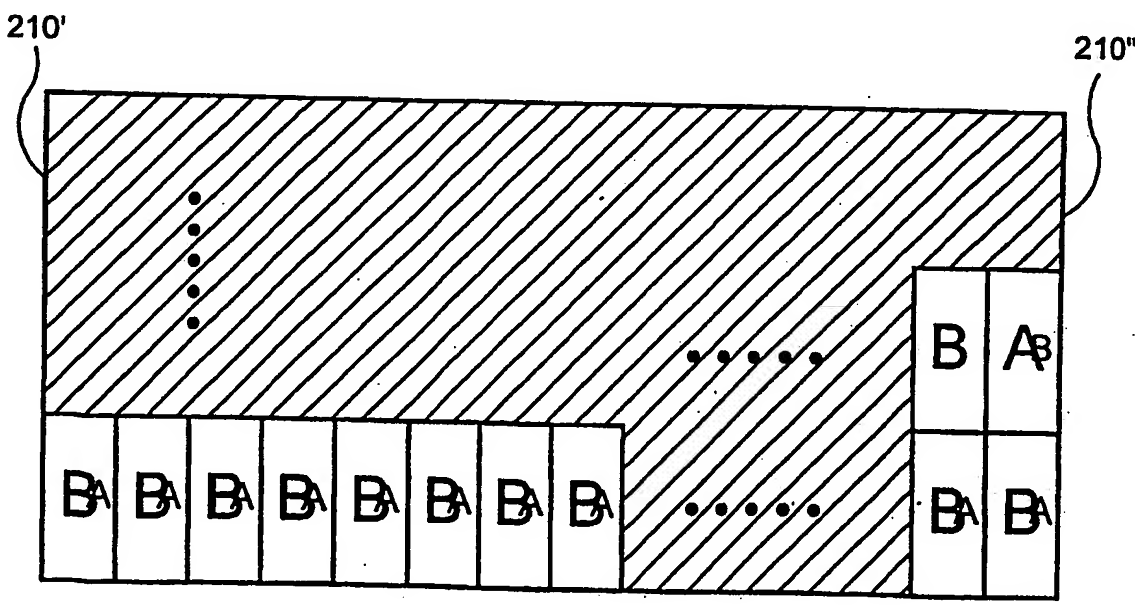


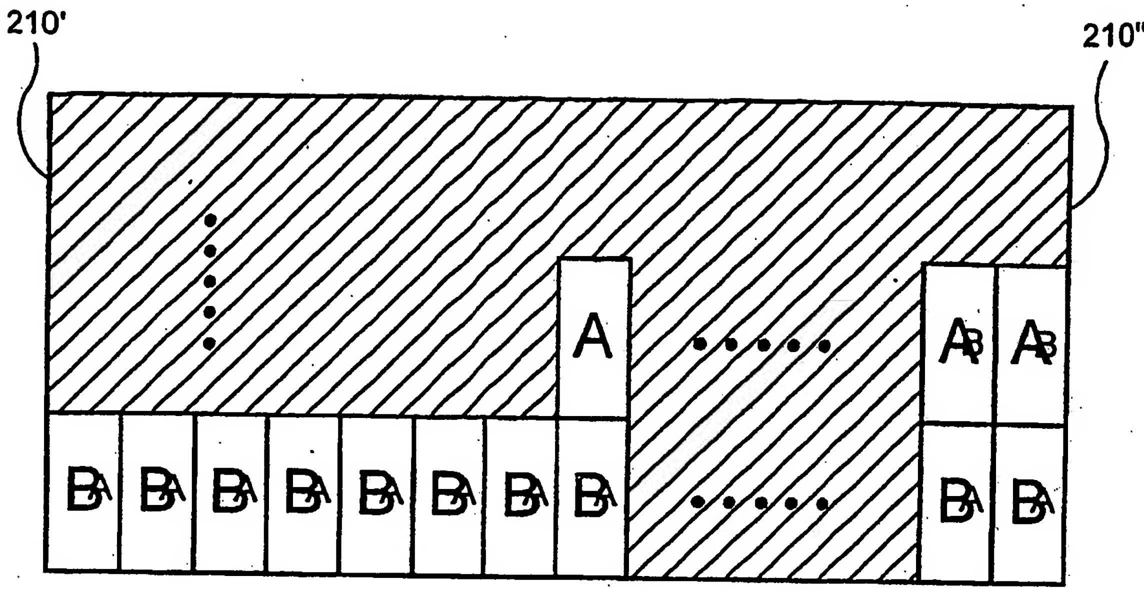
FIG. 4D


210'
210"
B
A
B A
B A
B A
B A
B A
B A
B A
B A
B A
B A
170

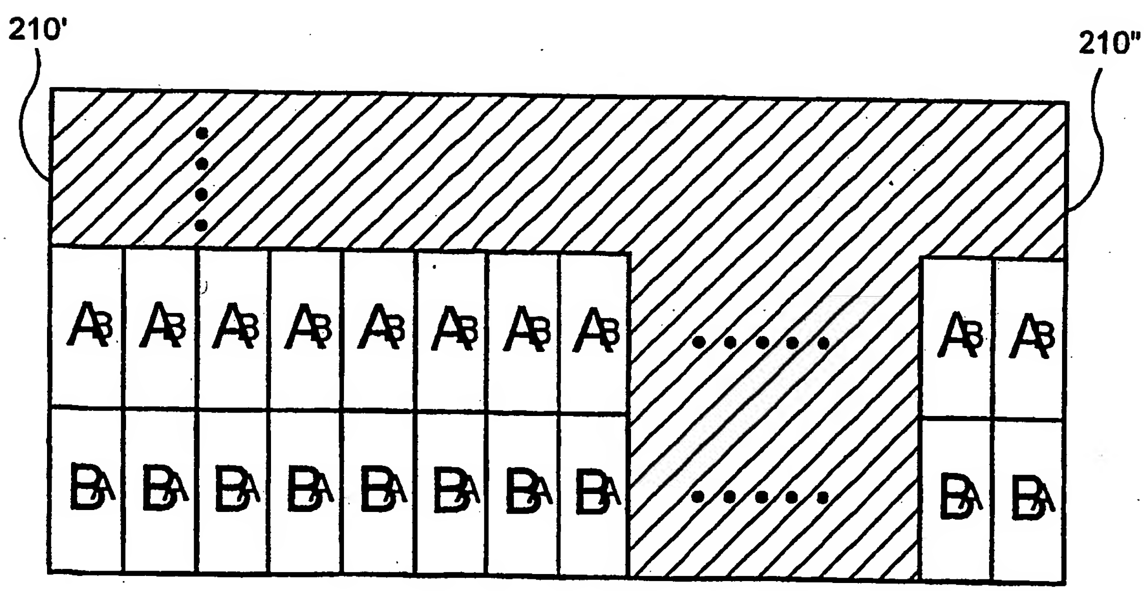
F I G. 4E


210'
210"
B
A B
B A
B A
B A
B A
B A
B A
B A
B A
B A
B A

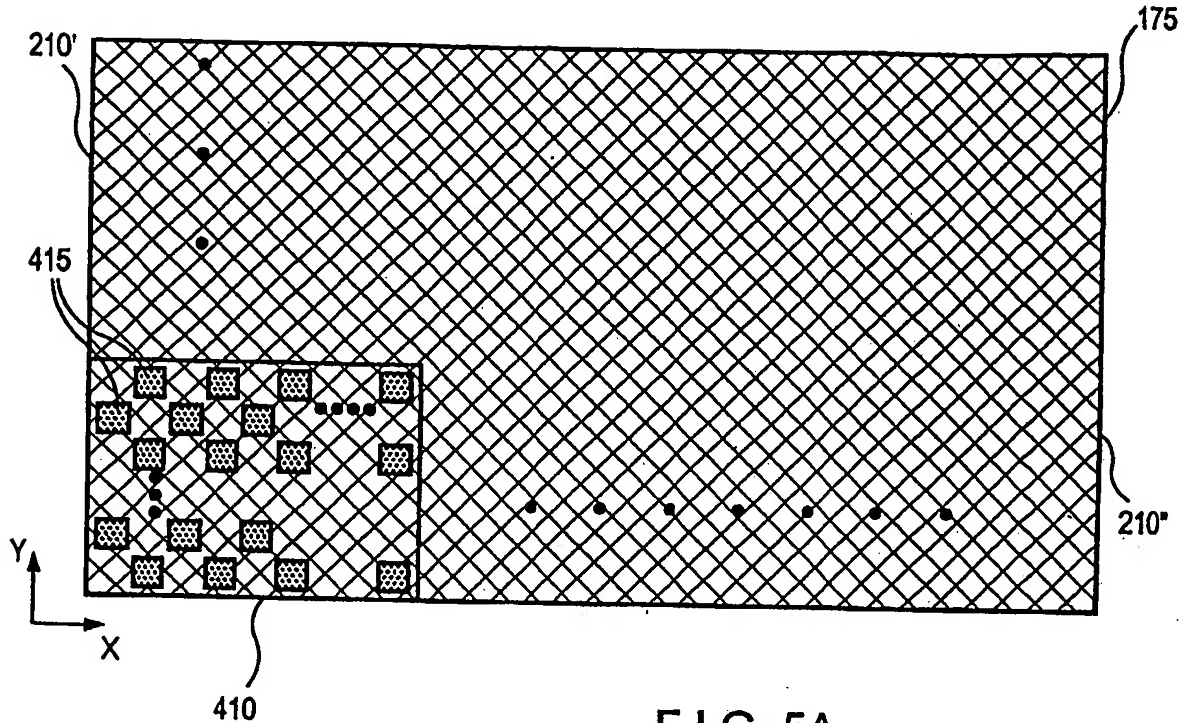
F I G. 4F


210'
210"
A
AB AB
BA BA BA BA BA BA BA BA
BA BA

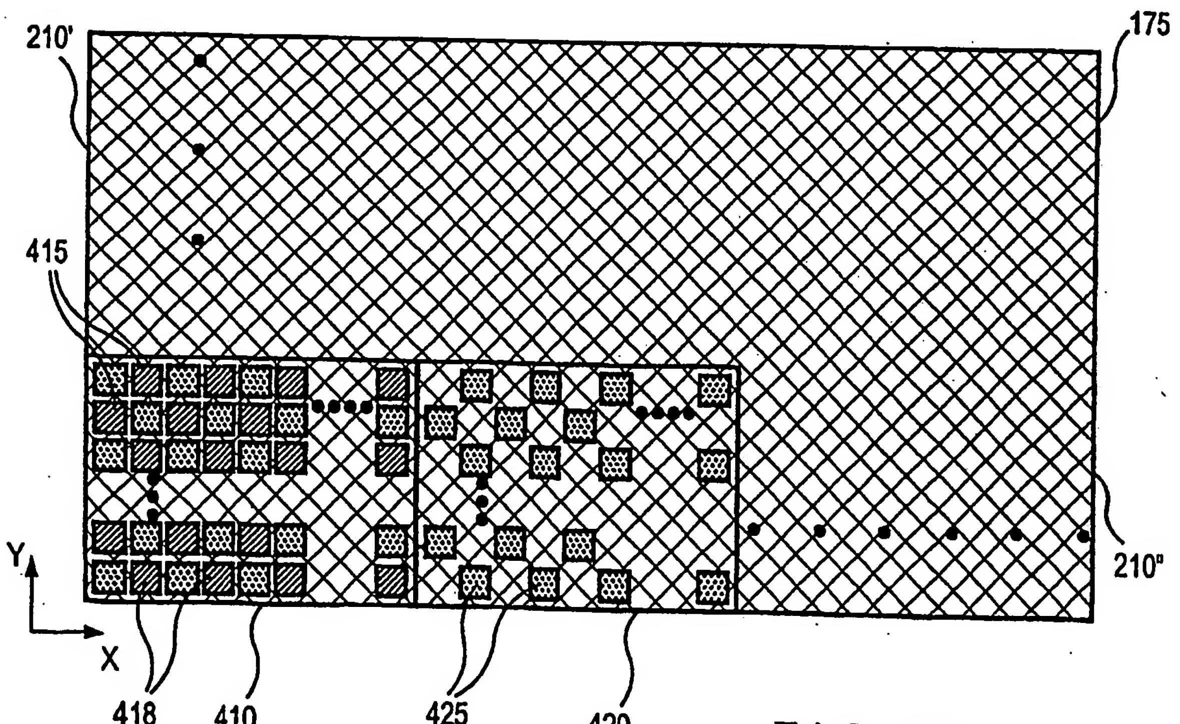
F I G. 4G


210'
210"
AB AB AB AB AB AB AB AB
AB AB
BA BA BA BA BA BA BA BA
BA BA

F I G. 4H



F I G. 5A



F I G. 5B

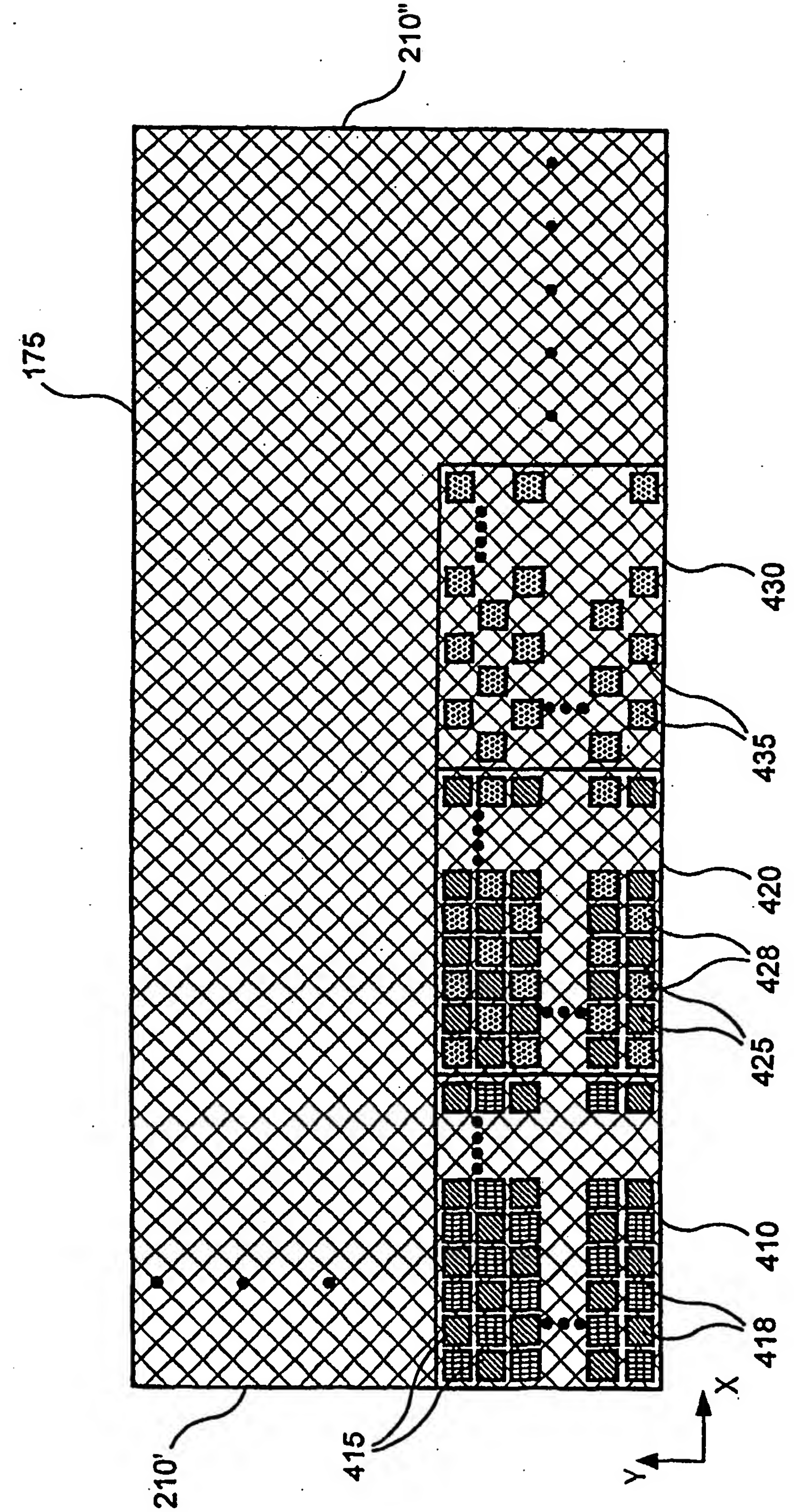


FIG. 5C

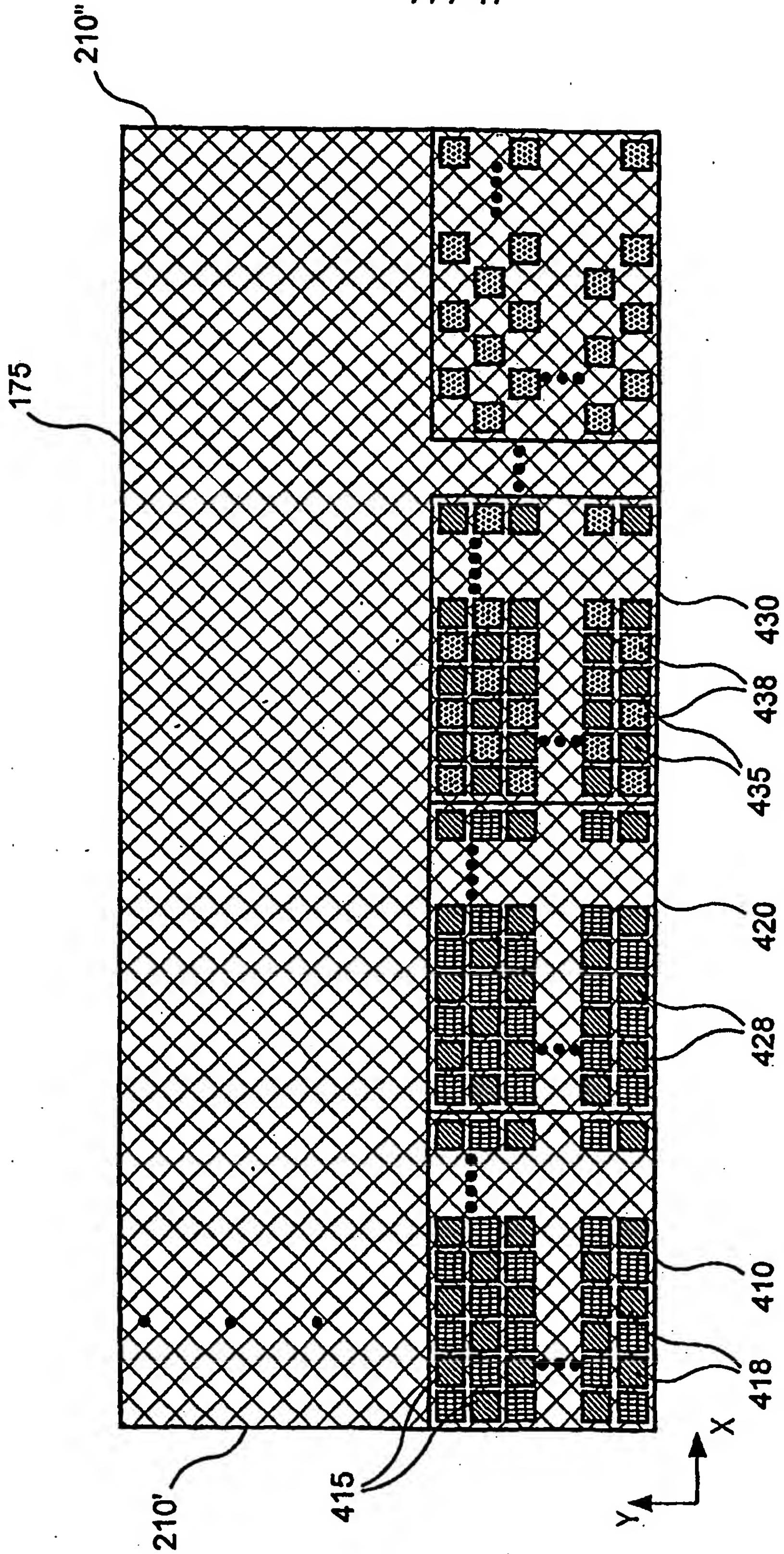


FIG. 5D

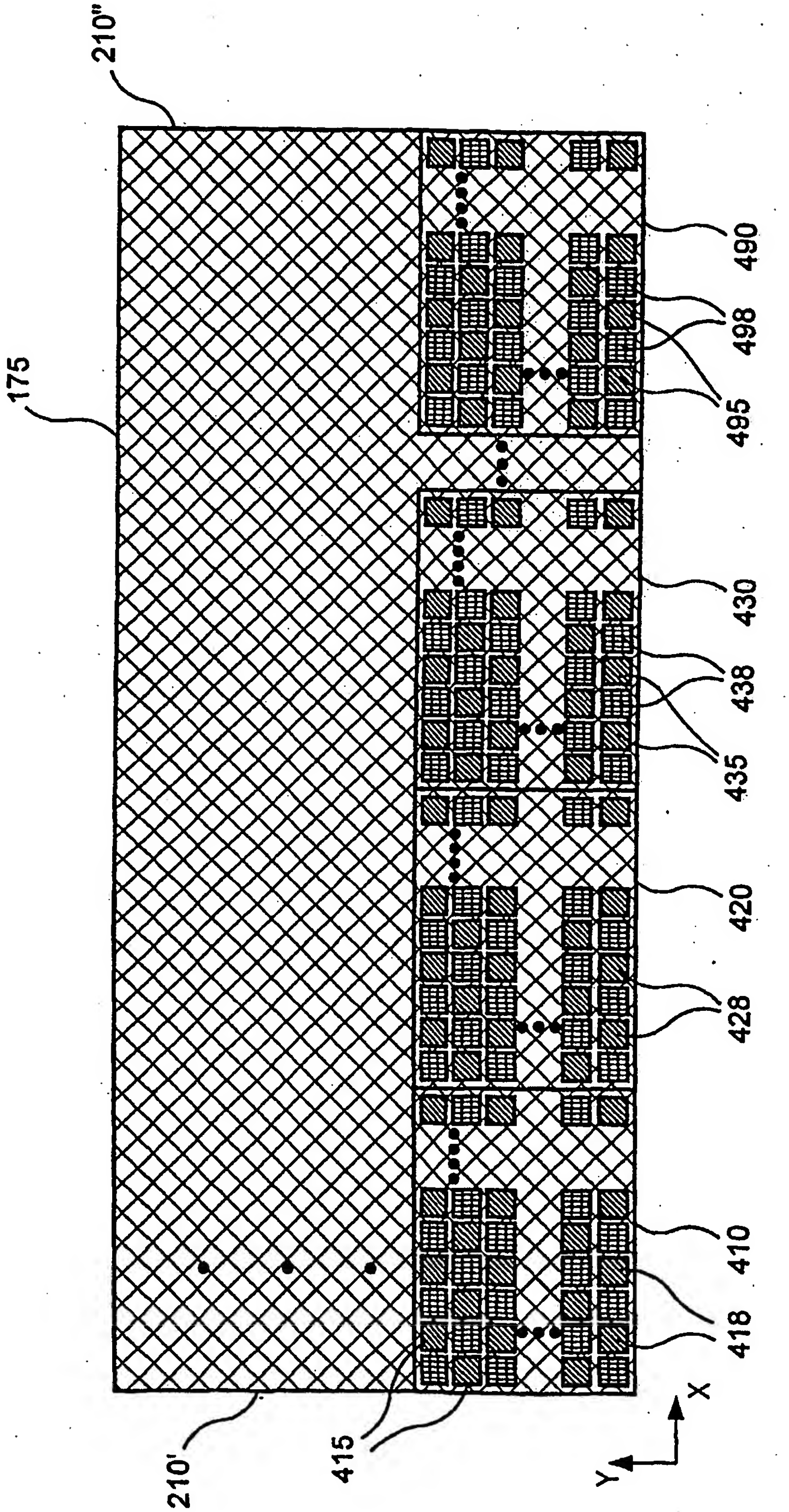


FIG. 5E

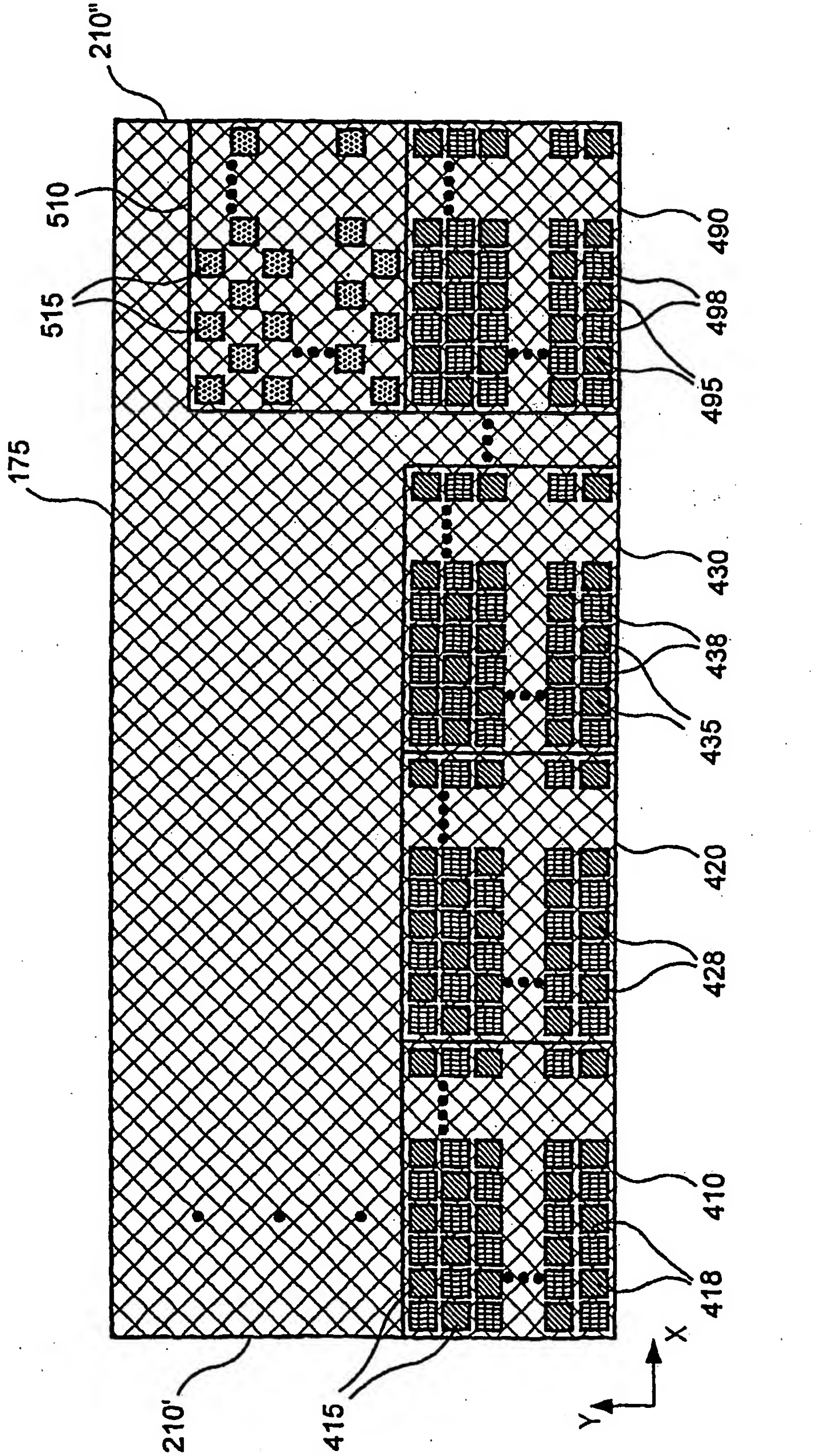

210"
510
515
175
490
498
495
430
438
435
420
428
410
418
210'
415
X
Y

FIG. 5F

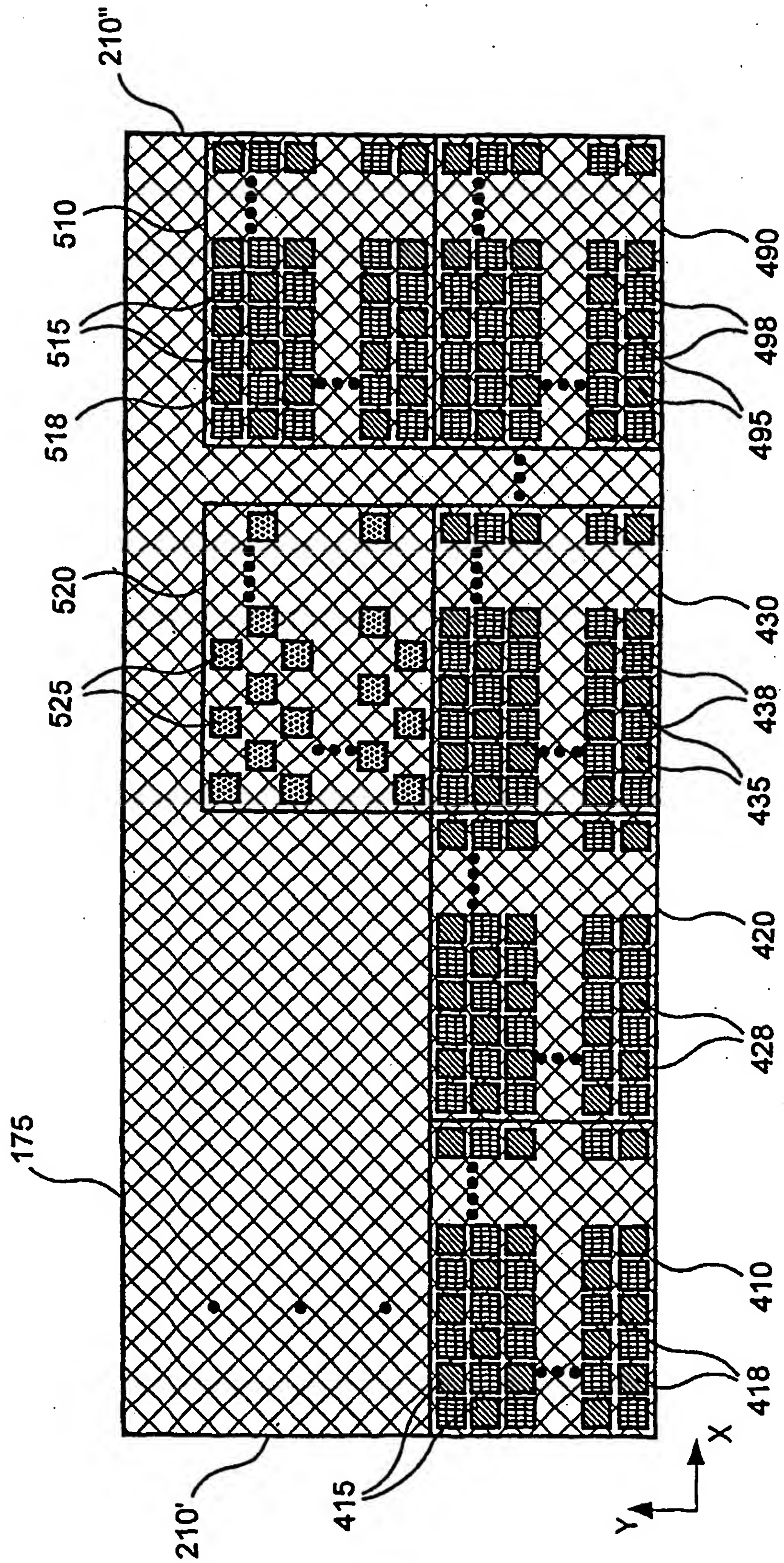

210"
510
515
518
520
525
175
210'
415
490
498
495
430
438
435
420
428
410
418
X
Y

FIG. 5G

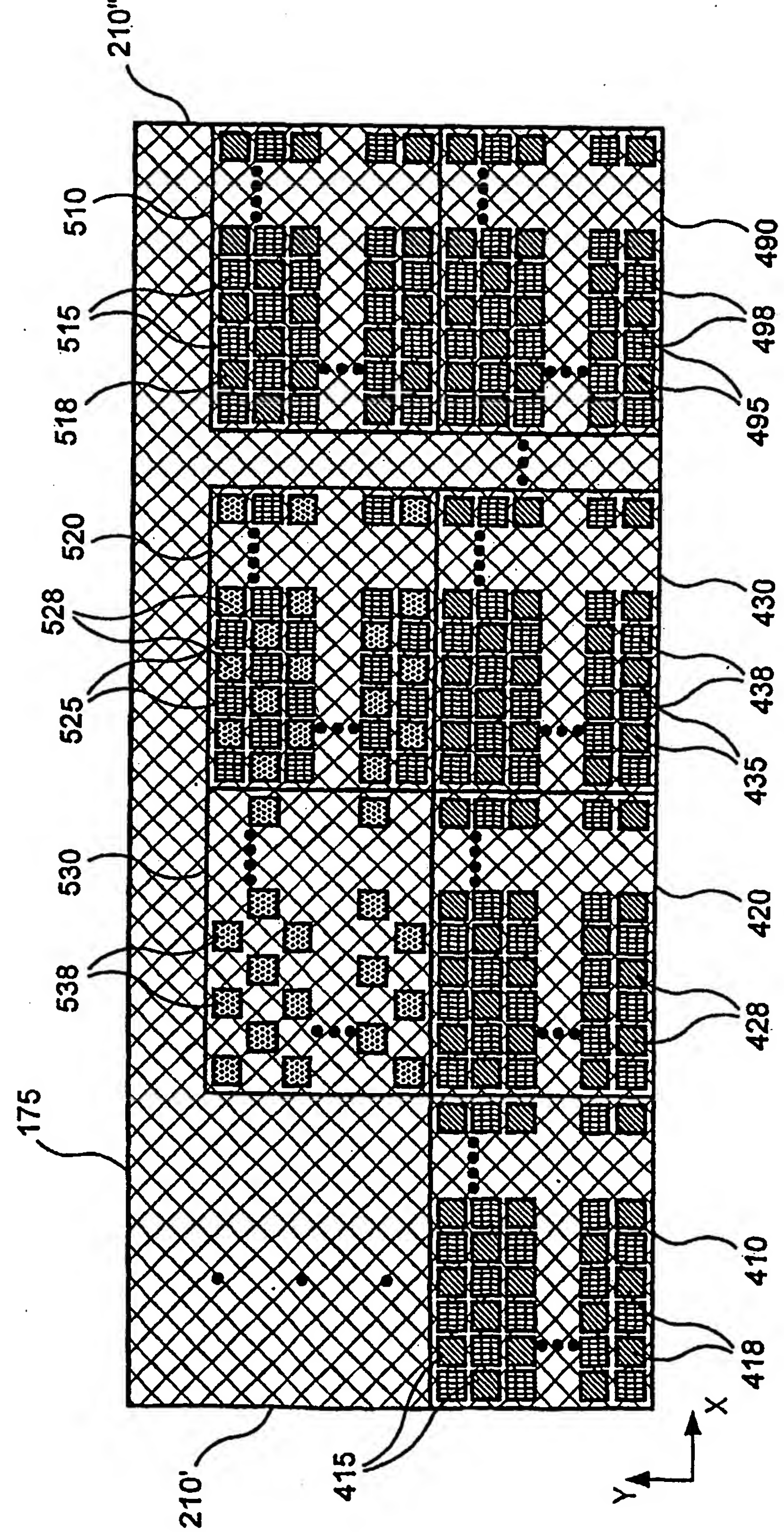
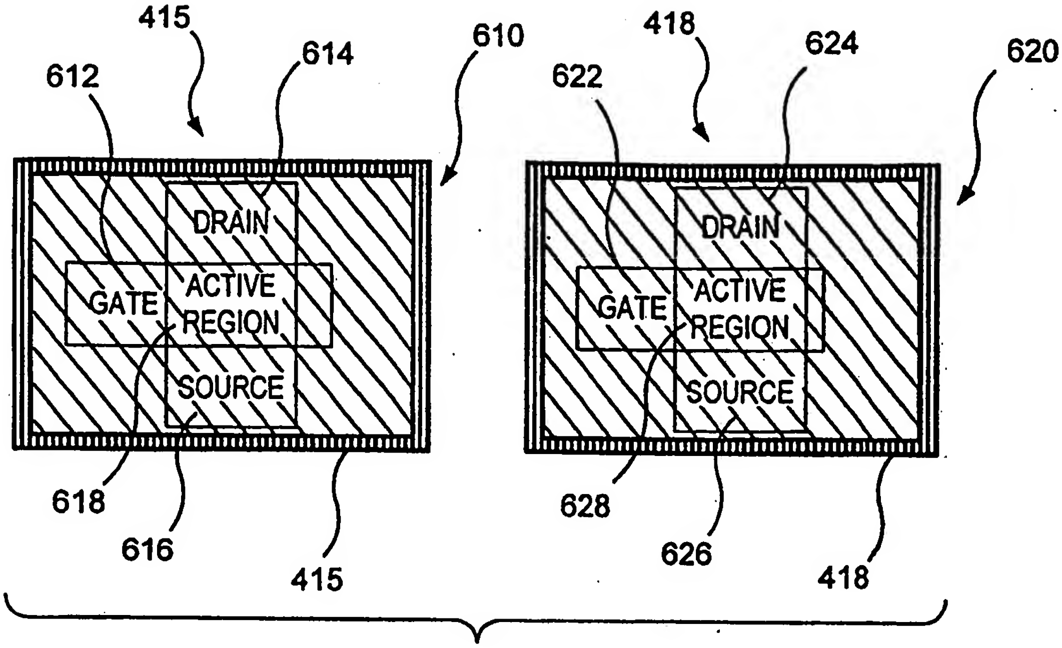
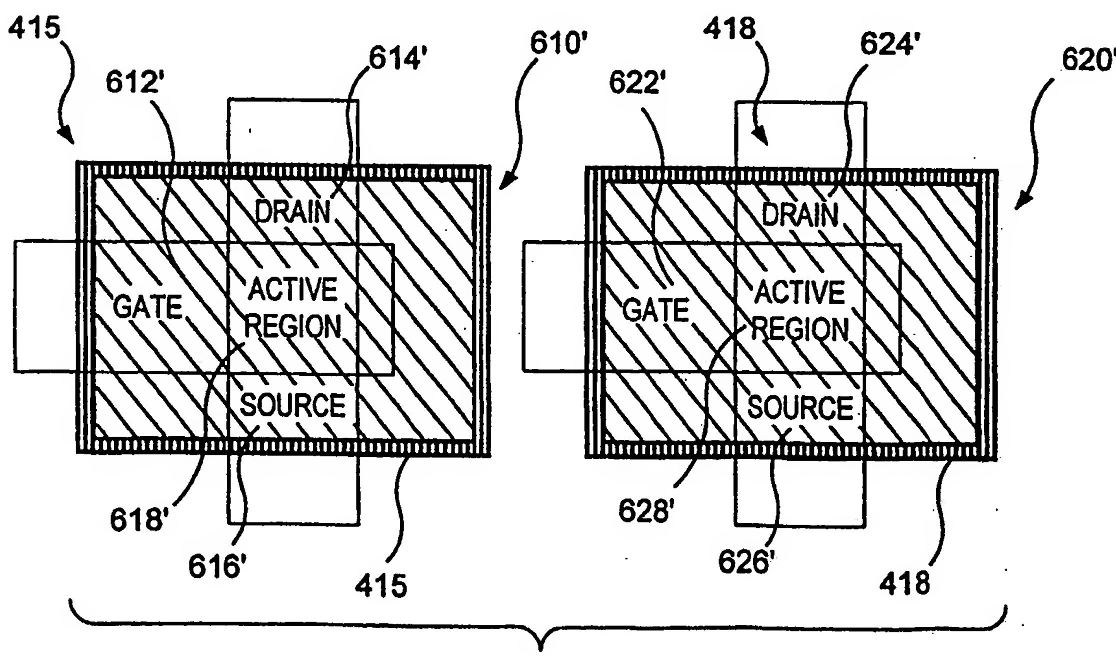

210"
510
515
518
520
528
525
530
538
175
210'
415
490
498
495
430
438
435
420
428
410
418
Y
X

FIG. 5H


415
612
614
610
418
622
624
620
DRAIN
GATE
ACTIVE REGION
SOURCE
DRAIN
GATE
ACTIVE REGION
SOURCE
618
616
415
628
626
418

F I G. 6A


415
612'
614'
610'
418
622'
624'
620'
DRAIN
GATE
ACTIVE REGION
SOURCE
DRAIN
GATE
ACTIVE REGION
SOURCE
618'
616'
415
628'
626'
418

F I G. 6B

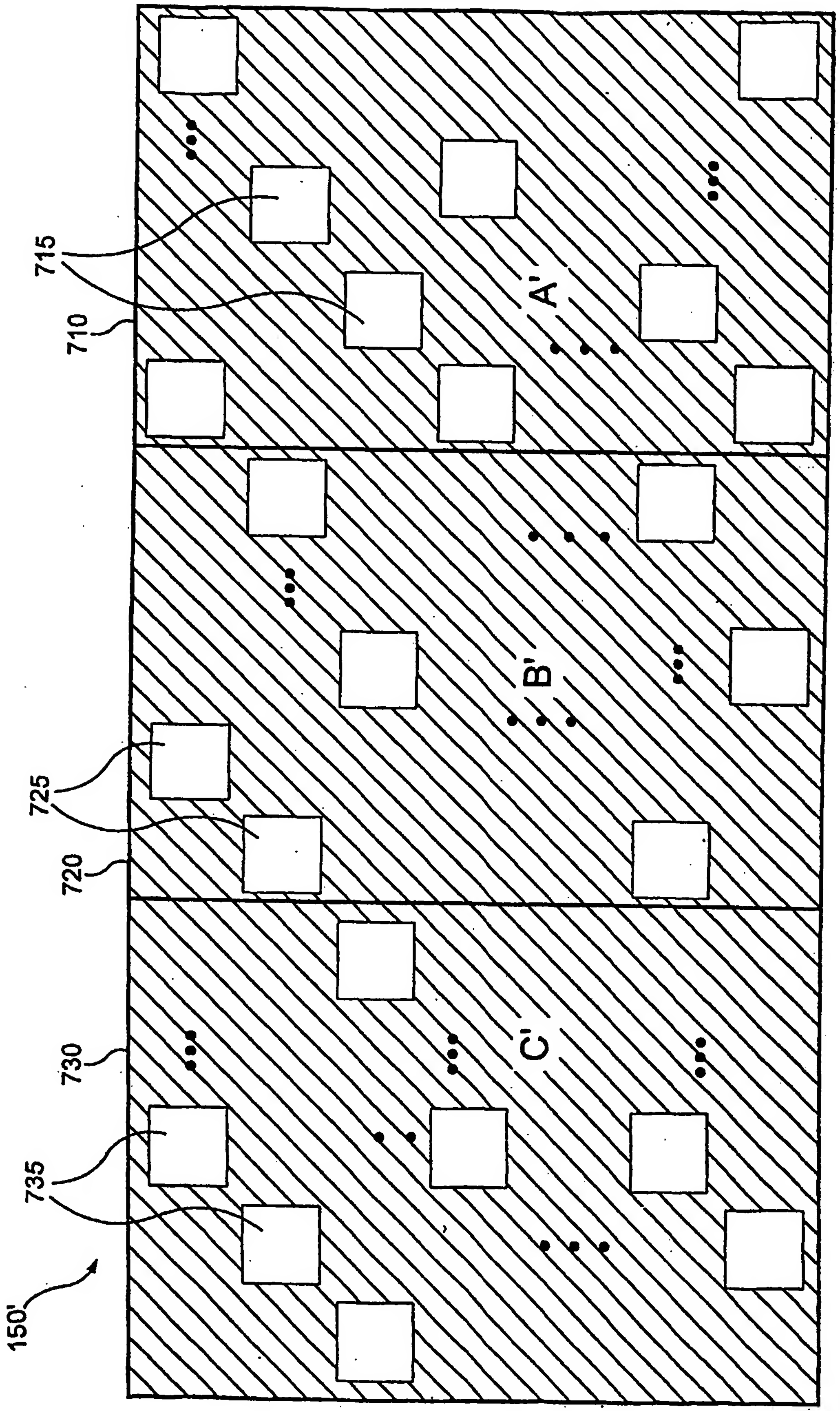
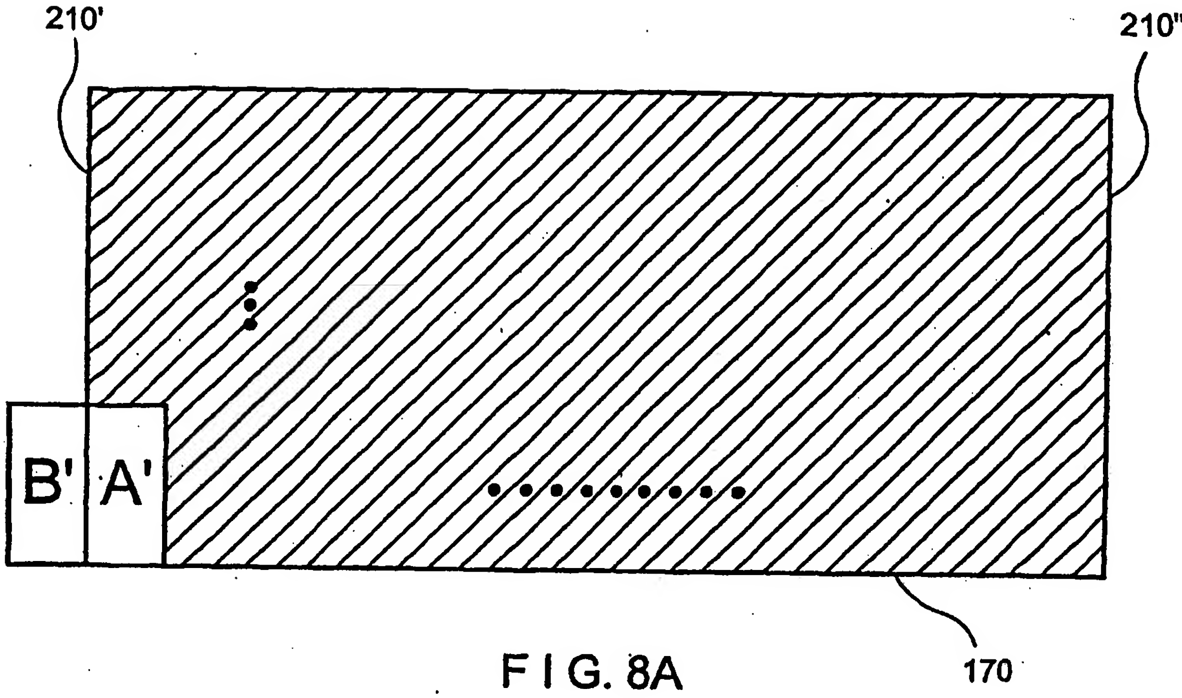
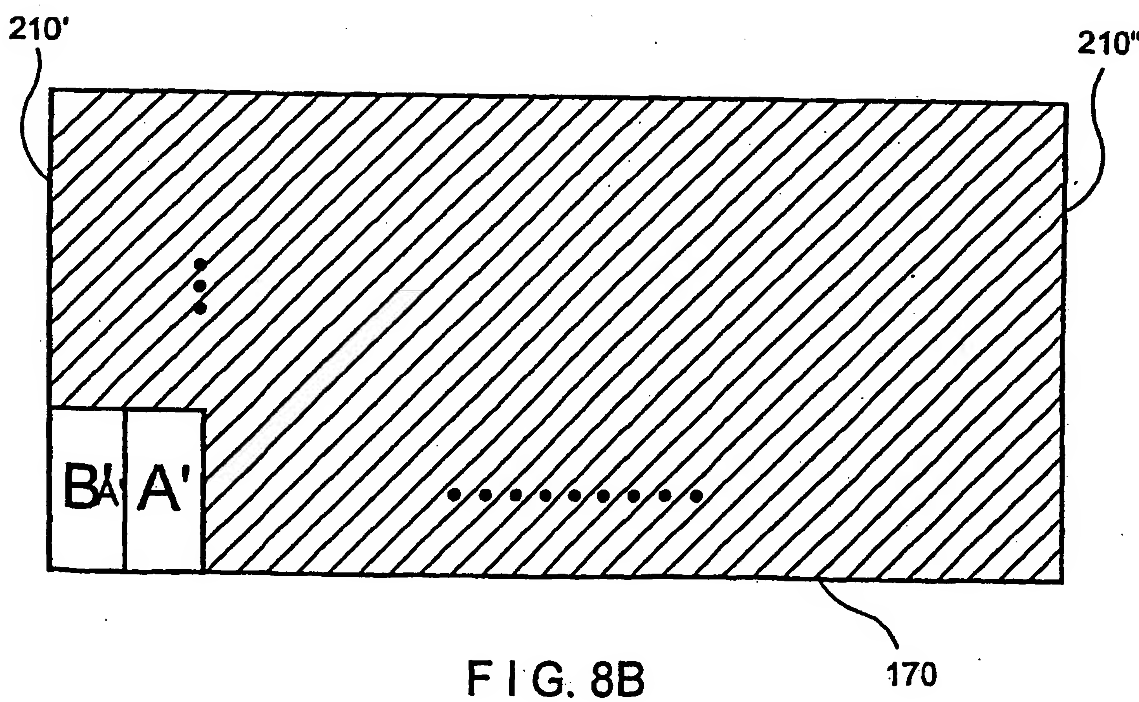


FIG. 7



F I G. 8A



F I G. 8B

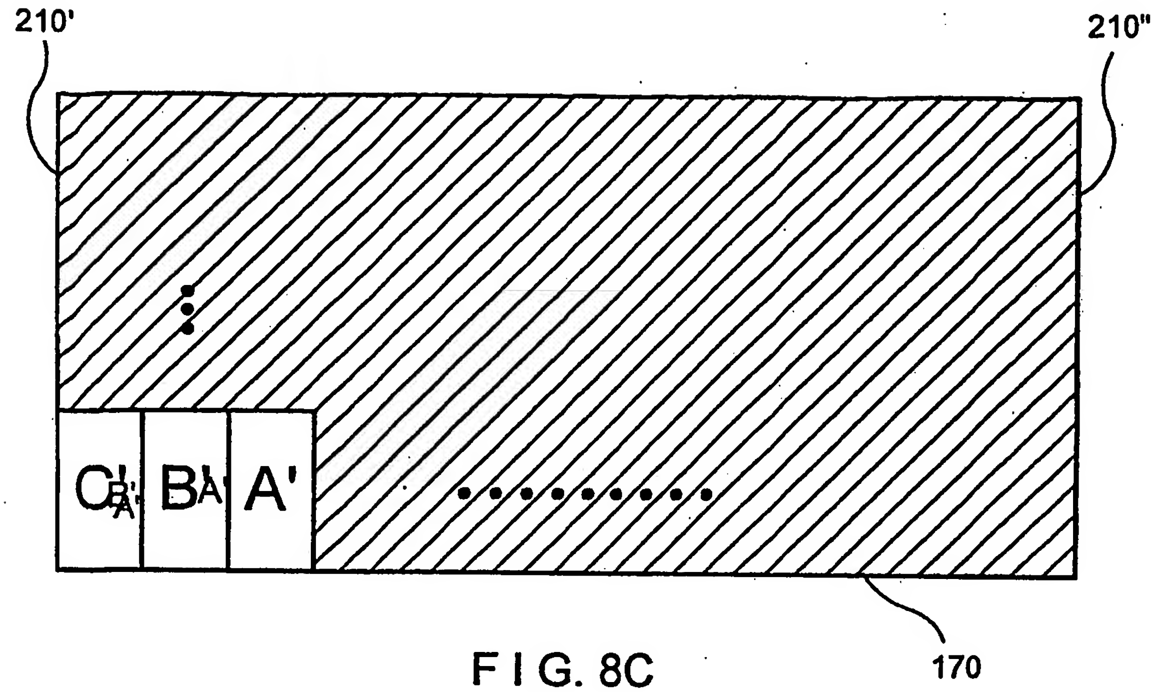


FIG. 8C

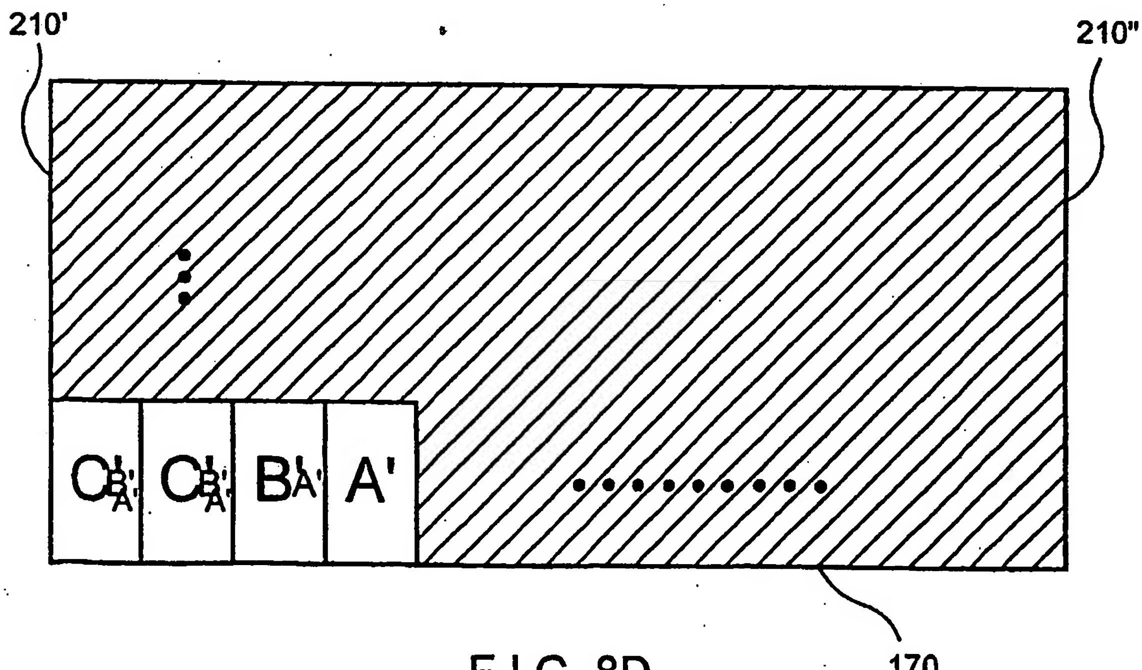
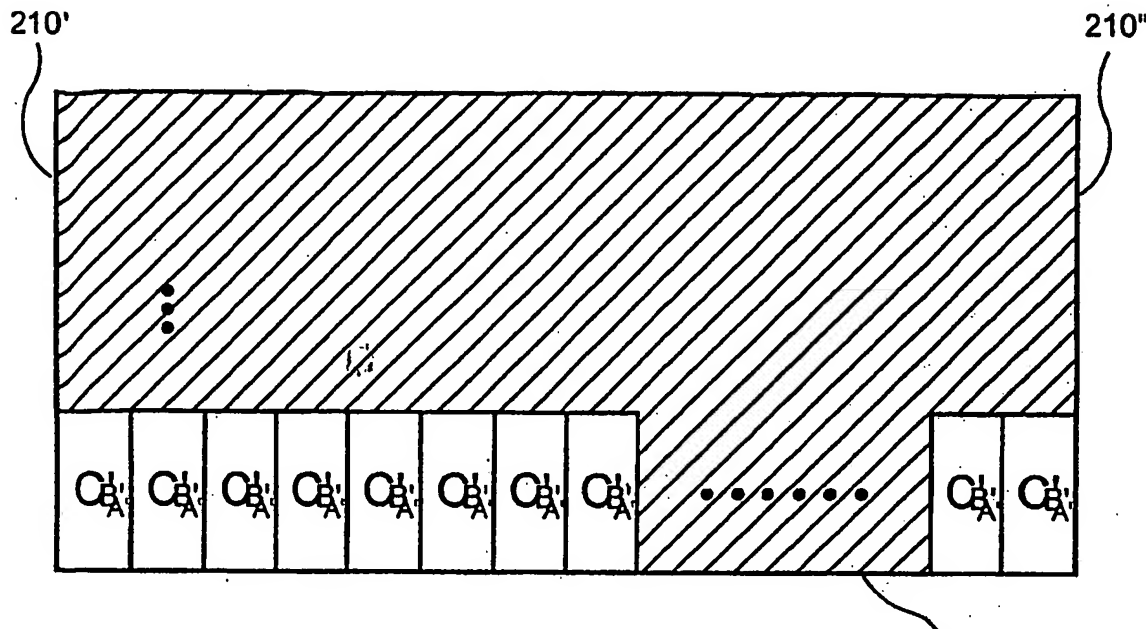
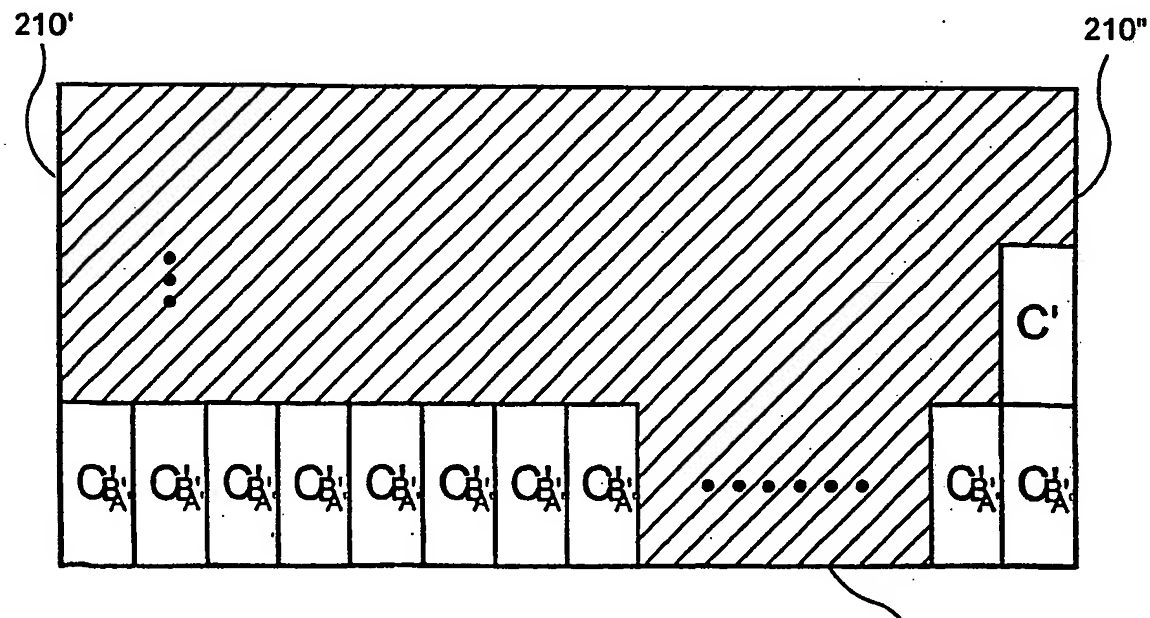


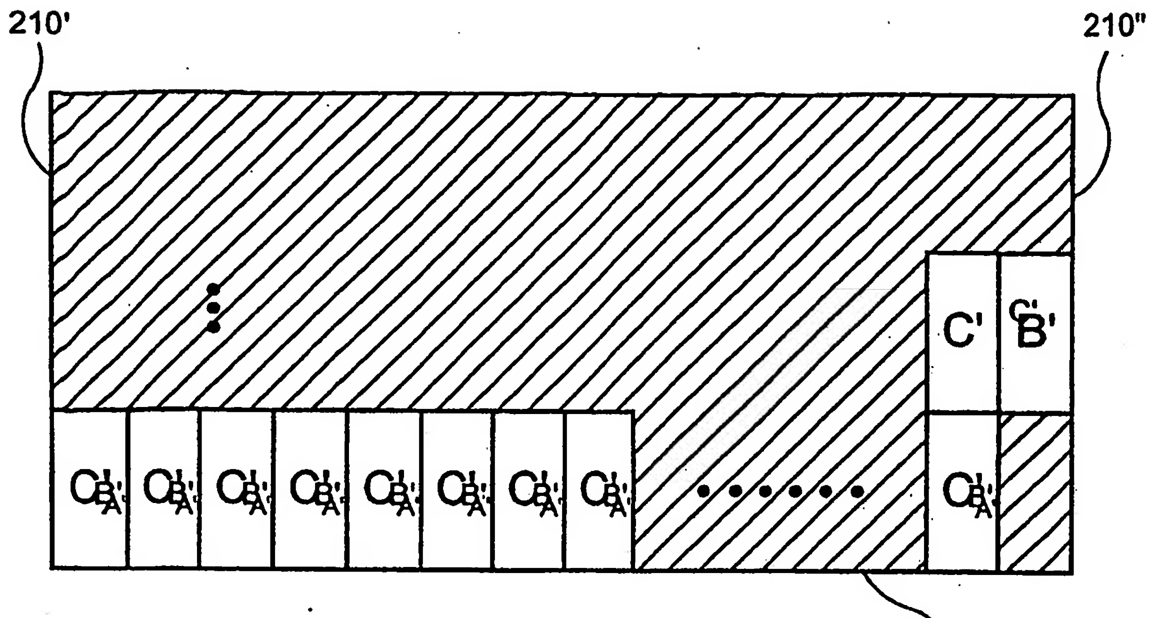
FIG. 8D



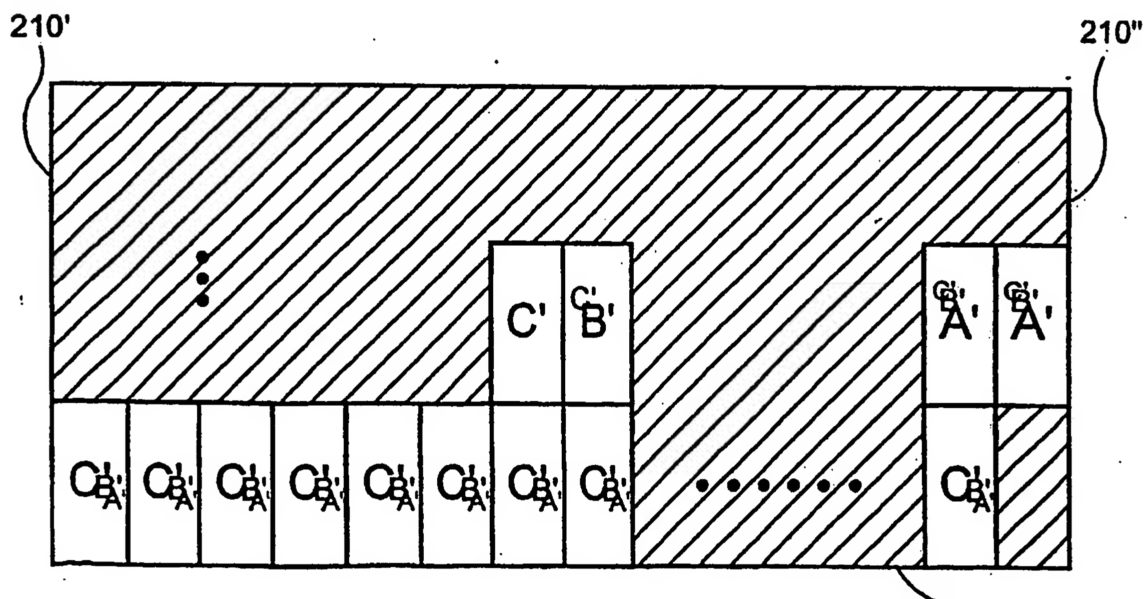
F I G. 8E



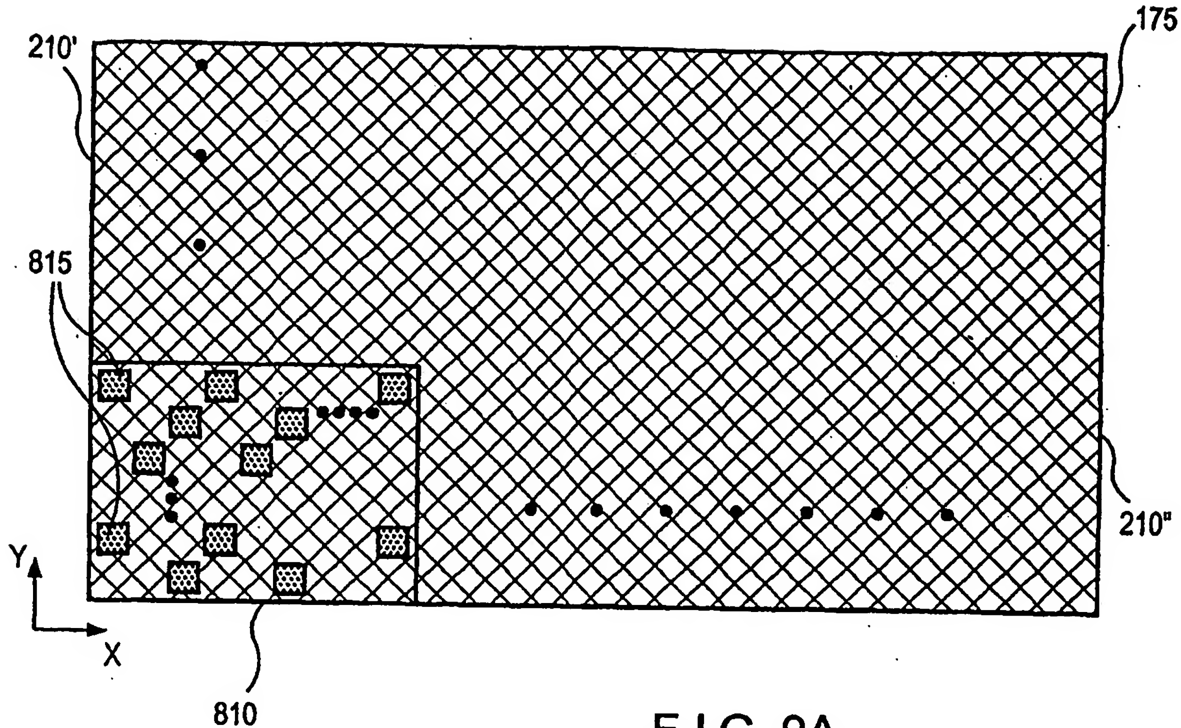
F I G. 8F



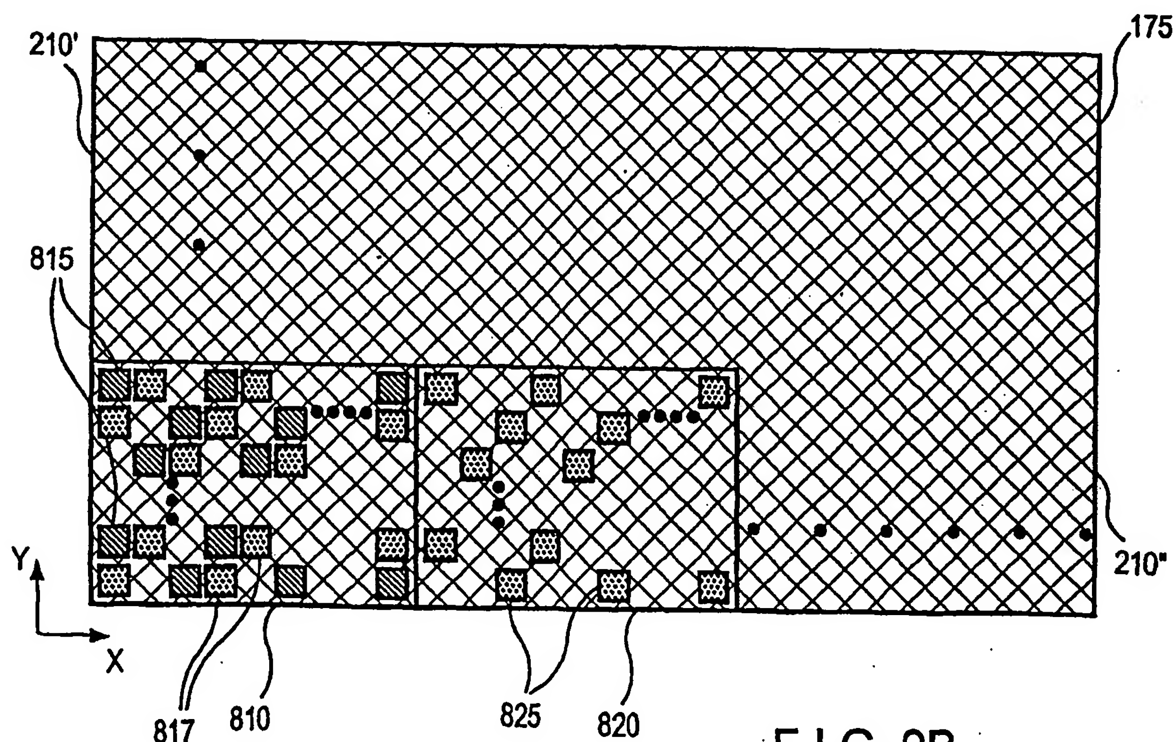
F I G. 8G



F I G. 8H



F I G. 9A



F I G. 9B

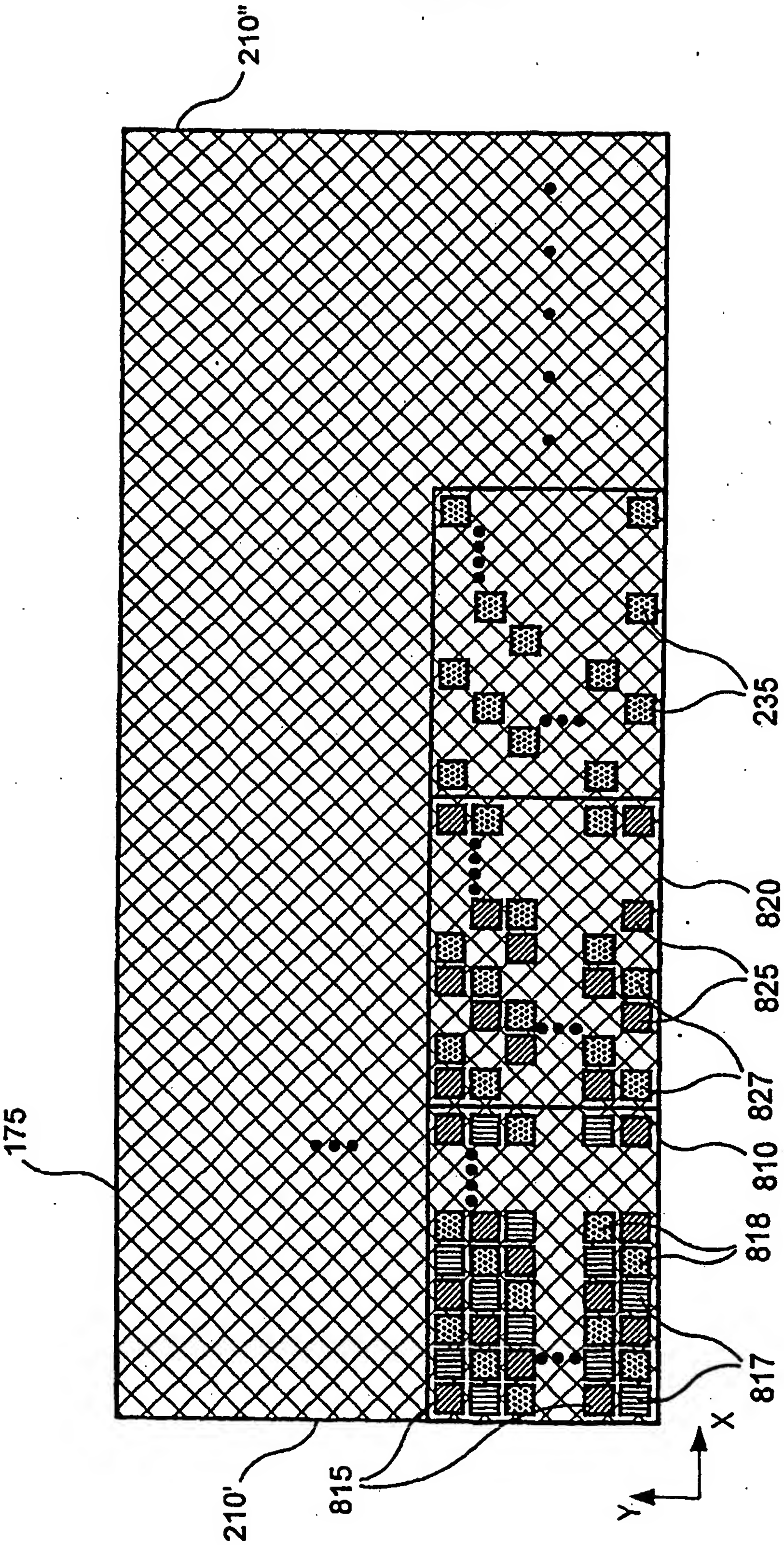


FIG. 9C

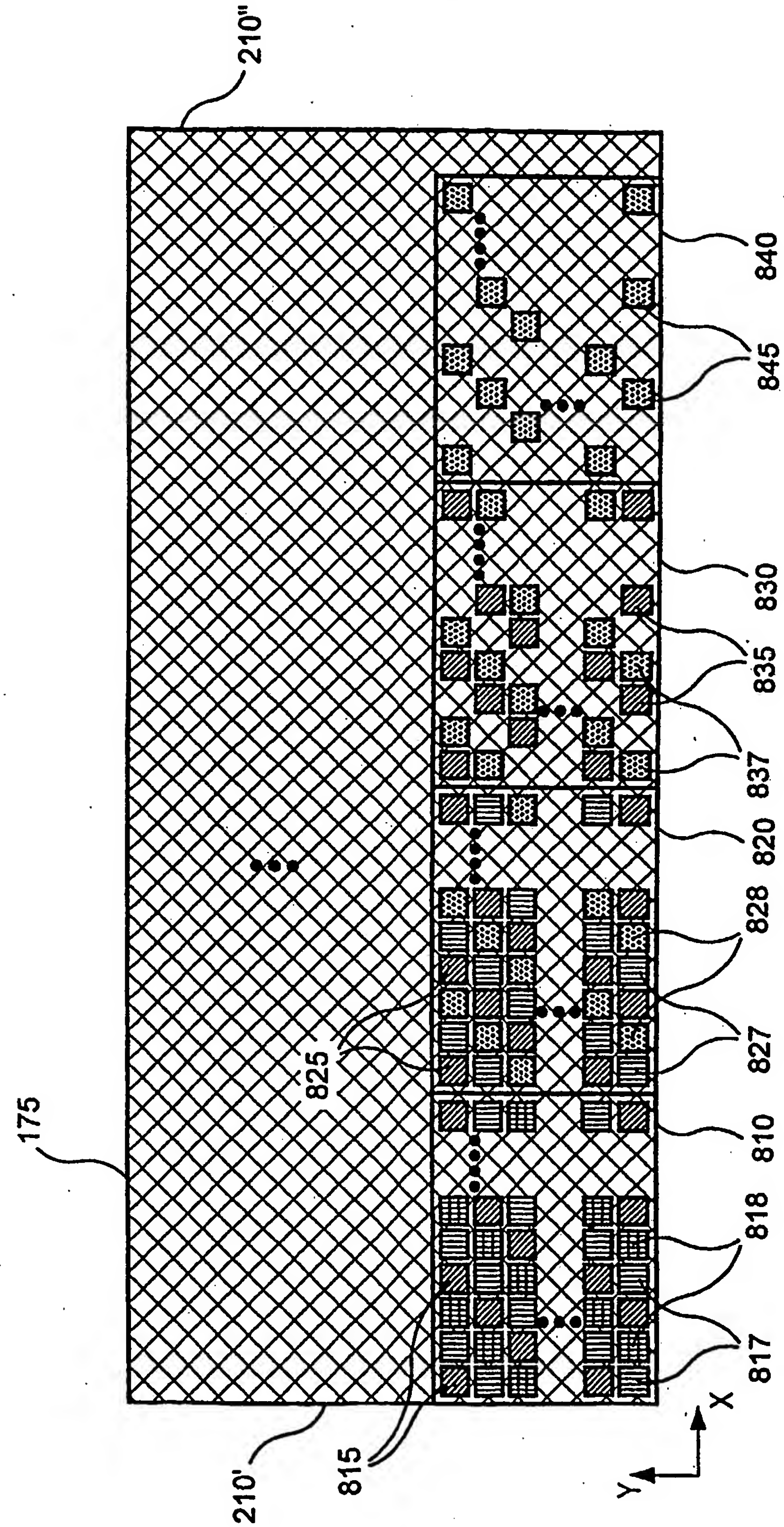
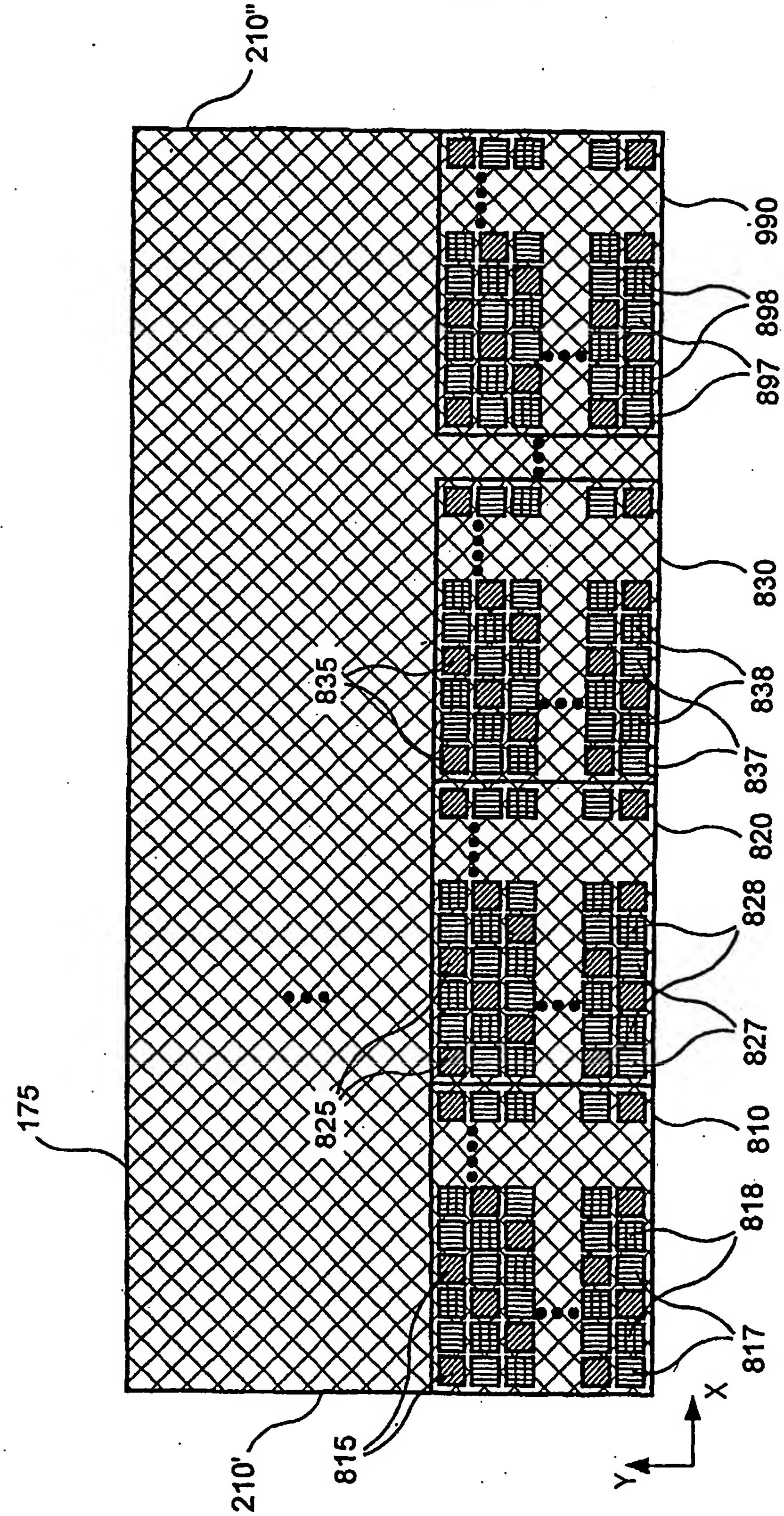

210"
840
845
830
835
837
820
828
827
825
175
810
818
817
210'
815
X
Y

FIG. 9D



210"
990
898
897
830
835
838
837
820
828
827
825
175
810
818
817
210'
815
X
Y

FIG. 9E

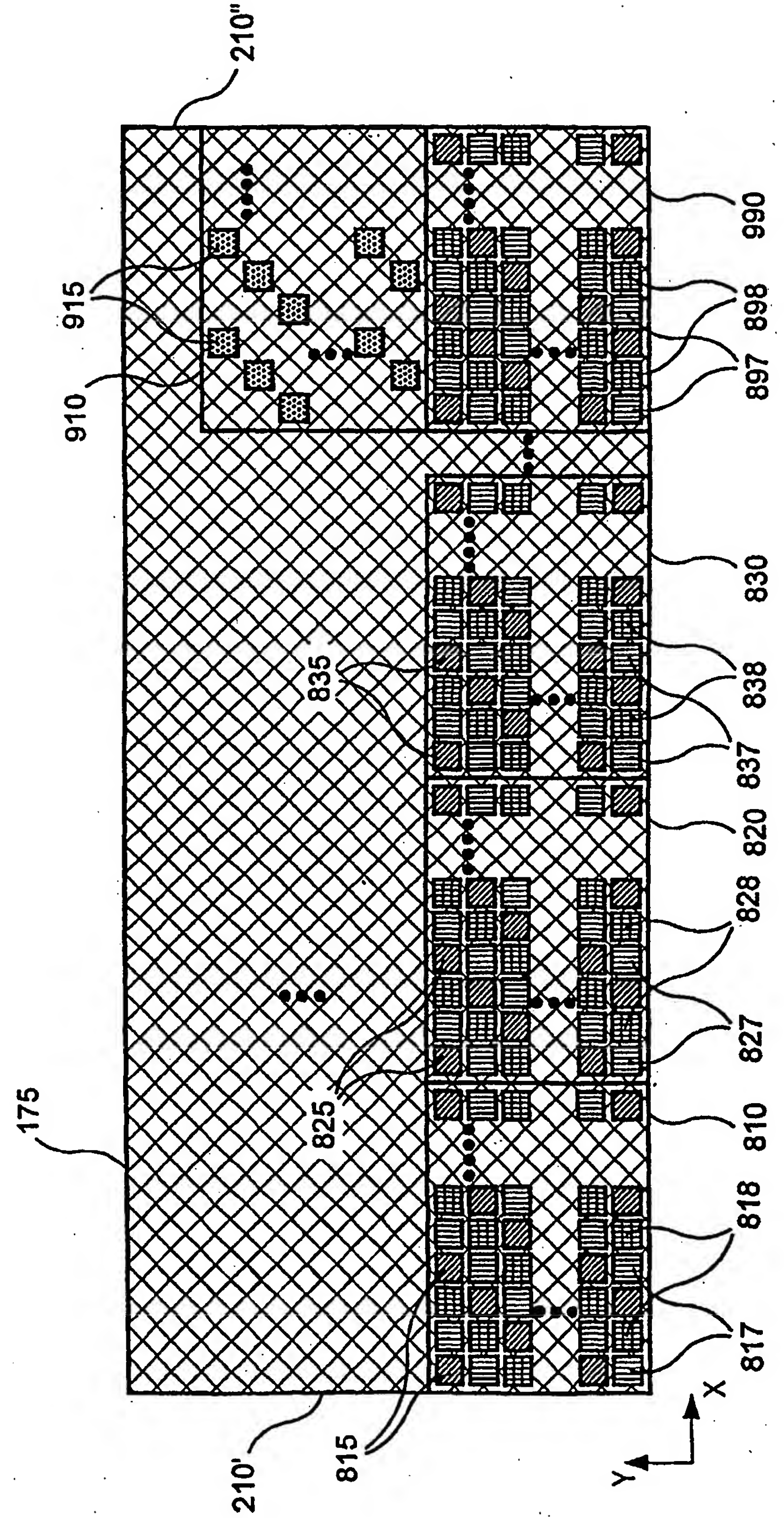

210"
915
910
990
898
897
830
835
838
837
820
828
827
825
810
818
817
175
210'
815
X
Y

FIG. 9F

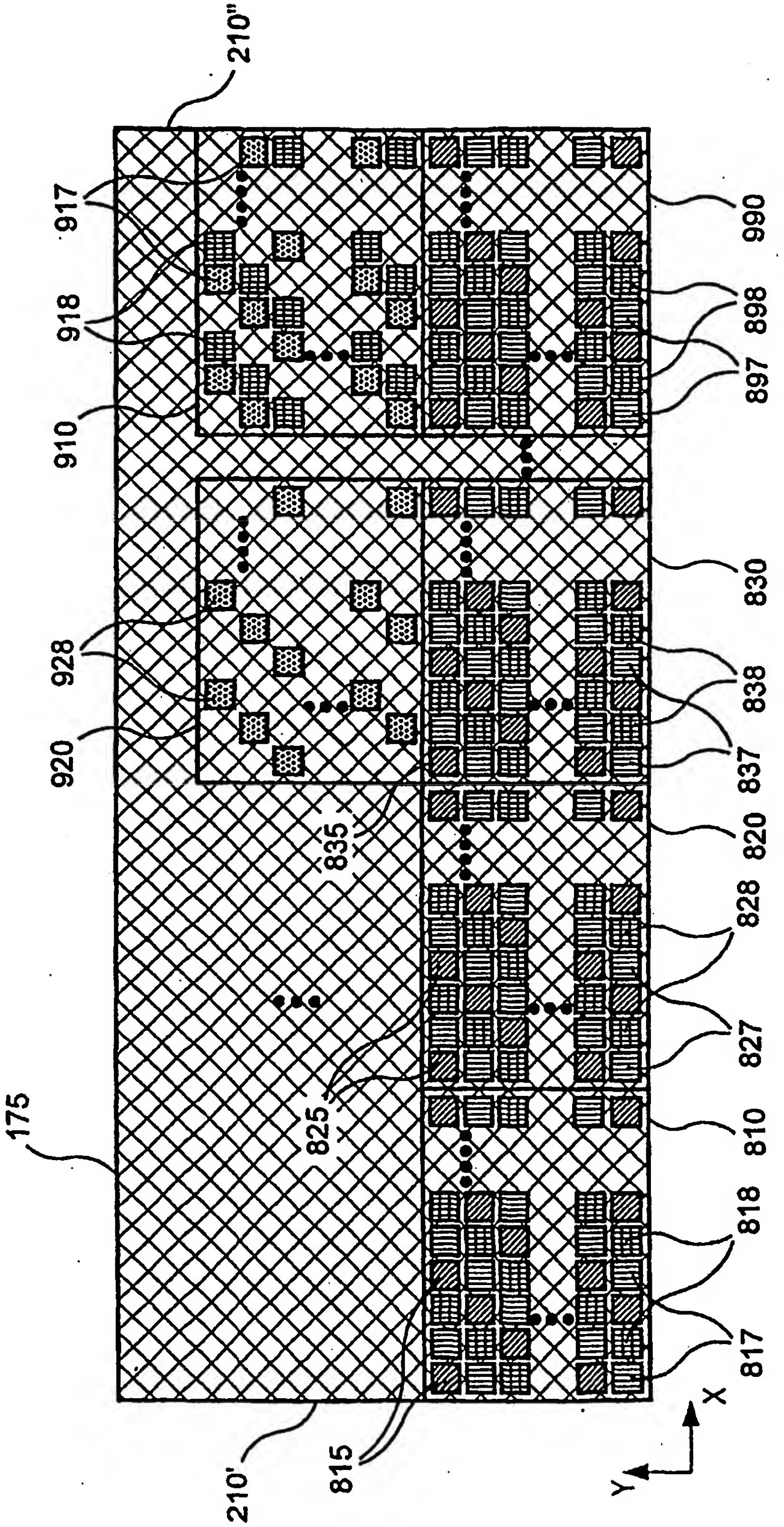

210"
917
918
910
928
920
835
825
175
210'
815
990
898
897
830
838
837
820
828
827
810
818
817
X
Y

FIG. 9G

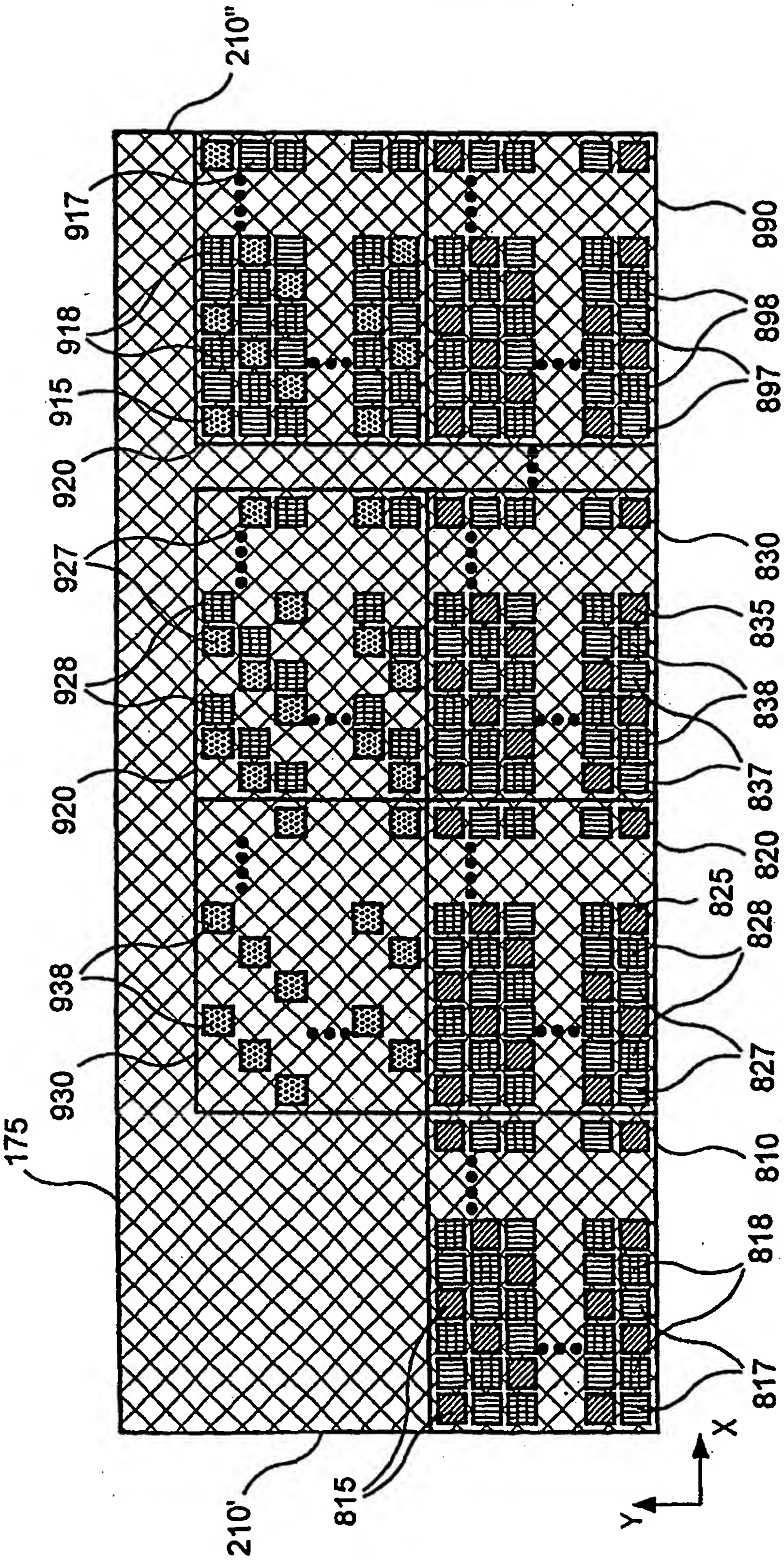

210"
917
918
915
920
927
928
920
938
930
175
210'
815
990
898
897
830
835
838
837
820
825
828
827
810
818
817
X
Y

FIG. 9H

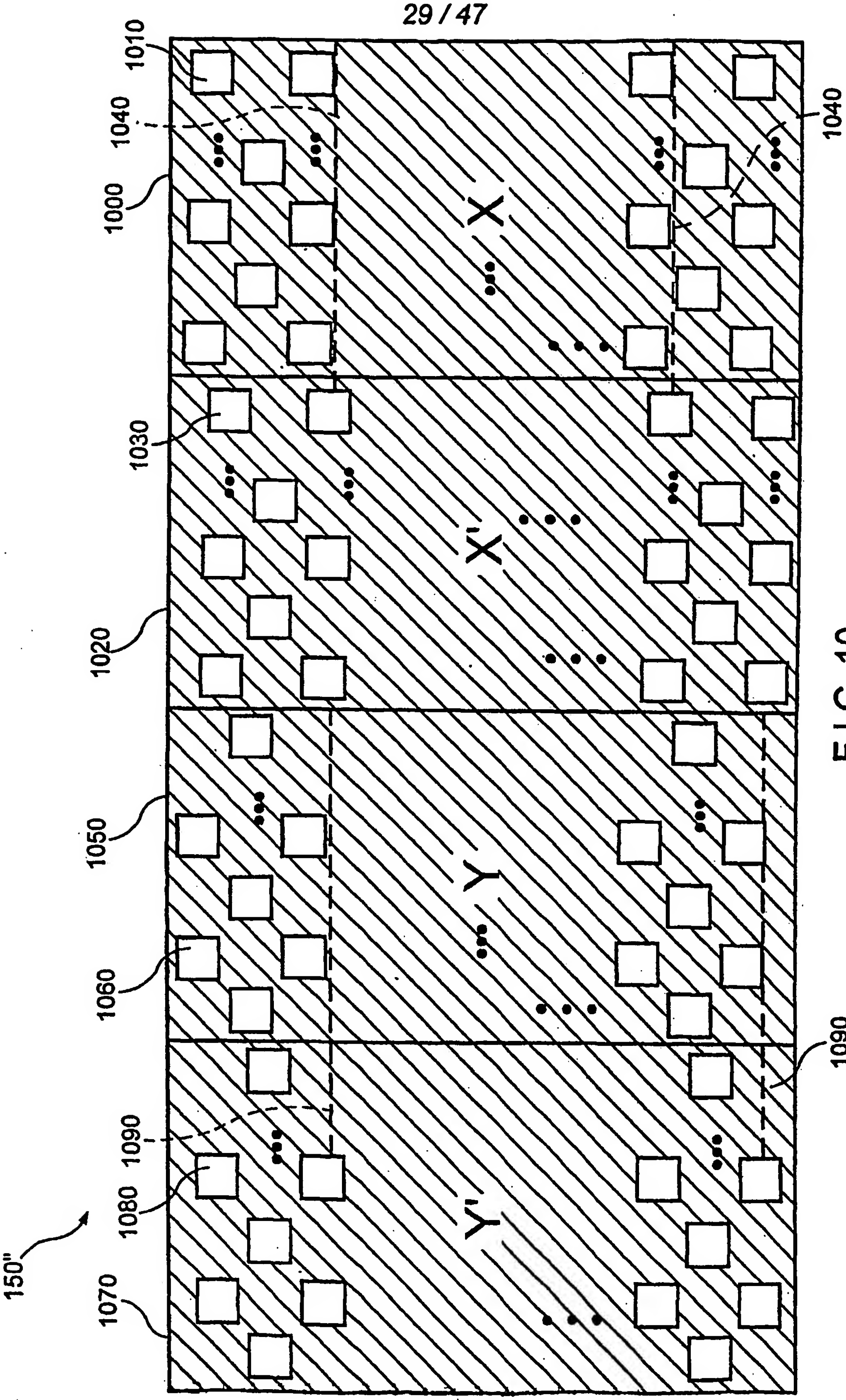

1010
1040
1000
1040
X
1030
X'
1020
1050
Y
1060
1090
1090
1080
Y'
150"
1070

FIG. 10

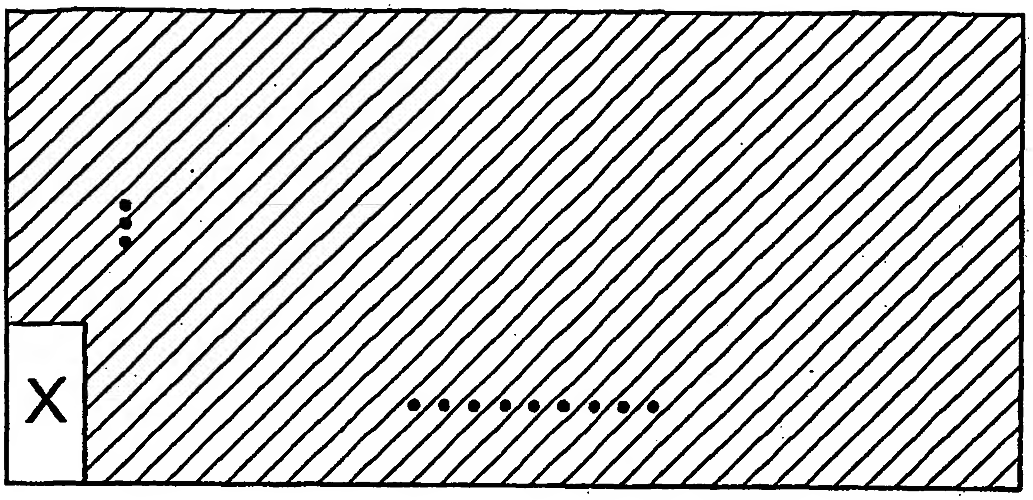


FIG. 11A

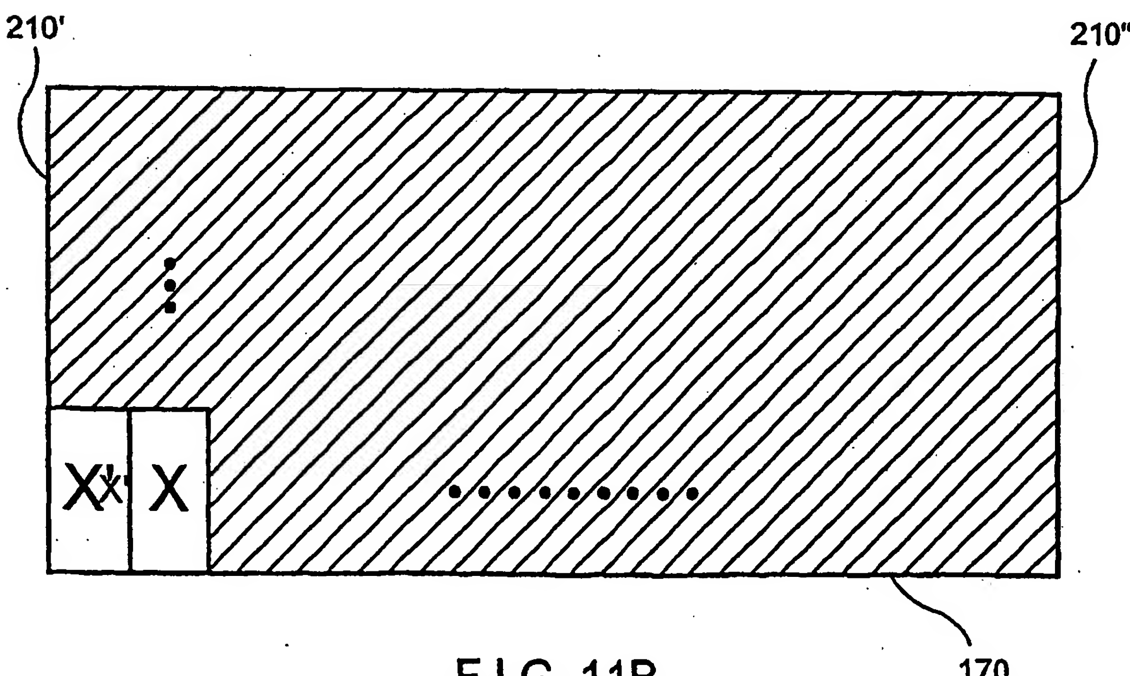
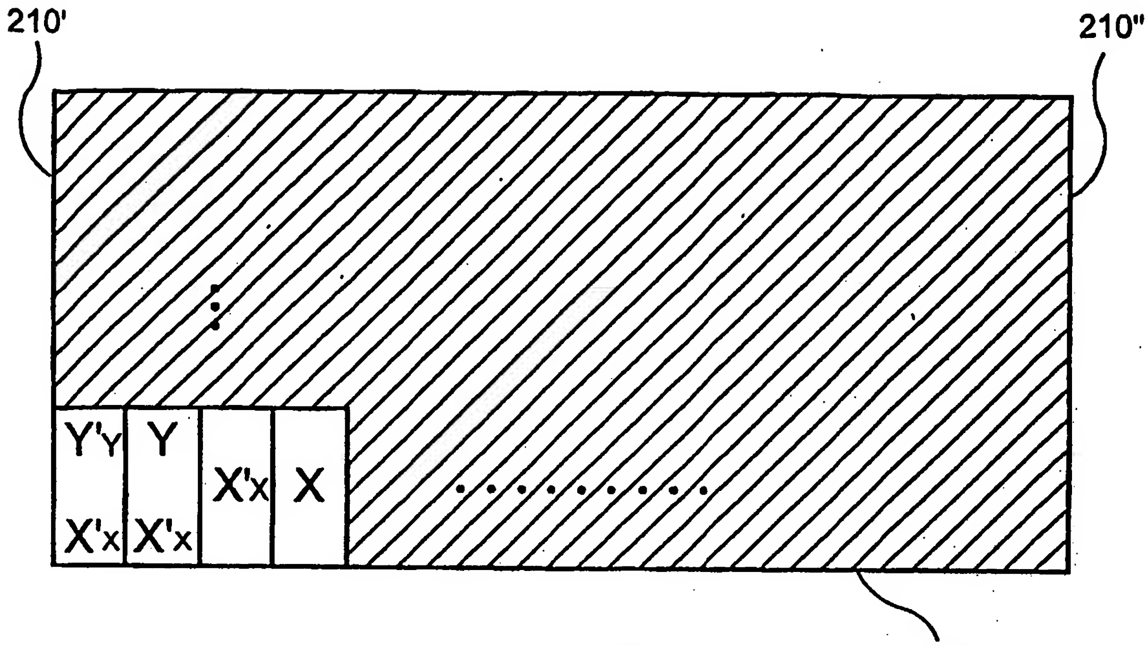
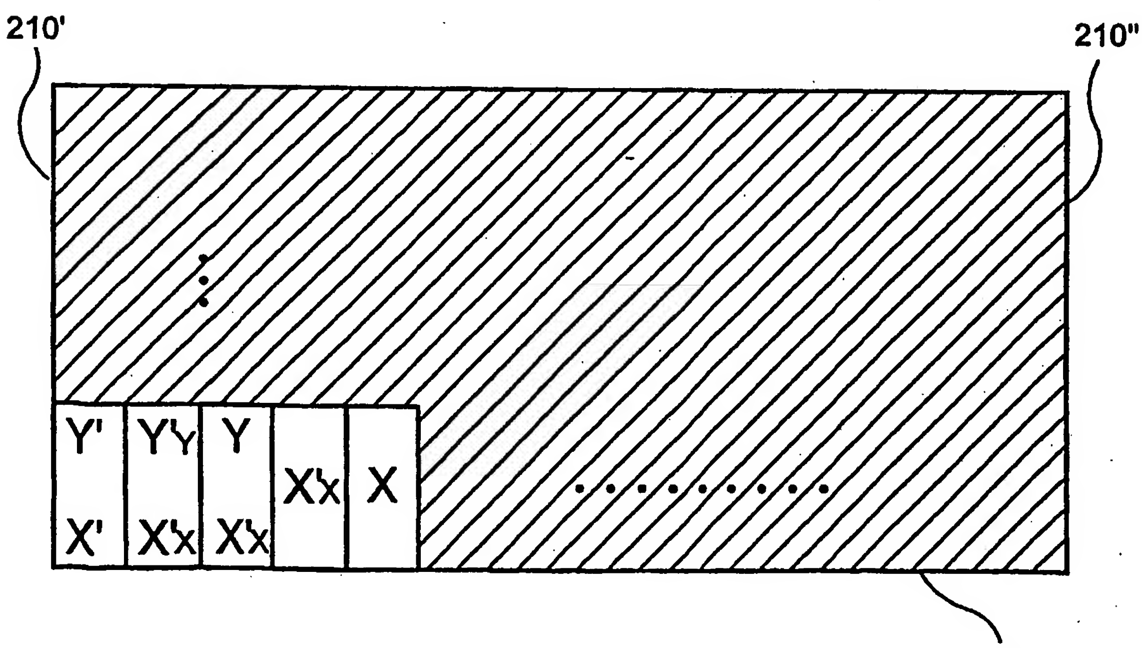


FIG. 11B



F I G. 11C



F I G. 11D

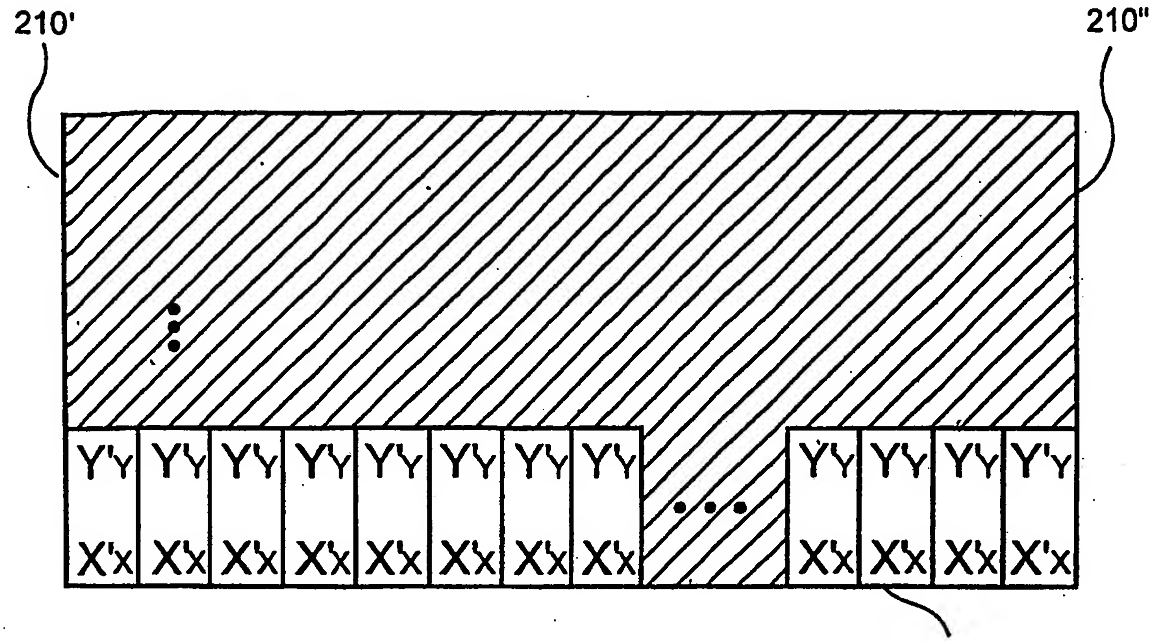


FIG. 11E

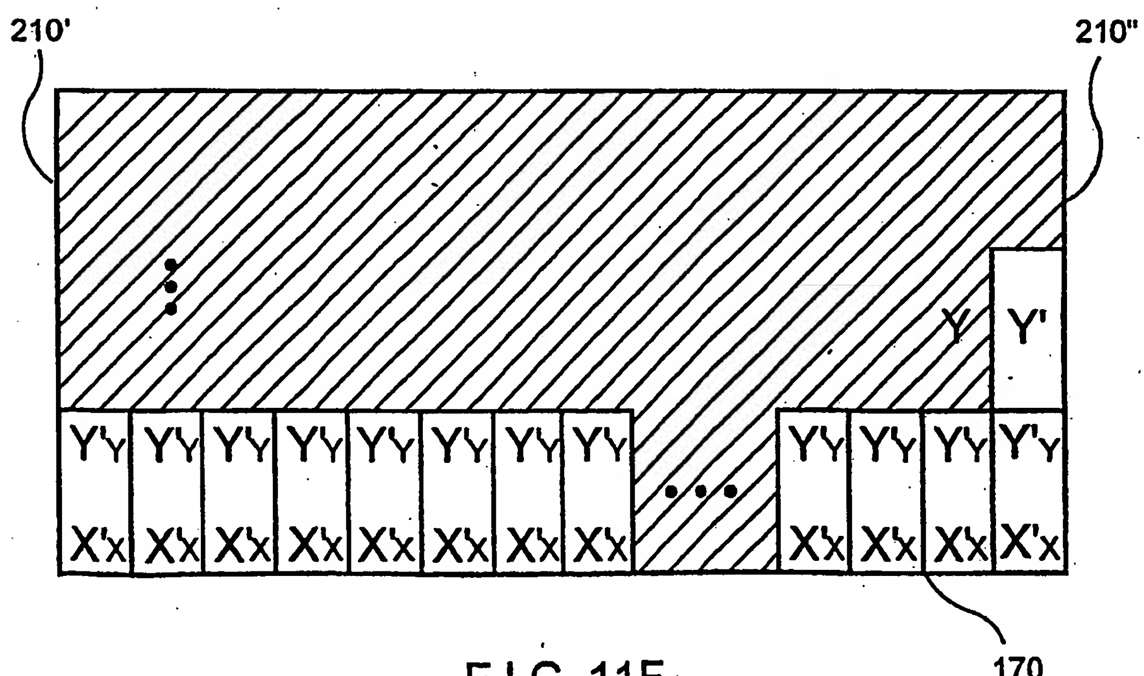


FIG. 11F

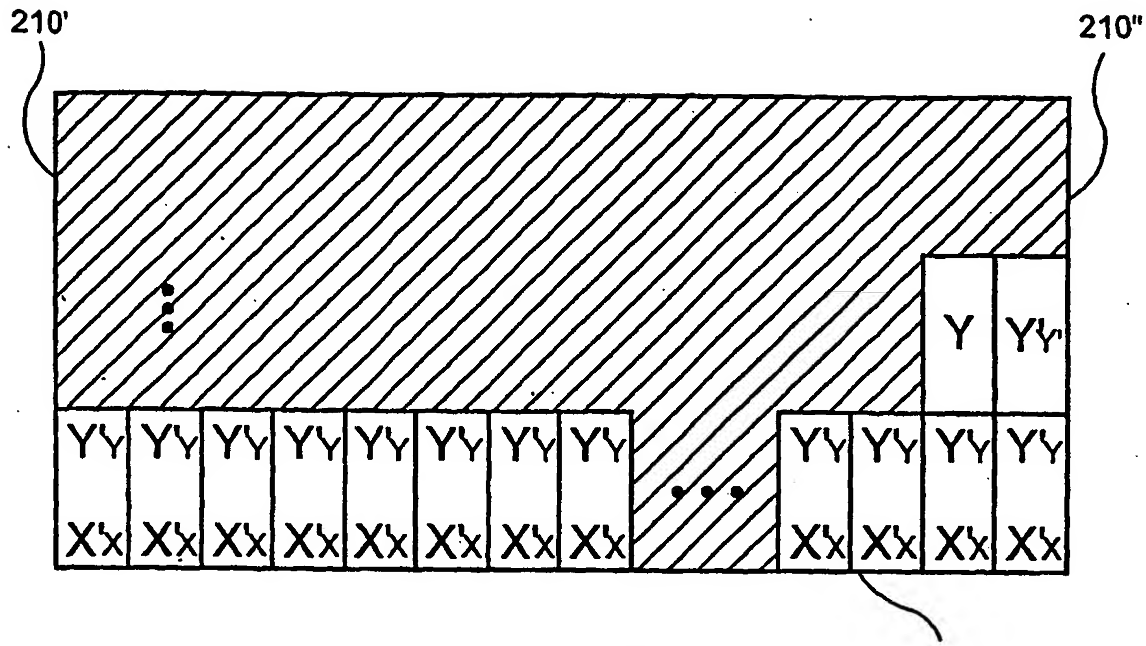


FIG. 11G

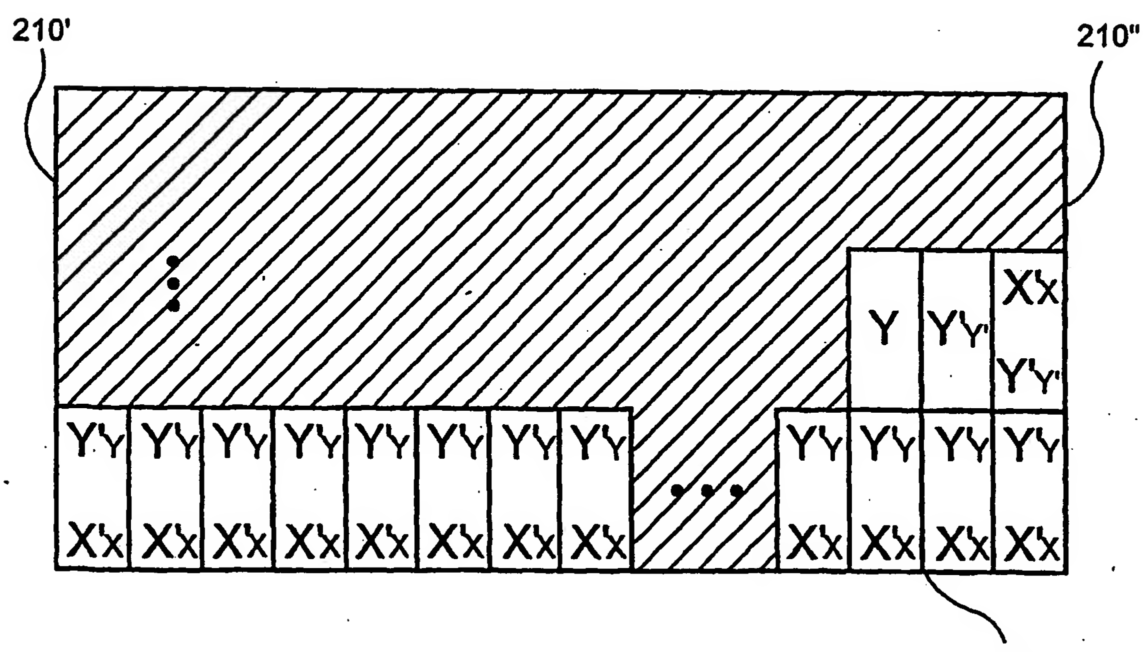


FIG. 11H

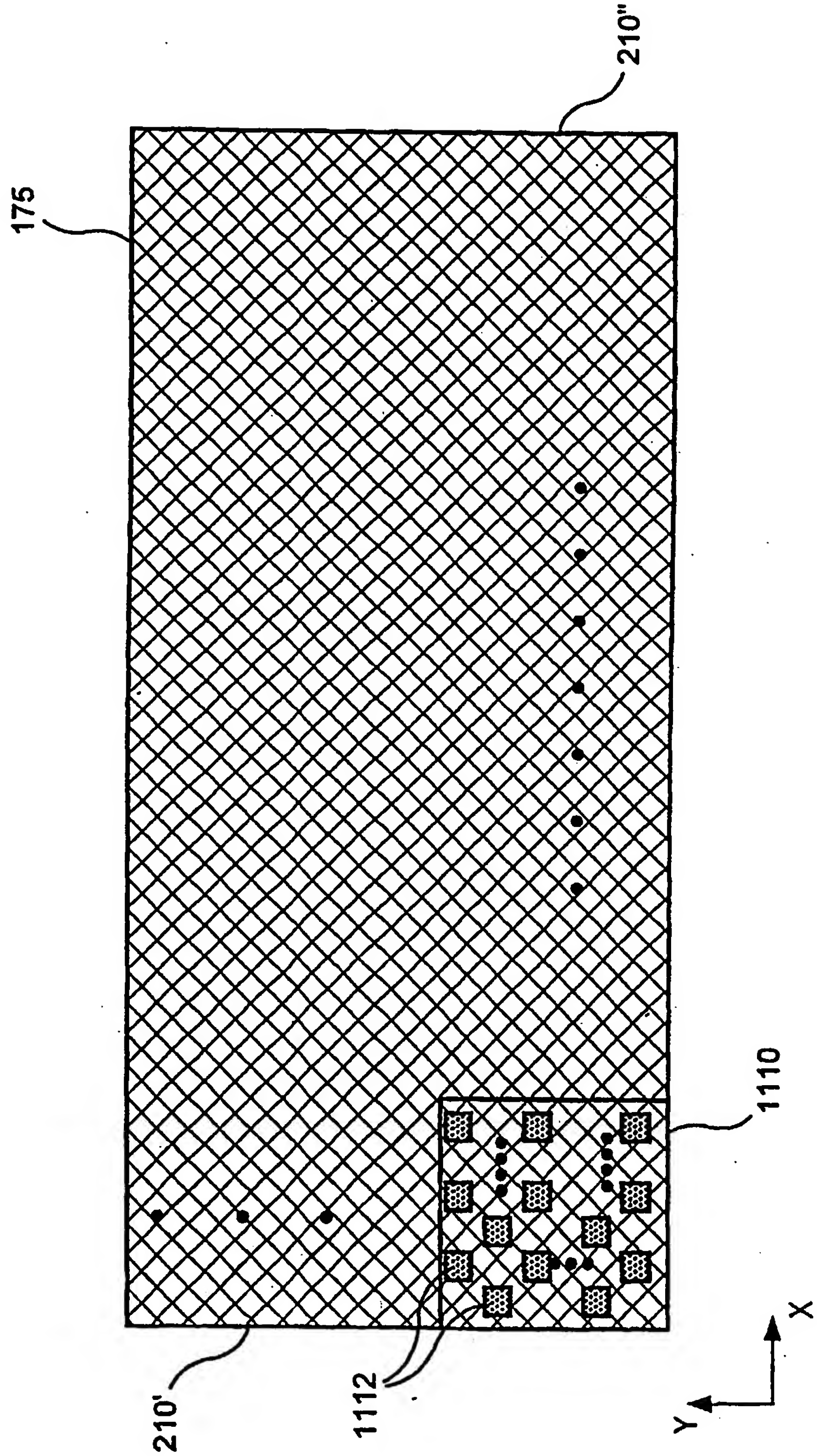


FIG. 12A

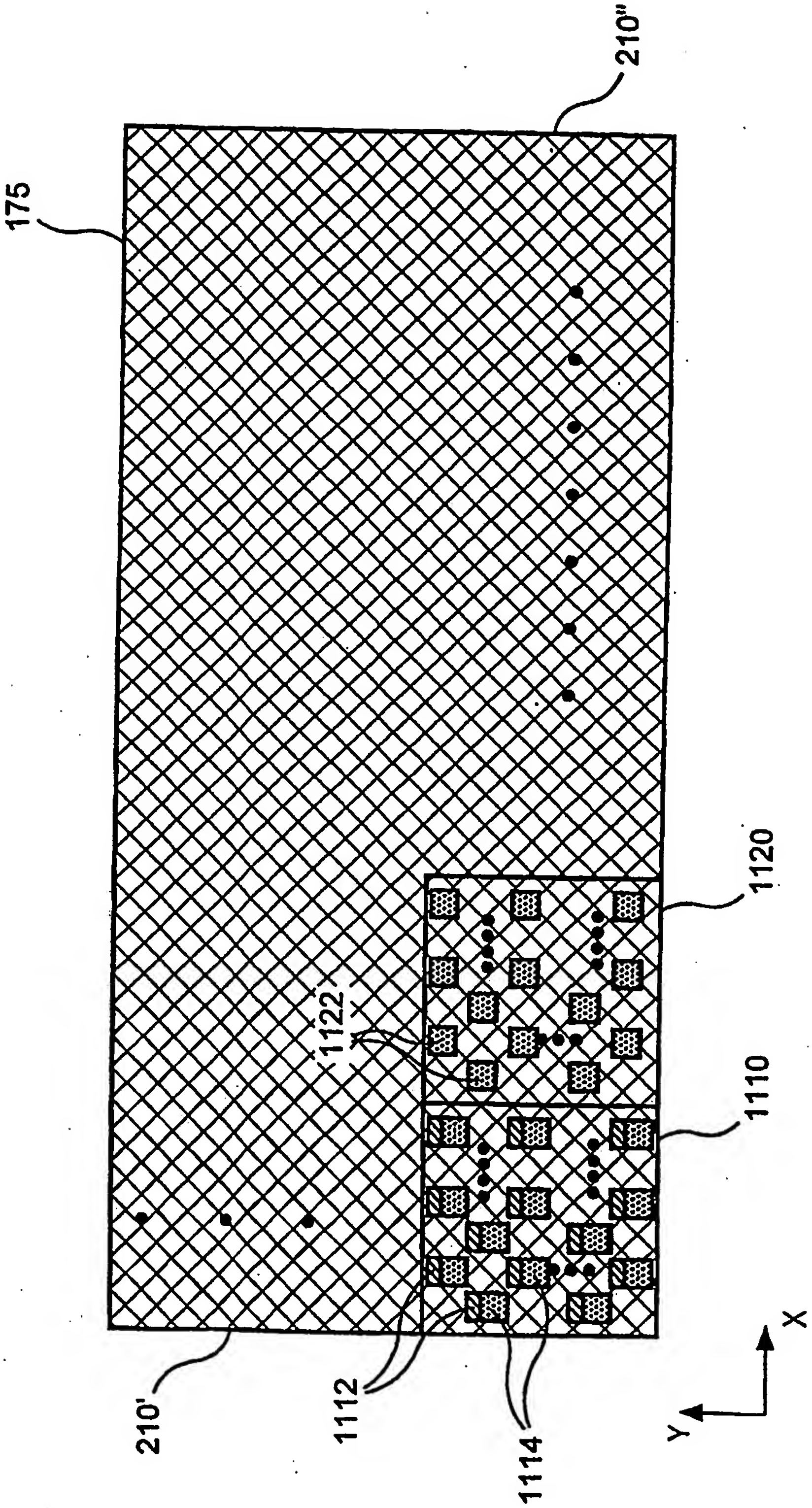
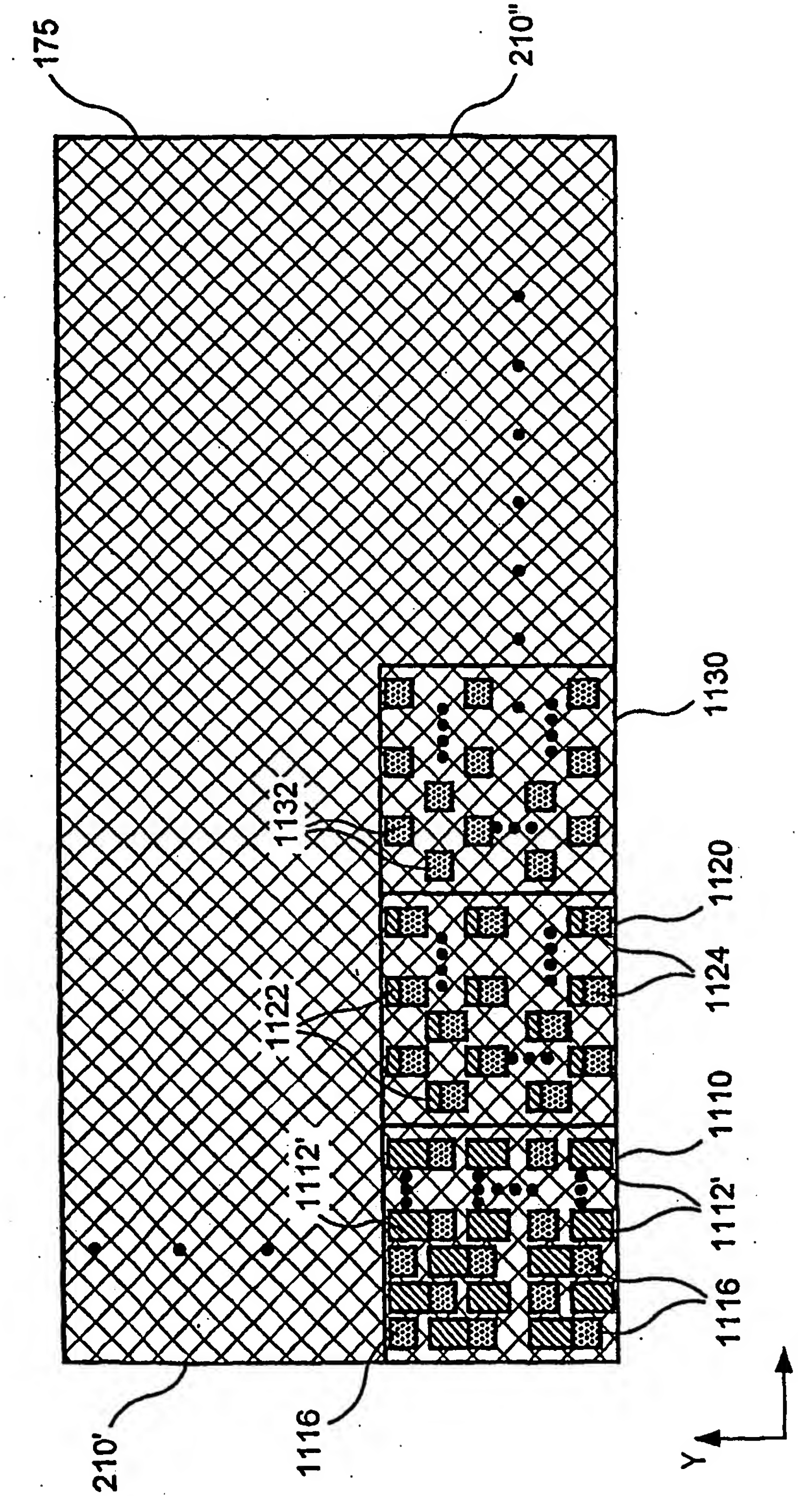
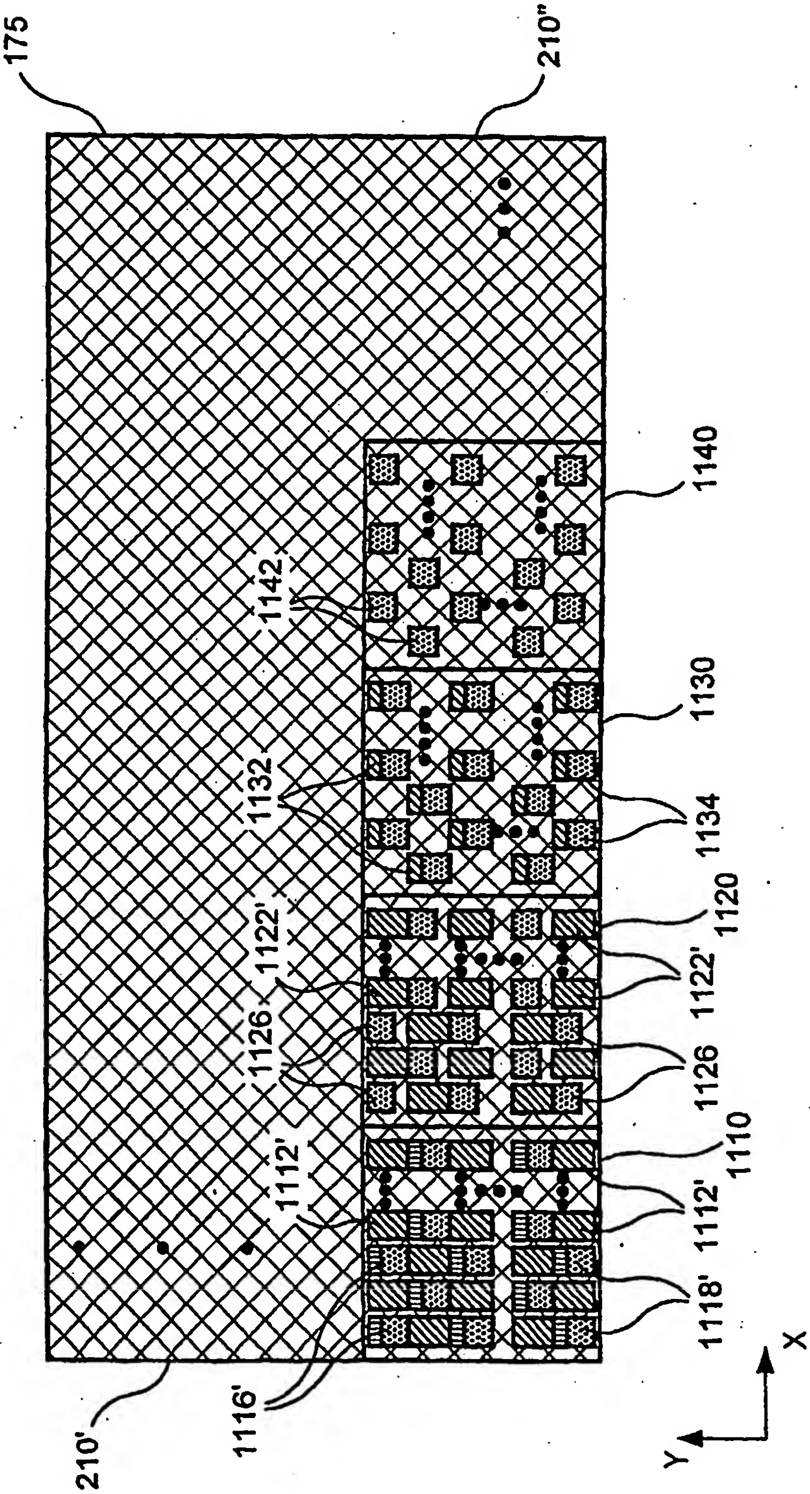


FIG. 12B


175
210"
1130
1132
1120
1124
1122
1110
1112'
1112'
1116
1116
210'
X
Y

F I G. 12C


175
210"
1140
1142
1130
1132
1134
1120
1122'
1126
1110
1112'
1118'
1116'
210'
X
Y

F I G. 12D

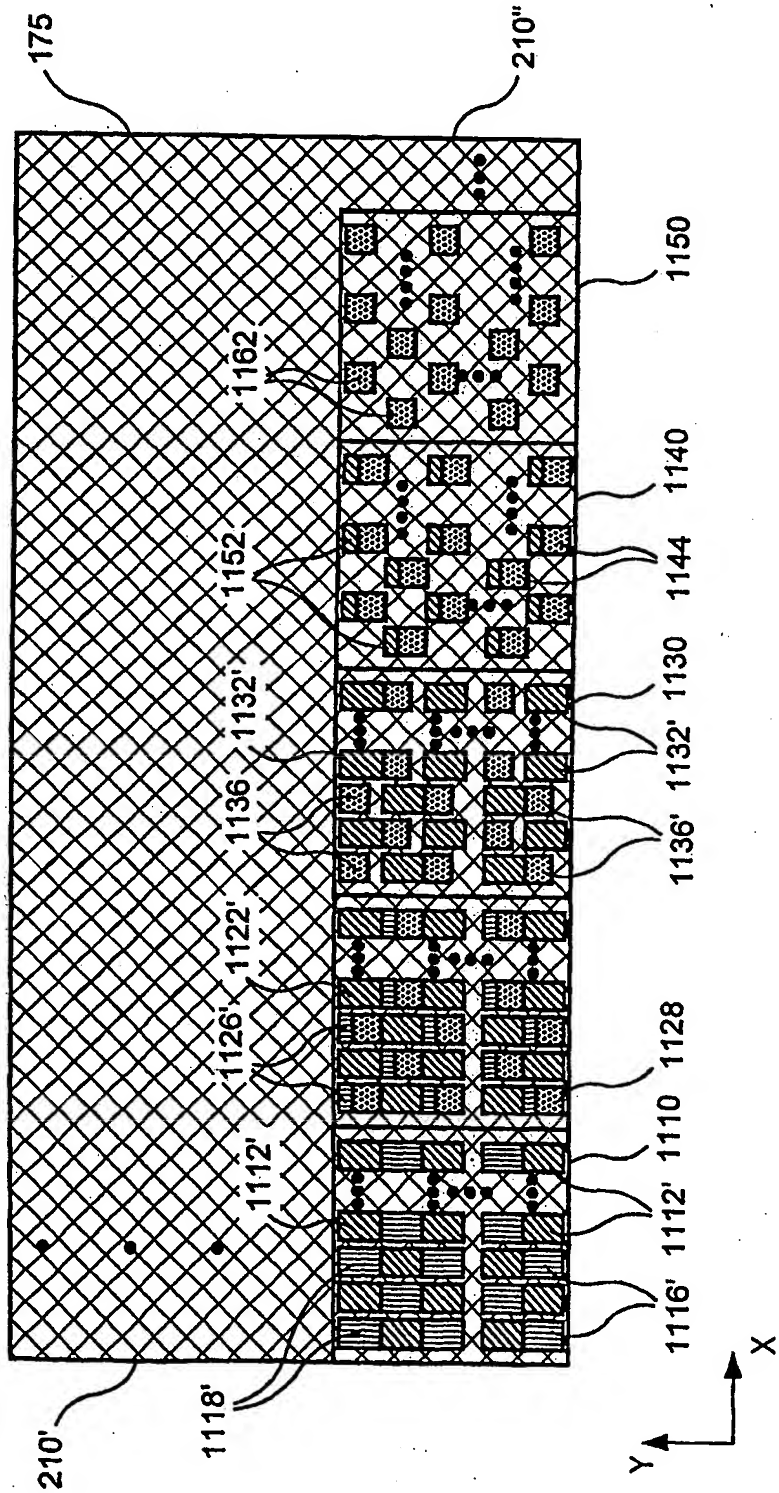

175
210"
1150
1162
1140
1152
1144
1132'
1130
1132'
1136
1136'
1122'
1126'
1128
1112'
1110
1112'
1116'
210'
1118'
X
Y

FIG. 12E

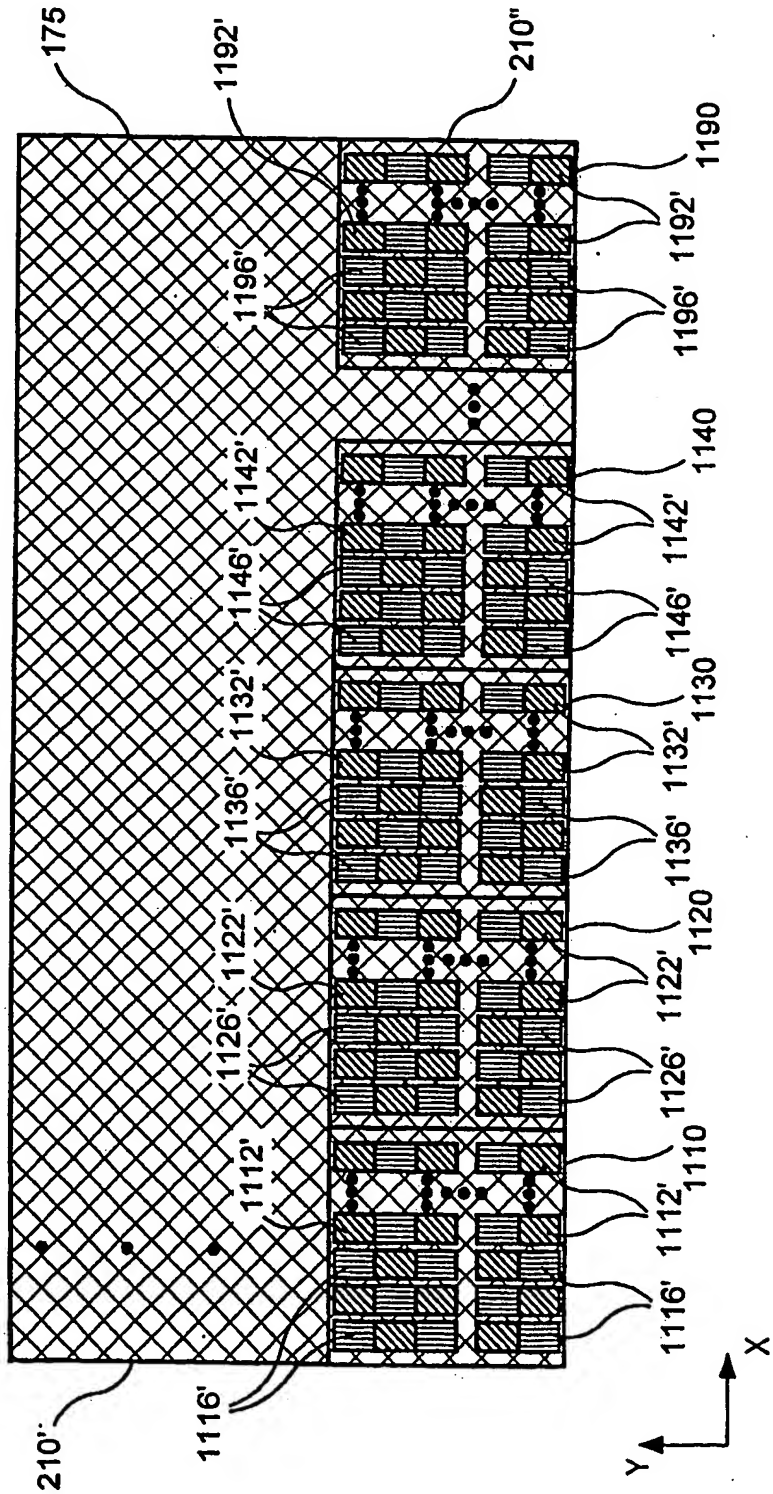

175
1192'
210''
1190
1192'
1196'
1196'
1140
1142'
1142'
1146'
1146'
1130
1132'
1132'
1136'
1136'
1120
1122'
1122'
1126'
1126'
1110
1112'
1112'
1116'
1116'
210''
X
Y

FIG. 12F

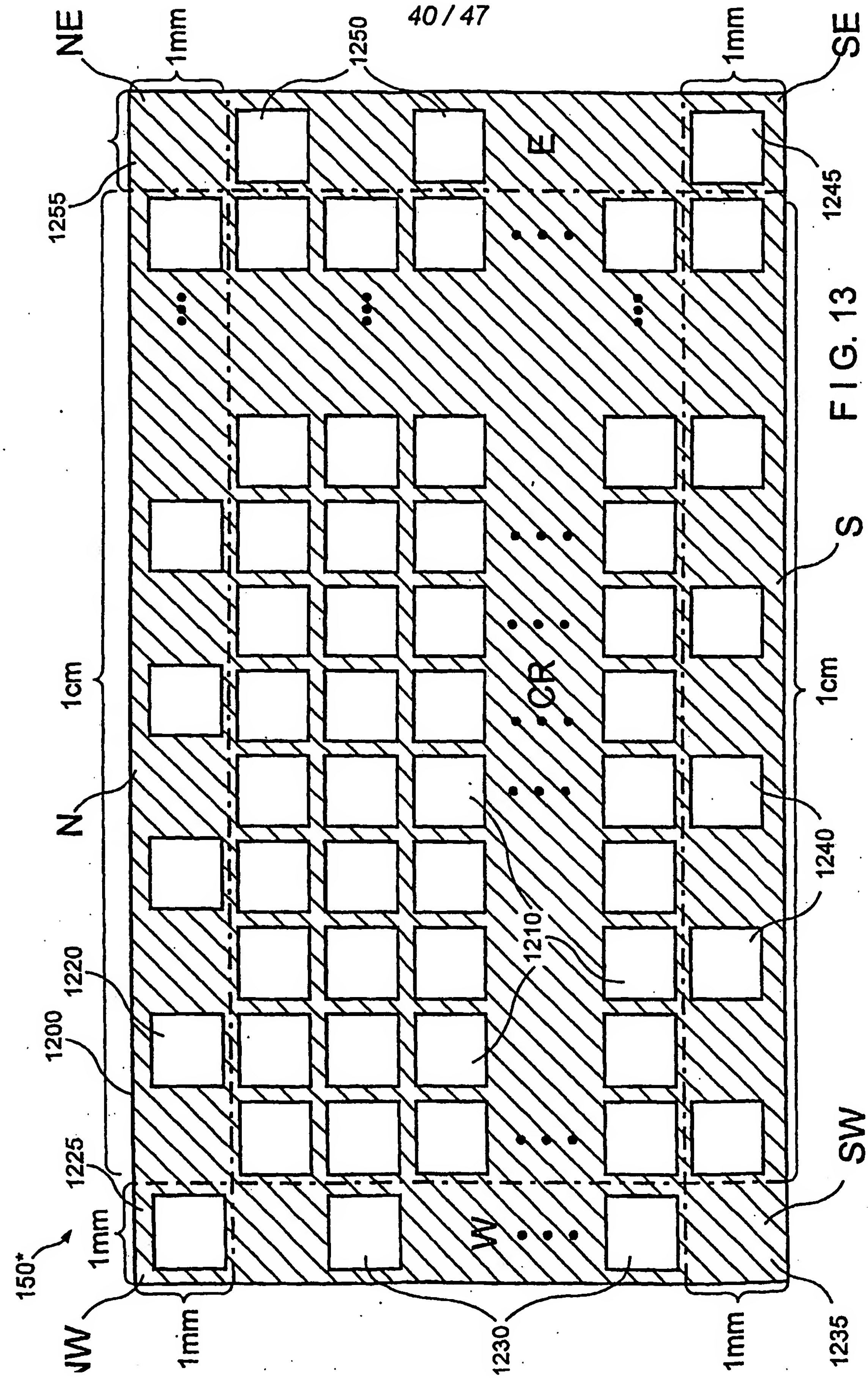

NE
1mm
1250
1mm
SE
E
1255
1245
1cm
1cm
S
CR
N
1240
1210
1220
1200
1225
SW
W
150*
1mm
NW
1mm
1230
1mm
1235

FIG. 13

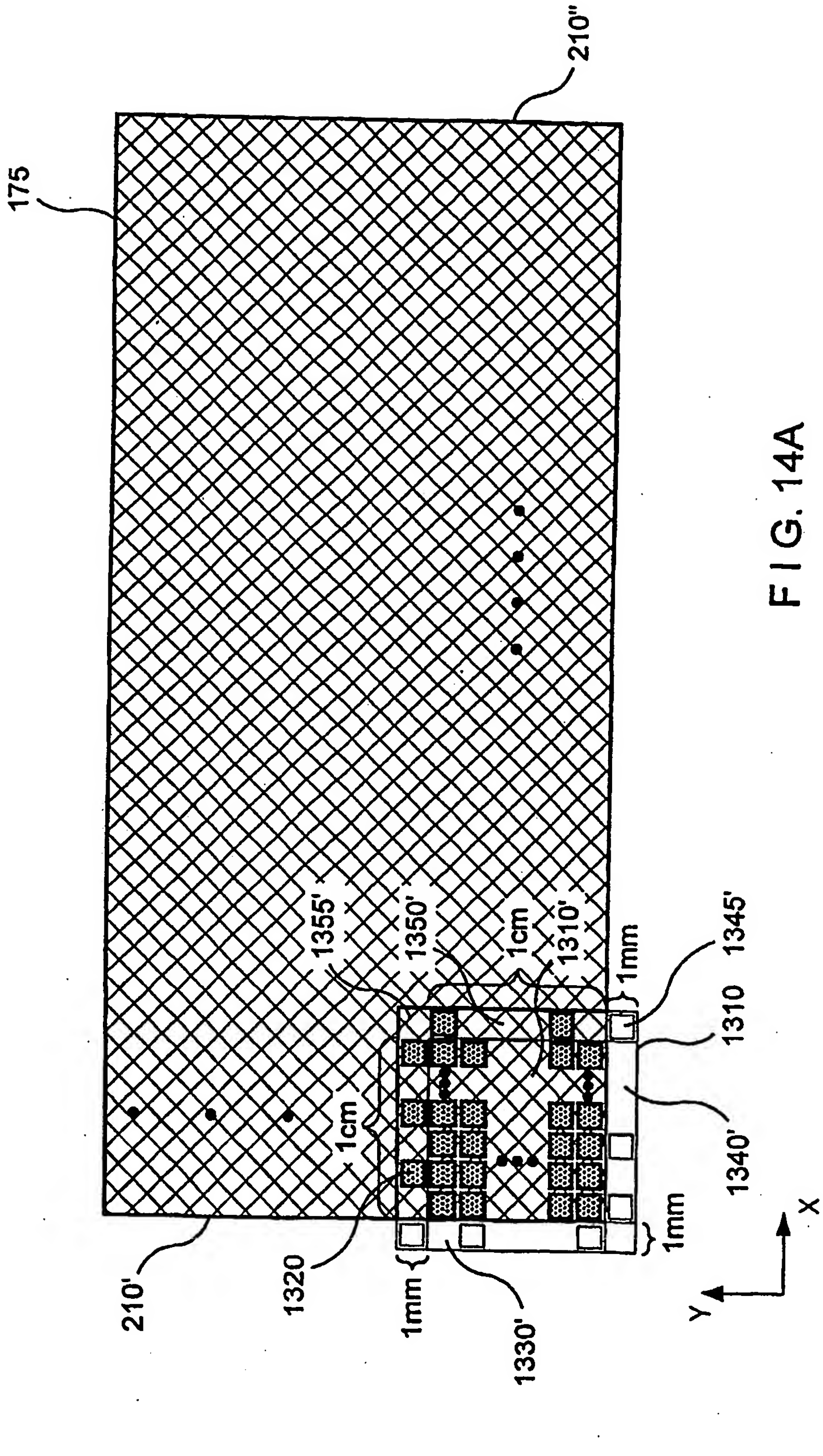

210"
175
1355'
1350'
1cm
1310'
1mm
1345'
1310
1340'
1cm
1mm
X
Y
210'
1320
1mm
1330'

FIG. 14A

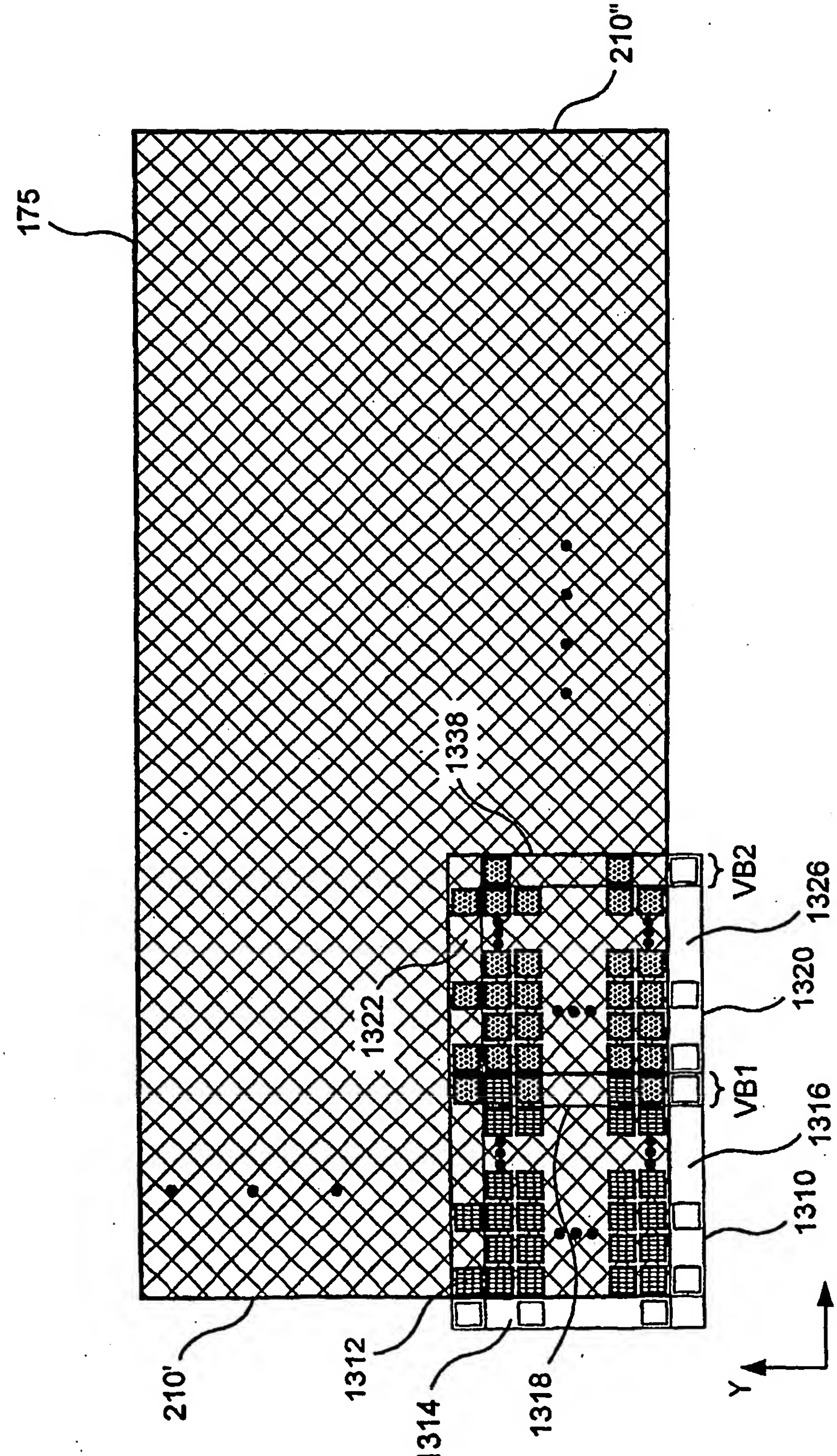

175
210"
210'
1312
1314
1318
1310
1316
1320
1322
1326
1338
VB1
VB2
X
Y

FIG. 14B

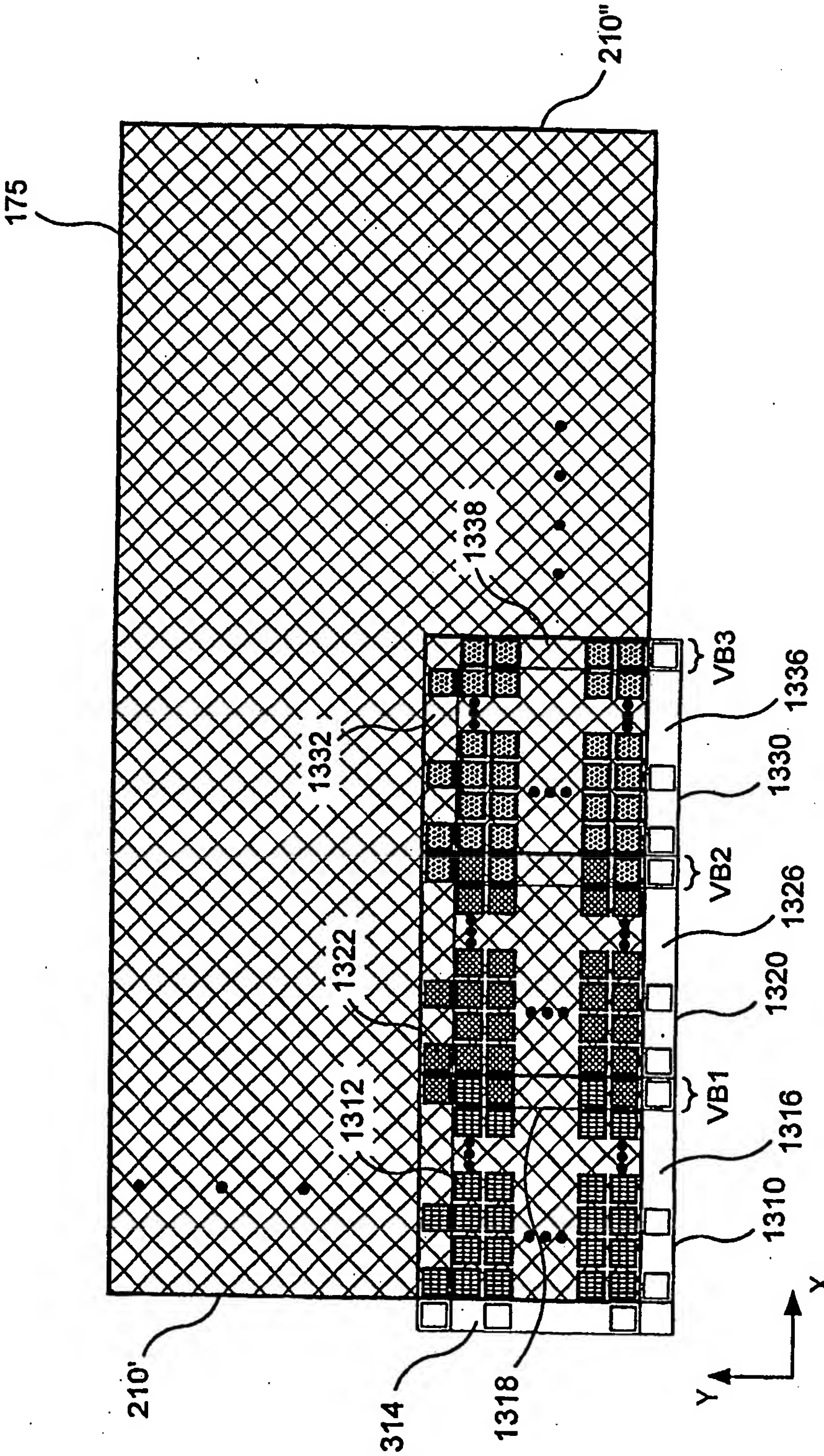

210"
175
1338
VB3
1336
1332
1330
VB2
1326
1322
1320
1312
VB1
1316
1310
210'
1314
1318
X
Y

FIG. 14C

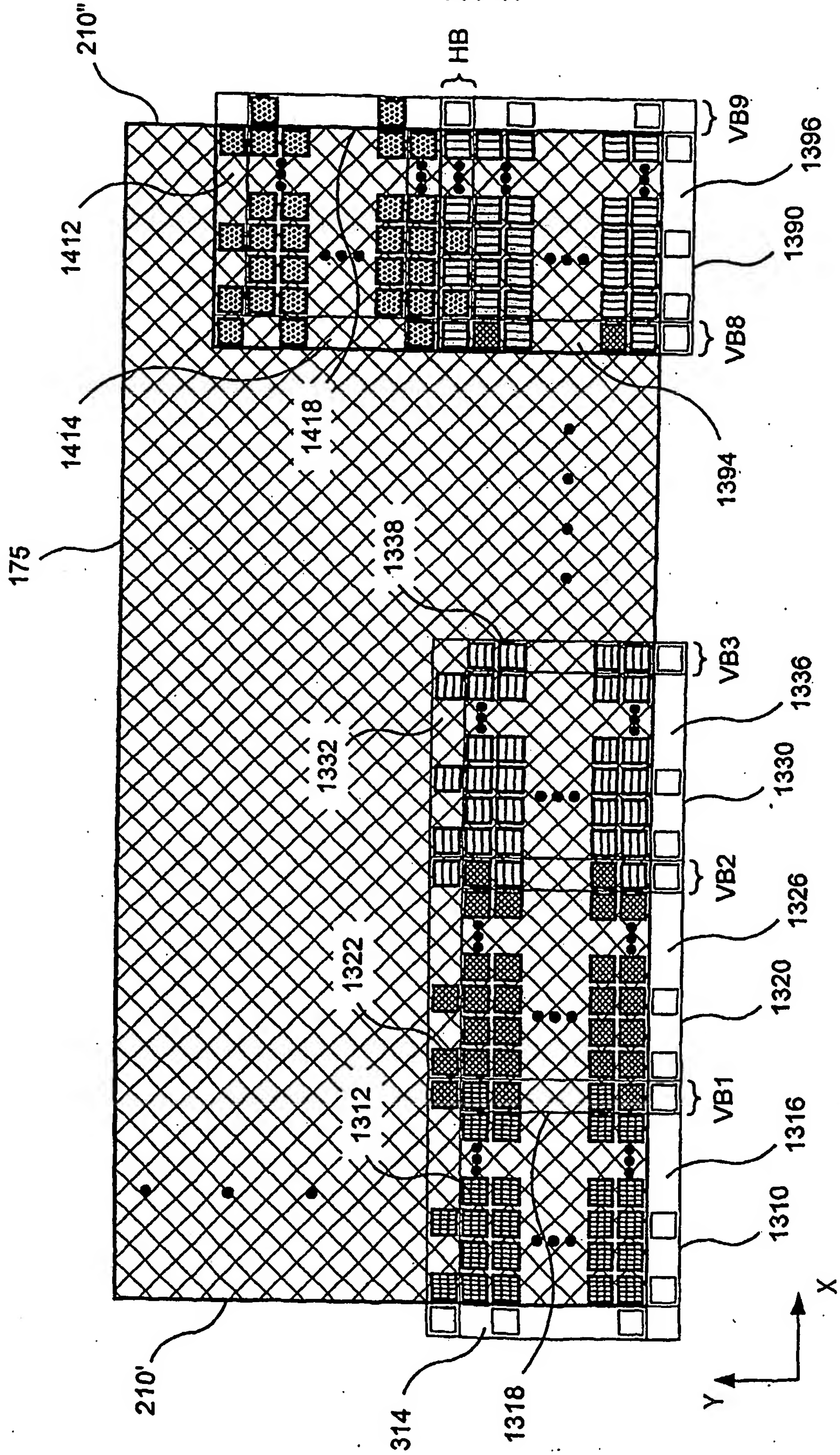

210"
HB
VB9
1396
1390
VB8
1412
1414
1418
1394
175
1338
VB3
1336
1332
1330
VB2
1326
1322
1320
VB1
1316
1312
1310
210'
314
1318
X
Y

FIG. 14D

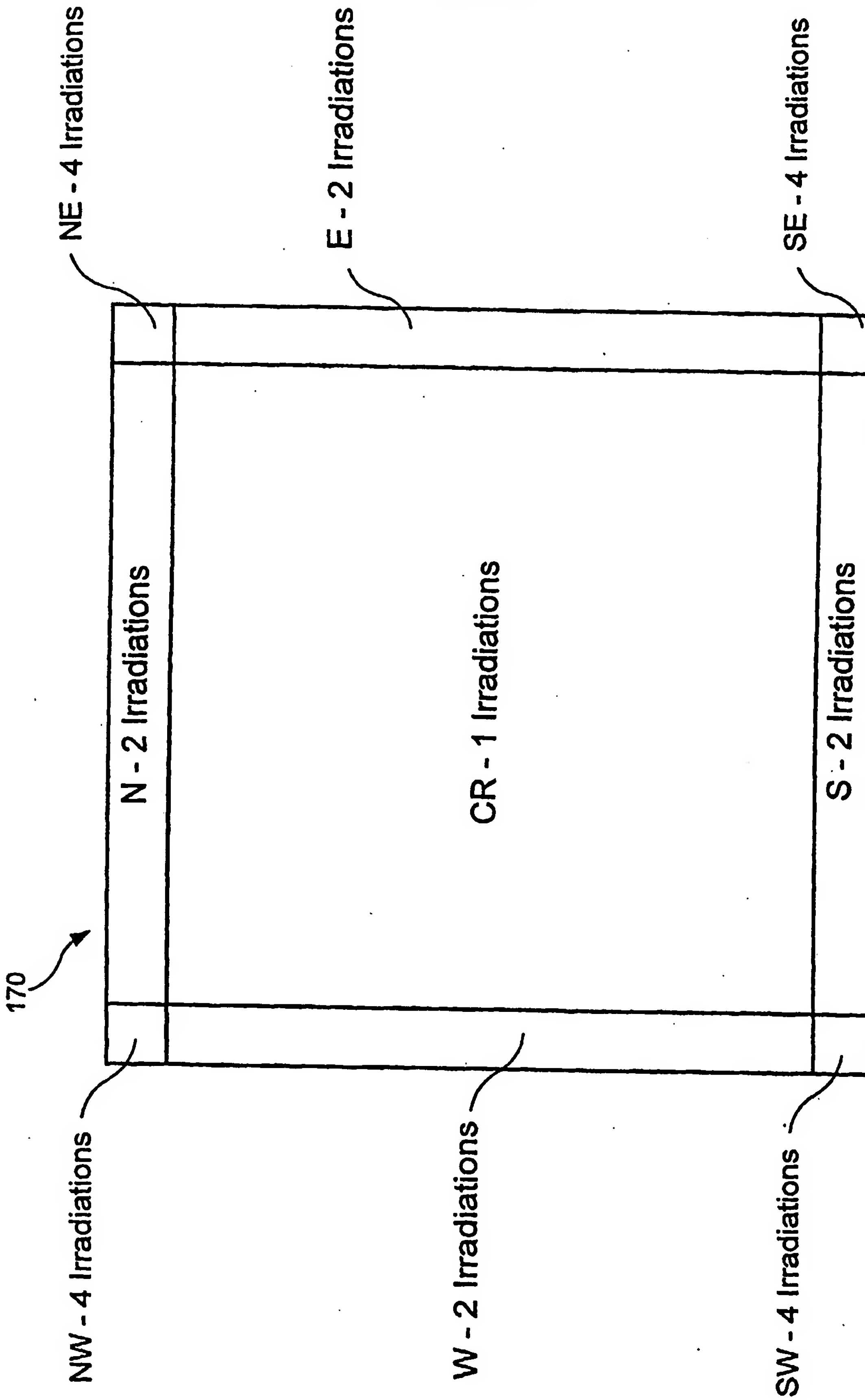

NE - 4 Irradiations
E - 2 Irradiations
SE - 4 Irradiations
N - 2 Irradiations
CR - 1 Irradiations
S - 2 Irradiations
170
NW - 4 Irradiations
W - 2 Irradiations
SW - 4 Irradiations

FIG. 15

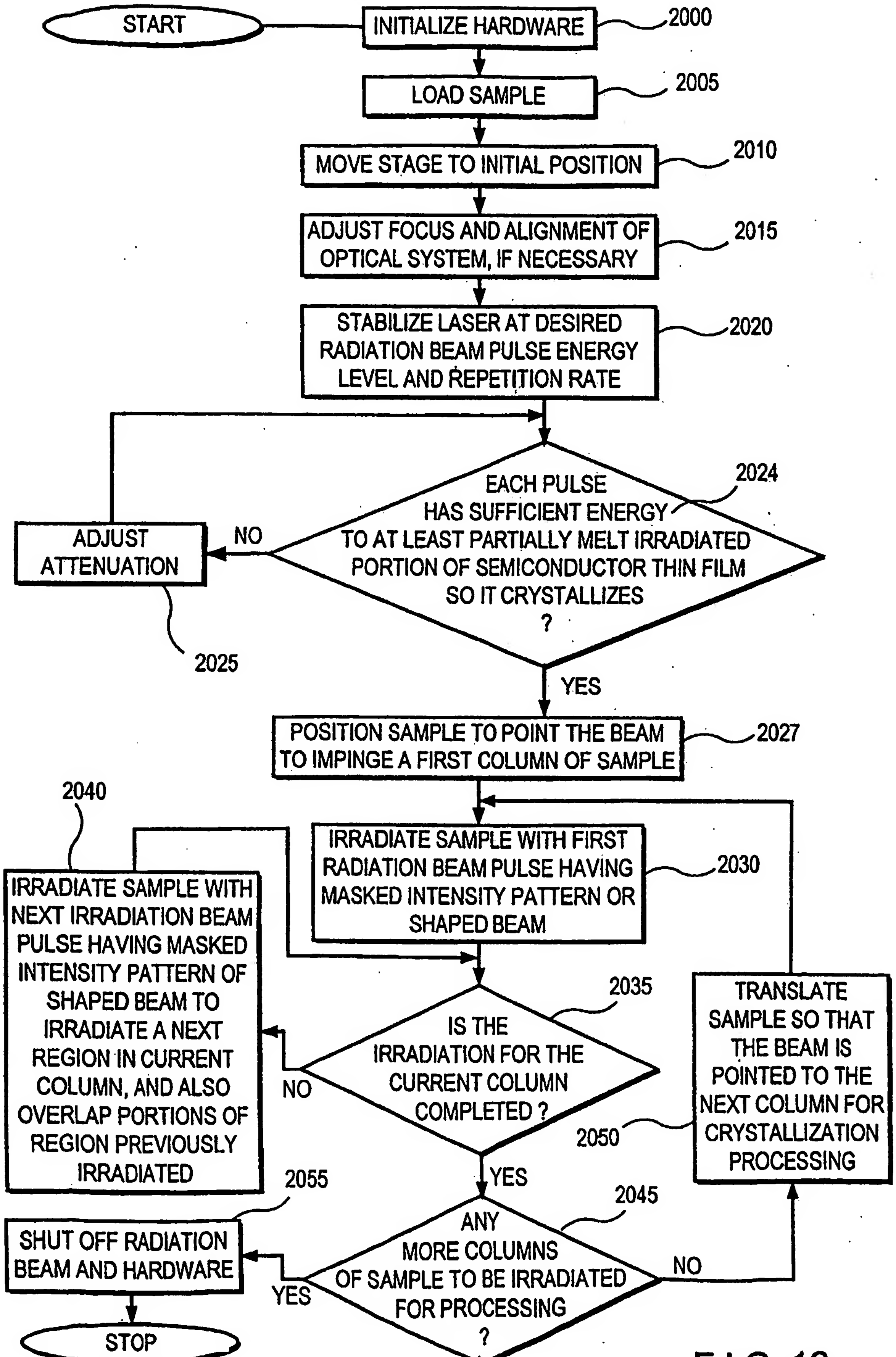

START
INITIALIZE HARDWARE
2000
LOAD SAMPLE
2005
MOVE STAGE TO INITIAL POSITION
2010
ADJUST FOCUS AND ALIGNMENT OF OPTICAL SYSTEM, IF NECESSARY
2015
STABILIZE LASER AT DESIRED RADIATION BEAM PULSE ENERGY LEVEL AND REPETITION RATE
2020
EACH PULSE HAS SUFFICIENT ENERGY TO AT LEAST PARTIALLY MELT IRRADIATED PORTION OF SEMICONDUCTOR THIN FILM SO IT CRYSTALLIZES ?
2024
NO
ADJUST ATTENUATION
2025
YES
POSITION SAMPLE TO POINT THE BEAM TO IMPINGE A FIRST COLUMN OF SAMPLE
2027
IRRADIATE SAMPLE WITH FIRST RADIATION BEAM PULSE HAVING MASKED INTENSITY PATTERN OR SHAPED BEAM
2030
2040
IRRADIATE SAMPLE WITH NEXT IRRADIATION BEAM PULSE HAVING MASKED INTENSITY PATTERN OF SHAPED BEAM TO IRRADIATE A NEXT REGION IN CURRENT COLUMN, AND ALSO OVERLAP PORTIONS OF REGION PREVIOUSLY IRRADIATED
IS THE IRRADIATION FOR THE CURRENT COLUMN COMPLETED ?
2035
NO
YES
TRANSLATE SAMPLE SO THAT THE BEAM IS POINTED TO THE NEXT COLUMN FOR CRYSTALLIZATION PROCESSING
2050
ANY MORE COLUMNS OF SAMPLE TO BE IRRADIATED FOR PROCESSING ?
2045
NO
YES
SHUT OFF RADIATION BEAM AND HARDWARE
2055
STOP

FIG. 16

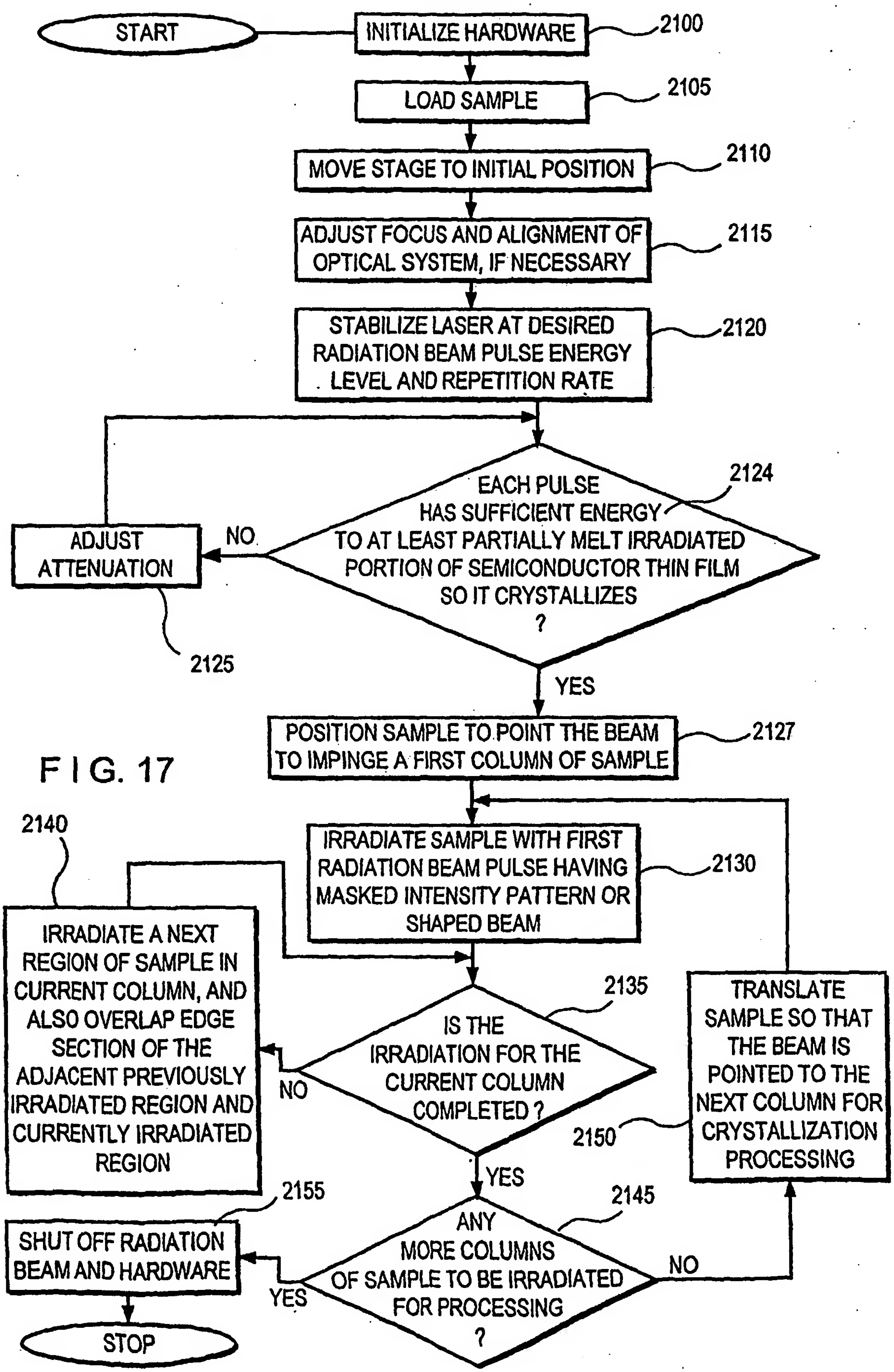

START
INITIALIZE HARDWARE
2100
LOAD SAMPLE
2105
MOVE STAGE TO INITIAL POSITION
2110
ADJUST FOCUS AND ALIGNMENT OF OPTICAL SYSTEM, IF NECESSARY
2115
STABILIZE LASER AT DESIRED RADIATION BEAM PULSE ENERGY LEVEL AND REPETITION RATE
2120
EACH PULSE HAS SUFFICIENT ENERGY TO AT LEAST PARTIALLY MELT IRRADIATED PORTION OF SEMICONDUCTOR THIN FILM SO IT CRYSTALLIZES ?
2124
NO
ADJUST ATTENUATION
2125
YES
POSITION SAMPLE TO POINT THE BEAM TO IMPINGE A FIRST COLUMN OF SAMPLE
2127
2140
IRRADIATE SAMPLE WITH FIRST RADIATION BEAM PULSE HAVING MASKED INTENSITY PATTERN OR SHAPED BEAM
2130
IRRADIATE A NEXT REGION OF SAMPLE IN CURRENT COLUMN, AND ALSO OVERLAP EDGE SECTION OF THE ADJACENT PREVIOUSLY IRRADIATED REGION AND CURRENTLY IRRADIATED REGION
IS THE IRRADIATION FOR THE CURRENT COLUMN COMPLETED ?
2135
NO
TRANSLATE SAMPLE SO THAT THE BEAM IS POINTED TO THE NEXT COLUMN FOR CRYSTALLIZATION PROCESSING
2150
YES
2155
2145
SHUT OFF RADIATION BEAM AND HARDWARE
ANY MORE COLUMNS OF SAMPLE TO BE IRRADIATED FOR PROCESSING ?
YES
NO
STOP

FIG. 17

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
2 September 2004 (02.09.2004)

PCT

(10) International Publication Number
WO 2004/075263 A2

(51) International Patent Classification[7]: H01L

(21) International Application Number: PCT/US2004/004929

(22) International Filing Date: 18 February 2004 (18.02.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/448,713 19 February 2003 (19.02.2003) US

(71) Applicant (*for all designated States except US*): THE TRUSTEES OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK [US/US]; 116th Street and Broadway, New York, NY 10027 (US).

(72) Inventor; and
(75) Inventor/Applicant (*for US only*): IM, James, S. [US/US]; 520 West 114th Street, Apt. 74, New York, NY 10027 (US).

(74) Agents: RAGUSA, Paul, A. et al.; Baker Botts LLP, 30 Rockefeller Plaza, New York, NY 10112-4498 (US).

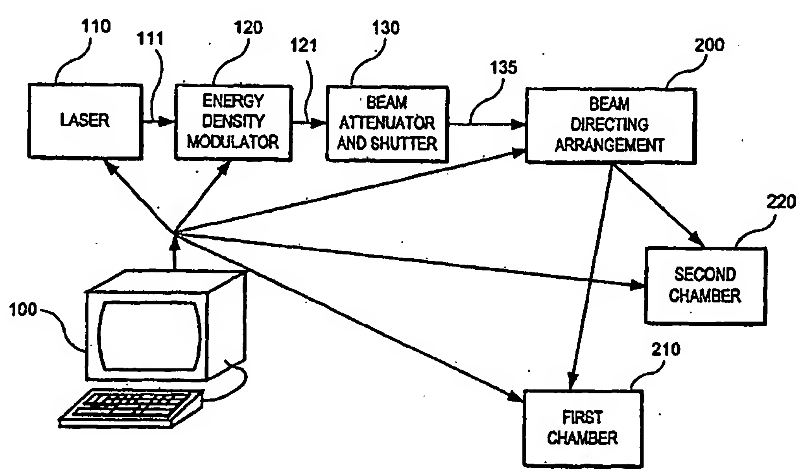
(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SYSTEM AND PROCESS FOR PROCESSING A PLURALITY OF SEMICONDUCTOR THIN FILMS WHICH ARE CRYSTALLIZED USING SEQUENTIAL LATERAL SOLIDIFICATION TECHNIQUES



(57) Abstract: A process and system are provided for processing at least one section of each of a plurality of semiconductor film samples. In these process and system, the irradiation beam source is controlled to emit successive irradiation beam pulses at a predetermined repetition rate. Using such emitted beam pulses, at least one section of one of the semiconductor film samples is irradiated using a first sequential lateral solidification ("SLS") technique and/or a first uniform small grained material ("UGS") techniques to process the such sections) of the first sample. Upon the completion of the processing of this section of the first sample, the beam pulses are redirected to impinge at least one section of a second sample of the semiconductor film samples. Then, using the redirected beam pulses, such sections) of the second sample are irradiated using a second SLS technique and/or a second UGS technique to process the at least one section of the second sample. The first and second techniques can be different from one another or substantially the same.

WO 2004/075263 A2

SYSTEM AND PROCESS FOR PROCESSING A PLURALITY OF SEMICONDUCTOR THIN FILMS WHICH ARE CRYSTALLIZED USING SEQUENTIAL LATERAL SOLIDIFICATION TECHNIQUES

SPECIFICATION

FIELD OF THE INVENTION

The present invention relates to a system and process for processing a plurality of semiconductor thin films (such as silicon thin films) using a pulse energy beam. In particular, one exemplary embodiment of the system and process utilizes a pulsed beam in conjunction with a sequential lateral solidification ("SLS") technique to irradiate at least two semiconductor thin films, without stopping the emission of energy the pulsed beam. Another exemplary embodiment of the system and process also uses a pulsed beam to irradiate sections of the film such that the areas that have been irradiated and resolidified which have small-grains therein do not overlap one another, and can be used to place therein thin film transistor ("TFT") devices.

BACKGROUND INFORMATION

Semiconductor films, such as silicon films, are known to be used for providing pixels for liquid crystal display devices. Such films have previously been processed (i.e., irradiated by an excimer laser and then crystallized) via excimer laser annealing ("ELA") techniques. However, the semiconductor films processed using such known ELA methods often suffer from microstructural non-uniformities such as edge effects, which manifest themselves in availing a non-uniform performance of thin-film transistor ("TFT") devices fabricated on such films. In addition, it may take approximately 200 second to 600 seconds to completely process the semiconductor film sample using the ELA techniques, without even taking into consideration the time it takes to load and unload such sample.

Other more advantageous processes and systems for processing the semiconductor thin films for use in the liquid crystal displays and organic light emitting diode displays for fabricating large grained single crystal or polycrystalline silicon thin films using sequential lateral solidification ("SLS") techniques have been described. For example, U.S. Patent Nos. 6,322,625 and 6,368,945 issued to Dr.

James Im, and U.S. patent application serial nos. 09/390,535 and 09/390,537, the entire disclosures of which are incorporated herein by reference, and which are assigned to the common assignee of the present application, describe such SLS systems and processes. These patent documents describe certain techniques in which one or more areas on the semiconductor thin film are, e.g., sequentially irradiated. One of the benefits of these SLS techniques is that the semiconductor film sample and/or sections thereof can be processed (e.g., crystallized) much faster that it would take for the processing the semiconductor film by the conventional ELA techniques. Typically, the processing/crystallization time of the semiconductor film sample depends on the type of the substrates, as well as other factors. For example, it is possible to completely process/crystallize the semiconductor film using the SLS techniques in approximately 50 to 100 seconds not considering the loading and unloading times of such samples.

In order to uniformly process the semiconductor films, it is important for the beam pulse to be stable. Thus, to achieve the optimal stability, it is preferable to pulse or fire the beam constantly, i.e., without stopping the pulsing of the beam. Such stability may be reduced or compromised when the pulsed beams are turned off or shut down, and then restarted. However, when the semiconductor sample is loaded and/or unloaded from a stage, the pulsed beam would be turned off, and then turned back on when the semiconductor sample to be processed was positioned at the designated location on the stage. The time for loading and unloading is generally referred to as a "transfer time." The transfer time for unloading the processed sample from the stage, and then loading another to-be-processed sample on the stage is generally the same when for the ELA techniques and the SLS techniques. Such transfer time can be between 50 and 100 seconds.

In addition, the costs associated with processing semiconductor samples are generally correlated with the number of pulses emitted by the beam source. In this manner, a "price per shot/pulse" is established. If the beam source is not shut down (i.e., still emit the beam pulses) when the next semiconductor sample is loaded unto the stage, or unloaded from the stage, the number of such irradiations by the beam source when the sample is not being irradiated by the beam pulse and corresponding time therefor is also taken into consideration for determining the price

per shot. For example, when utilizing the SLS techniques, the time of the irradiation, solidification and crystallization of the semiconductor sample is relatively short as compared to the sample processing time using the ELA techniques. In such case, approximately half of the beam pulses are not directed at the sample since such samples are being either loaded into the stage or unloaded from the stage. Therefore, the beam pulses that are not impinging the samples are wasted.

Another exemplary technique for processing semiconductor thin film has been developed. In particular, such system and process can produce generally uniform areas on the substrate films such that the TFT devices can be situated in such areas. For example, portions of the irradiated film are irradiated, then nucleated (based on the threshold behavior of the beam pulse), and then solidified, such that upon re-solidification, the nucleated area becomes a region with uniform small grained material (to be referred to herein below as the "UGS techniques"). Thus, such UGS techniques are different from the SLS techniques in that for the SLS-techniques, the nucleated areas are avoided, while for the UGS techniques, the nucleated areas are utilized for placing the TFT devices therein. Indeed, using the UGS technique, there can be significant time savings since each irradiated area of the semiconductor thin film is irradiated once, without the need to re-irradiate a substantial portion thereof, while still providing a good uniform material therein. Many of these UGS techniques are described in U.S. Patent Application Serial Nos. 60/405,084, 60/405,083 and 60/405,085, and International Applications PCT/US03/25946, PCT/US03/25972 and PCT/US03/25954, the entire disclosures of which are incorporated herein by reference.

Accordingly, it is preferable to reduce the price per shot, without stopping the emission of the beam pulses. It is also preferable to be able to process two or more semiconductor samples, without the need to stop or delay the emission of the pulsed beam by the beam source until the samples are loaded on the respective stages.

SUMMARY OF THE INVENTION

To achieve at least some of these objects, various systems and process according to the present invention are described below which can be utilized to, e.g., sequentially process a semiconductor (e.g., silicon) thin film sample (i.e., by irradiating and melting thin film of the sample, and allowing melted portions thereof to solidify and crystallize) on one stage, while unloading a previously-processed sample from another stage, and then loading an unprocessed sample thereon, without the need to shut down a pulsed beam. The exemplary embodiments of the systems and process for processing the samples in this manner shall be described in further detail below. However, it should be understood that the present invention is in no way limited to the exemplary embodiments of the systems and processes described herein.

One such exemplary embodiment of the process and system according to the present invention is provided for processing at least one section of each of a plurality of semiconductor film samples. With these process and system, the irradiation beam source can be controlled to emit successive irradiation beam pulses at a predetermined repetition rate. Using such emitted beam pulses, at least one section of one of the semiconductor film samples may be irradiated using at least one first sequential lateral solidification ("SLS") technique and/or at least one first uniform small grained material ("UGS") technique so as to process such section(s) of the first sample. Upon the completion of the processing of the section(s) of the first sample, the beam pulses can be redirected to impinge at least one section of a second sample of the semiconductor film samples. Then, using the redirected beam pulses, such section(s) of the second sample is irradiated using at least one second SLS technique and/or at least one second UGS technique to process the section(s) of the second sample. The first and second SLS and/or UGS techniques can be different from one another, or may be substantially the same.

According to another exemplary embodiment of the present invention, the second sample can be is an unprocessed sample. The first sample can be loaded on a stage of a first chamber, and the second sample may be loaded on a stage of the second chamber. In addition, during the irradiation of the first sample, a third sample

of the film samples that was previously irradiated and processed using the first SLS/UGS technique(s) and/or the second SLS/UGS technique(s) can be unloaded from the stage of the second chamber. Then, the second sample may be loaded unto the stage of the second chamber.

In yet another exemplary embodiment of the present invention, during the irradiation of the second sample, the first sample can be unloaded from the stage of the first chamber. Thereafter and during the irradiation of the second sample, a fourth unprocessed sample of the film samples may be loaded unto the stage of the first chamber. Upon the completion of the loading of the fourth sample, the beam pulse may again be redirected to impinge the section(s) of the fourth sample. After such redirection, such section(s) of the fourth sample can be irradiated using the first SLS/UGS technique(s) and/or the second SLS/UGS technique(s) so as to process the section(s) of the fourth sample.

According to still another exemplary embodiment of the present invention, the beam pulses can be redirected using a beam redirecting arrangement which may include a beam reflection device. Further, if is determined that the second sample has not been successfully loaded unto the stage of the second chamber, the irradiation of the second sample can be prevented or delayed until the second sample is successfully loaded unto the stage of the second chamber. If it is determined that the entire section(s) of the first sample was/were not successfully processed, the irradiation of the second sample can be prevented or delayed until the processing of all of the section(s) of the first sample has/have been successfully processed.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and its advantages, reference is now made to the following description, taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a schematic block diagram of an exemplary embodiment of a sequential-lateral solidification ("SLS") and/or uniform small grained material ("UGS") processing system according to the present invention which processes

semiconductor samples, sequentially, in two or more chambers using a beam directing arrangement;

Fig. 2 is a detailed illustration of an exemplary embodiment of one or more chambers shown in Fig. 1;

Fig. 3 is a detailed illustration of an exemplary embodiment of the beam directing arrangement of Fig. 1;

Fig. 4 is a top-level flow diagram of an exemplary embodiment of a process according to the present invention for sequentially SLS-processing or UGS-processing two or more samples, each being provided in its respective chamber; and

Fig. 5 is a detailed flow diagram of an exemplary embodiment of the process according to the present invention in which one sample on one stage is being processed, while previously SLS-processed or UGS-processed sample is removed from another stage and an unprocessed sample is loaded thereon.

DETAILED DESCRIPTION

Certain systems and processes for providing continuous motion SLS are described in U.S. Patent Nos. 6,322,625 and 6,368,945 and U.S. patent application serial nos. 09/390,535 and 09/390,537. In addition, systems and processes for providing uniform small grained materials ("UGS") techniques are described in U.S. Patent Application Serial Nos. 60/405,084, 60/405,083 and 60/405,085, and International Applications PCT/US03/25946, PCT/US03/25972 and PCT/US03/25954. Exemplary systems and processed according to the present invention can employ principles and components thereof to sequentially process a thin film of each of two or more semiconductor samples In particular, the system and process according to the present invention can be used to process two or more samples (provided on distinct stages). Each of the sample has an amorphous silicon thin film provided thereon.

In particular, as shown in Fig. 1, an exemplary embodiment of the system according to the present invention may include a beam source 110 (e.g., a Lambda Physik model LPX-315I XeCl pulsed excimer laser) emitting a pulsed irradiation beam (e.g., a laser beam), a controllable beam energy density modulator

120 for modifying the energy density of the irradiation beam, and a MicroLas two plate variable attenuator 130 (e.g., from MicroLas). It should be understood by those skilled in the art that instead of the beam source 110 (e.g., the pulsed excimer laser), it is possible to use a pulsed solid state laser, a chopped continuous wave laser, a pulsed electron beam and a pulsed ion beam, etc. Typically, the radiation beam pulses 111 generated by the beam source 110 provide a beam intensity in the range of 10 mJ/cm^2 to $1J/cm^2$, a pulse duration (FWHM) in the range of 10 to 300 nsec, and a pulse repetition rate in the range of 10 Hz to 300 Hz. The modulated beam pulses 135 exiting a beam attenuator and shutter 130 can be provided to a beam directing arrangement 200, which further directs the pulsed beam either to a first chamber 210 or to a second chamber 220. Exemplary details of such chambers 210, 220 shall be described below in further detail, with reference to Fig. 2.

Each of the first and second chambers 210, 220 is configured to be able to load therein the semiconductor sample prior to the thin film (or portion thereof) of such sample being irradiated and melted by the pulsed beam, solidified and then crystallized using one or more sequential lateral solidification ("SLS") and/or uniform small grained materials ("UGS") techniques. In addition, upon the completion of such processing of the semiconductor sample, each of these chambers 210, 220 can be configured to remove the SLS/UGS-processed sample therefrom, and load another unprocessed sample after the previously SLS-processed sample is removed.

The exemplary embodiment of the system illustrated in Fig. 1 also includes a processing arrangement 100 (e.g., a computer which includes a microprocessor executing instructions thereon, such as those implemented by software stored on its storage device or which is provided remotely therefrom). This processing arrangement 100 is communicably coupled to the beam source 110, the energy density modulator 120, and the beam attenuator and shutter 130. In this manner, the processing arrangement 100 can control the rate of the pulse of the beam being emitted by the beam source 110. The processing arrangement 100 can also control the repetition of the pulsed beam, as well as its modulation and attenuation (e.g., using arrangements 120, 130).

The processing arrangement 100 is further communicably coupled to the beam directing arrangement 200, the first chamber 210 and the second chamber 220. Such coupling by the processing arrangement 100 to first chamber 210 and the second chamber 220 provides information to the processing arrangement regarding whether the entire sample in the respective chamber has been completely crystallized using the particular SLS and/or UGS technique, if the previously processed sample has been unloaded from the chamber, and if the unprocessed sample has been loaded into such chamber. In addition, the processing arrangement 100 can control the loading and unloading of the sample into the chambers 210, 220.

With such information, the processing arrangement 100 can control the beam directing arrangement 200 to selectively direct the pulsed beam 135 toward the first chamber 210 or the second chamber, depending on the information obtained by the processing arrangements 100 from these chambers 210, 220. The details of the control by the processing arrangement 100 of the beam directing arrangement 200 based on such information shall be described in further detail below.

In exemplary operation of the system and process according to the present invention, the SLS and/or UGS processing of the sample in the first chamber 210 can be performed under the control of the processing arrangement 100 such that the pulsed beam 135 is provided by the beam directing arrangement 200 to the first chamber 210 so as to irradiate and crystallize the semiconductor sample therein. During such SLS-processing of the sample in the first chamber 210, the previously SLS-processed sample situated in the second chamber 220 is unloaded also under the control and direction of the processing arrangement 100, and a different, previously-unprocessed sample is loaded into this second chamber 220.

Upon the completion of the SLS and/or UGS processing of the sample in the first chamber 210, the processing arrangement 100 determines if the new unprocessed sample has been properly loaded into the second chamber 220 (e.g., unto a stage thereof). If that is the case, the processing arrangement 100 controls the beam directing arrangement 200 to direct the pulsed beam 135 toward the second chamber 220 so as to SLS-process and/or UGS-process the new sample that has been loaded into the second chamber 220. When the SLS-processing of this sample in the second

chamber 220 is commenced, the processing arrangement 100 controls the first chamber 210 (e.g., a stage thereof) to unload the SLS/UGS-processed sample therefrom, and then load another yet-unprocessed semiconductor sample into the first chamber 210. In this manner, while one sample is being processed in one chamber, another unprocessed sample is loaded to a further chamber to be SLS/UGS-processed immediately or shortly thereafter.

As described above, this exemplary procedure is effectuated, without shutting down the beam source 110, by re-directing the beam from the previously irradiated chamber to another chamber which has loaded therein the unprocessed sample so as to subsequently SLS/UGS-process such sample. This exemplary procedure continues until it is determined (either by the processing arrangement 100 and/or manually by an operator of the system) that the intended samples have been SLS/UGS-processed. At that time, the beam source 110 is shut down, and the loading/unloading of the samples in the first and second chambers 210, 220 can be stopped.

In this manner, the pulsed beam 135 is operated until all intended samples have been SLS-processed, without being shut down between the processing of the subsequent samples. Therefore, due to the fact the pulsed beam is not shut down by the beam source 110, such beam can be pulsed or shot continuously, and its stability would not be compromised. In addition, the loading and unloading time within of one chamber can be used to process a further semiconductor sample in another chamber so as to continuously process the samples in the chambers, and thus the price-per-shot achieved with these system and process of the present invention may be significantly smaller that the price-per-shot effectuated by the conventional systems.

Fig. 2 shows a detailed illustration of an exemplary embodiment of at least one of the chambers 210, 220 that are provided in Fig. 1. In particular, the exemplary chamber of Fig. 2 includes beam steering mirrors 140, 143, 147, 160 and 162, beam expanding and collimating lenses 141 and 142, a beam homogenizer 144, a condenser lens 145, a field lens 148, a projection mask 150 which may be mounted in a translating stage (not shown), a 4×-6× eye piece 161, a controllable shutter 152, a

multi-element 4× – 6× objective lens 163 for focusing a radiation beam pulse 164 onto the sample 170 having the semiconductor thin film to be processed mounted on a sample translation stage 180, and a granite block optical bench 190 supported on a vibration isolation and self-leveling system 191, 192, 193 and 194. The pulsed beam 135 is forwarded toward the chamber and to the beam steering mirror 140 by the beam directing arrangement 200

The computing arrangement 100 is communicably coupled to and the sample translation stage 180. As described in U.S. Patent Nos. 6,322,625 and 6,368,945, the sample translation stage 180 is preferably controlled by the processing arrangement 100 to effectuate translations of the sample 170 in the planar X-Y directions, as well as in the Z direction. In this manner, the processing arrangement 100 can control the relative position of the sample 170 with respect to the irradiation beam pulse 164 directed at the respective sample 170. In addition, the processing arrangement 100 can control the loading of the sample 170 to the translation stage 180, and unloading thereof from the translation stage 180, in the manner described herein above, and as shall further be described below.

Fig. 3 shows a detailed illustration of an exemplary embodiment of the beam directing arrangement 200 of Fig. 1. In particular, the beam directing arrangement 200 is designed so as to selectively direct the pulsed beam 135 toward a particular chamber, e.g., pursuant to the instructions of the processing arrangement 100. As described above, upon the completion of the SLS-processing of the sample 170 in the first chamber 210, the processing arrangement 100 may configure the beam directing arrangement 200 to direct the pulsed beam to the second chamber 220 so as to SLS-process the newly-loaded and previously unirradiated sample 170 that is provided on the translation stage 180 of the second chamber 220.

This can be accomplished by providing a beam reflecting member 250 (e.g., a mirror) in the beam directing arrangement 200 so that it would be able to selective control the path of the pulsed beam 135 (based on the instructions of the processing arrangement 100) toward the first chamber 210 or the second chamber 220. It should be understood by those skilled in the art that, either in addition or instead of the beam reflecting member 250, it is also possible to use other mechanical

components in the beam directing arrangement 200 to selectively direct the pulsed beam in the manner discussed above.

Fig. 4 shows a top-level flow diagram of an exemplary embodiment of a process according to the present invention for sequentially SLS-processing and/or UGS-processing two or more samples, with each sample being provided in the respective chamber. In step 1000, the hardware components of the system of Fig. 1, such as the beam source 110, the energy beam modulator 120, and the beam attenuator and shutter 130 are first initialized at least in part by the processing arrangement 100. The sample 170 is loaded onto the sample translation stage 180 of the first chamber in step 1005. It should be noted that such loading may be performed either manually or automatically using known sample loading apparatuses under the control of the processing arrangement 100. Next, the sample translation stage 180 of the first chamber 210 can be moved, preferably under the control of the computing arrangement 100, to an initial position in step 1010. Various other optical components of one or more of the chambers 210, 220 may be adjusted and/or aligned either manually or under the control of the processing arrangement 100 for a proper focus and alignment in step 1015, if necessary. In step 1020, the irradiation beam 111 can be stabilized at a predetermined pulse energy level, pulse duration and repetition rate.

Then, in step 1027, the entire sample 170 that is provided on the stage 180 of the first chamber 210 is irradiated according to one or more of the SLS-techniques and/or UGS-techniques described in the publications listed above until such sample is completely processed. Then, in step 1030, the processing arrangement 100 determines if the next unprocessed sample is available in the second chamber 220. In particular, it is determined if the next unprocessed sample 170 has been loaded into the translation stage 180 of the second chamber 220. If that is not the case, then the exemplary process according to the present invention waits until the sample 170 is loaded unto the stage 180 of the second chamber 220. Otherwise, in step 1035, the unprocessed sample 170 arranged on the translation stage 180 of the second chamber 220 is irradiated according to one or more of the SLS/UGS-techniques until it is completely processed.

Then, in step 1040, it is determined whether there are any further samples to be SLS-processed and/or UGS-processed. If so, in step 1045, the pulsed beam is directed to process another unprocessed sample that is loaded unto the translation stage 180 of the first chamber 210 (from which the previously SLS/UGS-processed sample has been unloaded), and the process according to the present invention returns to step 1030 for processing such unprocessed sample 170 that is provided in the first chamber 210, as described above. If, in step 1040, it is determined that there are no more samples to be processed, and the hardware components and the beam 111 of the system shown in Fig. 1 can be shut off in step 1050, and this process may be terminated.

Fig. 5 shows a detailed flow diagram of an exemplary embodiment of step 1035 of the process according to the present invention in which the sample 170 provided on one translation stage 170 of a particular chamber (e.g., the second chamber 220) is being SLS/UGS-processed, while previously SLS-processed sample 170 is unloaded from the translation stage 180 of another chamber (e.g., the first chamber 210), and an unprocessed sample is loaded thereon. In particular, while the sample 170 (provided in the second chamber 220) is being irradiated to be completely SLS/UGS-processed in step 2010, the previously SLS/UGS-processed sample 170 of the first chamber 210 is unloaded from this chamber 210 (step 2020), and then another unprocessed sample 170 is loaded unto the translation stage 180 of the first chamber 210 (step 2030). Step 2010 is preferably performed contemporaneously (or at least in the same time period) as steps 2020 and 2030.

Thereafter, it is determined, in step 2040, whether the SLS/UGS-processing of the sample 170 provided in the second chamber 220 being irradiated in step 2010 has been completed. If not, the process according to the present invention (preferably under the control of the processing arrangement 100) waits until the processing of such sample 170 is completed in the second chamber 220. Otherwise, it is determined, in step 2050, whether the new unprocessed sample 170 is loaded onto the translation stage 180 of the first chamber 210. If such unprocessed sample 170 has not yet been loaded, the pulsed beam is provided away from the completely SLS/UGS-processed sample 170 that is arranged in the second chamber 220 with the aid of the beam directing arrangement 200, and under the control of the processing

arrangement 100. This is performed without the need to shut down the beam source 110, thus not compromising the stability of the pulsed beam 135, 164. If it is determined that the unprocessed sample 170 has been loaded onto the translation stage 180 of the first chamber 210, the process according to the present invention continues to step 1040, directs the pulsed beam (using the beam directing arrangement 200 under the control of the processing arrangement 100) to irradiate and completely SLS-process the unprocessed sample 170 loaded onto the stage 180 of the first chamber 210.

It is to be understood that while the invention has been described in conjunction with the detailed description hereof, the foregoing description is intended to illustrate and not limit the scope of the invention. Other aspects, advantages, and modifications are within the scope of the present invention. In particular, other exemplary embodiments of the system and process according to the present invention can process the samples provided in more than two chambers. For such embodiments, the processing arrangement 100 may control the beam directing arrangement to selectively direct the pulsed beam 135 to each of these chambers when new unprocessed samples are loaded therein.

The foregoing merely illustrates the principles of the invention. Various modifications and alterations to the described embodiments will be apparent to those skilled in the art in view of the teachings herein. For example, while the above embodiment has been described with respect to at least partial lateral solidification and crystallization of the semiconductor thin film, it may apply to other materials processing techniques, such as micro-machining, photo-ablation, and micro-patterning techniques, including those described in International patent application no. PCT/US01/12799 and U.S. patent application serial nos. 09/390,535, 09/390,537 and 09/526,585, the entire disclosures of which are incorporated herein by reference. The various mask patterns and intensity beam patterns described in the above-referenced patent application can also be utilized with the process and system of the present invention. It will thus be appreciated that those skilled in the art will be able to devise numerous systems and methods which, although not explicitly shown or described herein, embody the principles of the invention and are thus within the spirit and scope of the present invention.

WHAT IS CLAIMED IS:

1. A process for processing at least one section of each of a plurality of semiconductor film samples, comprising the steps of:

(a) controlling an irradiation beam source to emit successive irradiation beam pulses at a predetermined repetition rate;

(b) using the emitted beam pulses, irradiating the at least one section of a first sample of the semiconductor film samples using at least one of a first sequential lateral solidification ("SLS") technique and a first uniform small grained material ("UGS") technique to process the at least one section of the first sample;

(c) upon the completion of step (b), redirecting the beam pulses to impinge the at least one section of a second sample of the semiconductor film samples; and

(d) using the redirected beam pulses, irradiating the at least one section of the second sample using at least one of a second SLS technique and second UGS techniques to process the at least one section of the second sample, the first and second techniques being one of different from one another and substantially the same.

2. The process according to claim 1, wherein the second sample is an unprocessed sample, wherein, in step (b), the first sample is loaded on a stage of a first chamber, wherein, in step (d), the second sample is provided on a stage of the second chamber.

3. The process according to claim 2, further comprising the steps of:

(e) during step (b), unloading a third sample of the film samples previously irradiated and processed using at least one of the first and second techniques from the stage of the second chamber; and

(f) during step (b), after step (e) and before step (d), loading the second sample unto the stage of the second chamber.

4. The process according to claim 3, further comprising the steps of:

(g) during step (d), unloading the first sample from the stage of the first chamber; and

(h) during step (d) and after step (g), loading a fourth unprocessed sample of the film samples unto the stage of the first chamber.

5. The process according to claim 4, further comprising the steps of:

(i) upon the completion of step (h), redirecting the beam pulses to impinge the at least one section of the fourth sample; and

(j) after step (i) and using the redirected beam pulses, irradiating the at least one section of the fourth sample using at least one of the first and second techniques to process the at least one section of the fourth sample.

6. The process according to claim 1, wherein the beam pulses are redirected in step (c) using a beam redirecting arrangement which includes a beam reflection device.

7. The process according to claim 3, further comprising the steps of:

(k) determining if the second sample successfully loaded unto the stage of the second chamber; and

(l) if step (k) produces an unsuccessful determination, preventing the irradiation of the second sample in step (d) until step (k) produces a successful result.

8. The process according to claim 1, further comprising the steps of:

(m) determining if all of the at least one section of the first sample was successfully processed in step (b); and

(n) if step (m) produces an unsuccessful determination, preventing the irradiation of the second sample in step (d) until step (k) produces a successful result.

9. A system for processing at least one section of each of a plurality of semiconductor film samples, comprising:

a processing arrangement which, when executing a set of instruction, is operable to:

(a) control an irradiation beam source to emit successive irradiation beam pulses at a predetermined repetition rate,

(b) using the emitted beam pulses, direct the beam pulse to irradiate the at least one section of a first sample of the semiconductor film samples using at least one of a first sequential lateral solidification ("SLS") technique and a first uniform small grained materials("UGS") technique to process the at least one section of the first sample,

(c) upon the completion of the processing of the at least one section of the first sample, effect a redirection of the beam pulses to impinge the at least one section of a second sample of the semiconductor film samples, and

(d) direct the redirected beam pulse to irradiate the at least one section of the second sample using at least one of a second SLS technique and a second UGS technique to process the at least one section of the second sample, the first and second techniques being one of different from one another and substantially the same.

10. The system according to claim 9, wherein the second sample is an unprocessed sample, wherein the processing arrangement is operable to load the first sample on a stage of a first chamber, wherein the processing arrangement is operable to load the second sample on a stage of the second chamber.

11. The system according to claim 10, wherein the processing arrangement is further operable to:

(e) during the irradiation of the first sample, effect an unloading of a third sample of the film samples previously irradiated and processed using at least one of the first and second techniques from the stage of the second chamber, and

(f) during the irradiation of the first sample and after the unloading of the second sample, effect a loading of the second sample unto the stage of the second chamber.

12. The system according to claim 11, wherein, the processing arrangement is further operable to:

(g) during the irradiation of the second sample, effecting the unloading the first sample from the stage of the first chamber, and

(h) during the irradiation of the second sample and after the unloading of the first sample, effect a loading of a fourth unprocessed sample of the film samples unto the stage of the first chamber.

13. The system according to claim 12, wherein the processing arrangement is further operable to:

(i) upon the completion of the loading of the fourth sample, effecting a redirection of the beam pulse to impinge the at least one section of the fourth sample, and

(j) after redirecting the beam pulses to impinge the at least one section of the fourth sample, directing the redirected beam pulses to irradiate the at least one section of the fourth sample using at least one of the first and second techniques to process the at least one section of the fourth sample.

14. The system according to claim 9, wherein the processing arrangement is operable to redirect the beam pulses a beam redirecting arrangement which includes a beam reflection device.

15. The system according to claim 11, wherein the processing arrangement is further operable to:

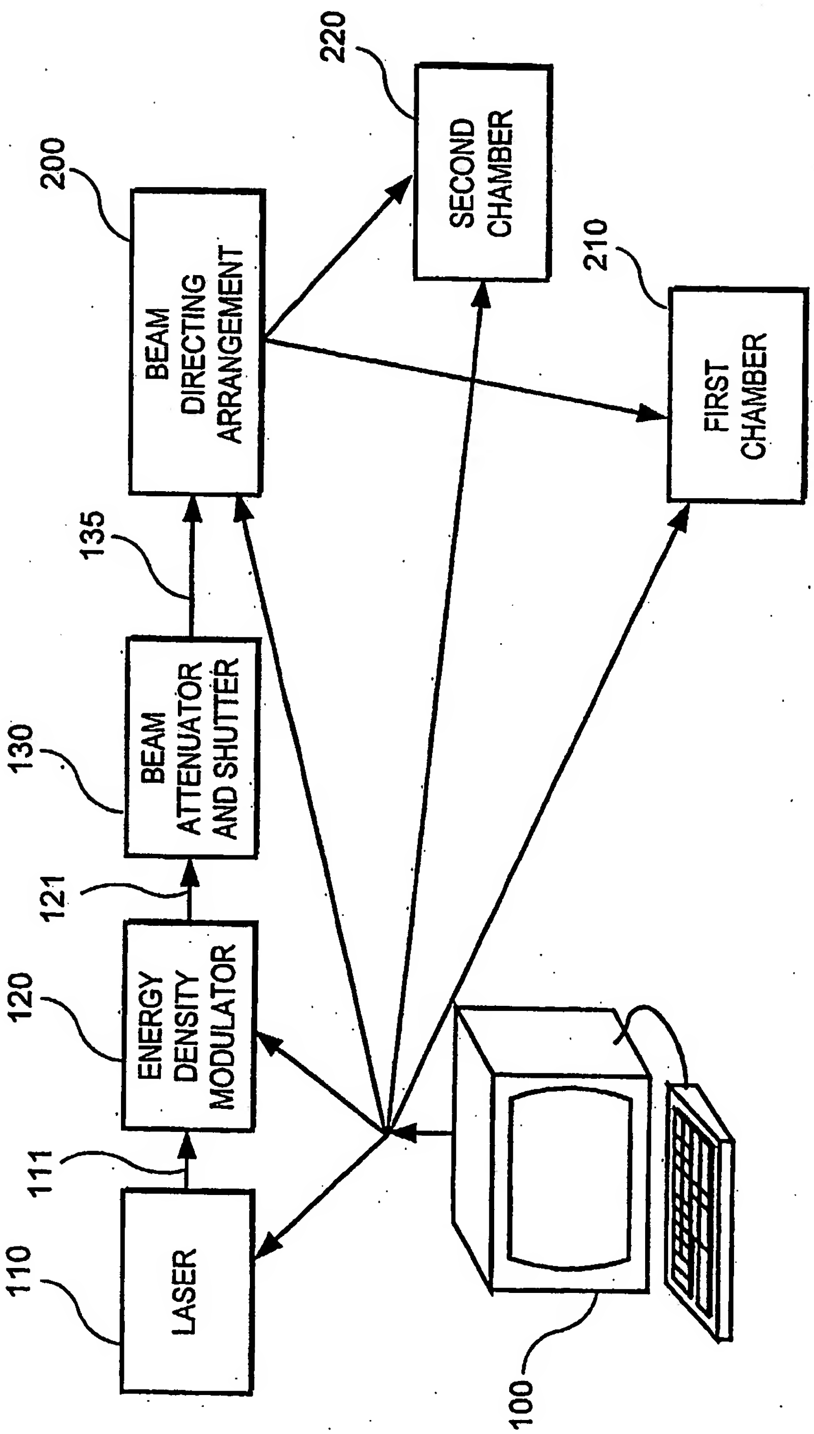
(k) determine if the second sample successfully loaded unto the stage of the second chamber, and

(l) if item (k) produces an unsuccessful determination, prevent the irradiation of the second sample in until the second sample is successfully loaded unto the stage of the second chamber.

16. The system according to claim 9, wherein the processing arrangement is further operable to:

(m) determine if all of the at least one section of the first sample was successfully processed; and

(n) if item (m) produces an unsuccessful determination, preventing the irradiation of the second sample until the processing of all of the at least one section of the first sample has been successfully processed.


100
110
LASER
111
120
ENERGY DENSITY MODULATOR
121
130
BEAM ATTENUATOR AND SHUTTER
135
200
BEAM DIRECTING ARRANGEMENT
210
FIRST CHAMBER
220
SECOND CHAMBER

F I G. 1

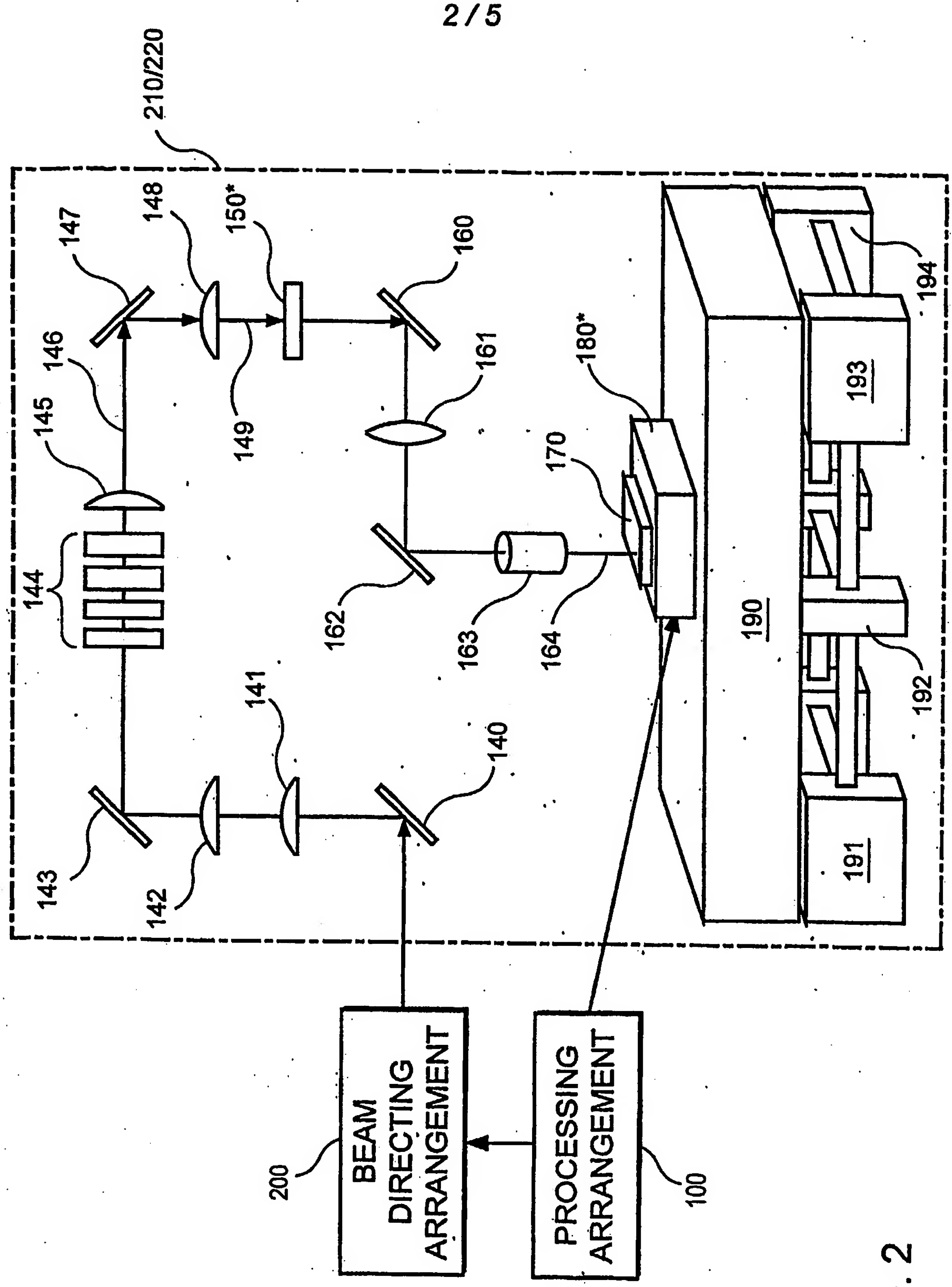

210/220
147
148
150*
160
146
145
149
161
180*
170
144
162
163
164
190
193
194
192
141
140
143
142
191
BEAM DIRECTING ARRANGEMENT
PROCESSING ARRANGEMENT
200
100

FIG. 2

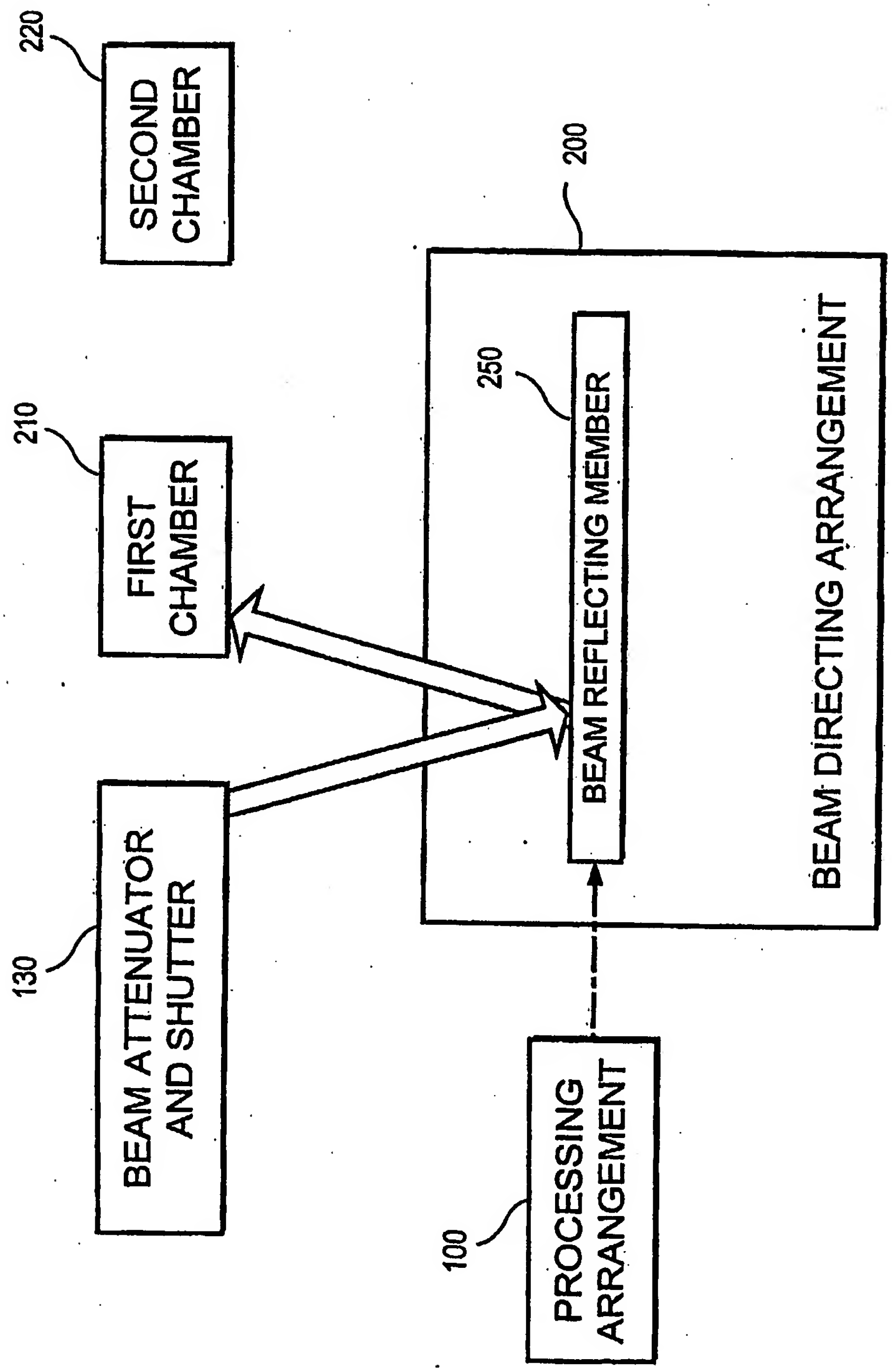

220
SECOND CHAMBER
210
FIRST CHAMBER
130
BEAM ATTENUATOR AND SHUTTER
200
250
BEAM REFLECTING MEMBER
BEAM DIRECTING ARRANGEMENT
100
PROCESSING ARRANGEMENT

FIG. 3

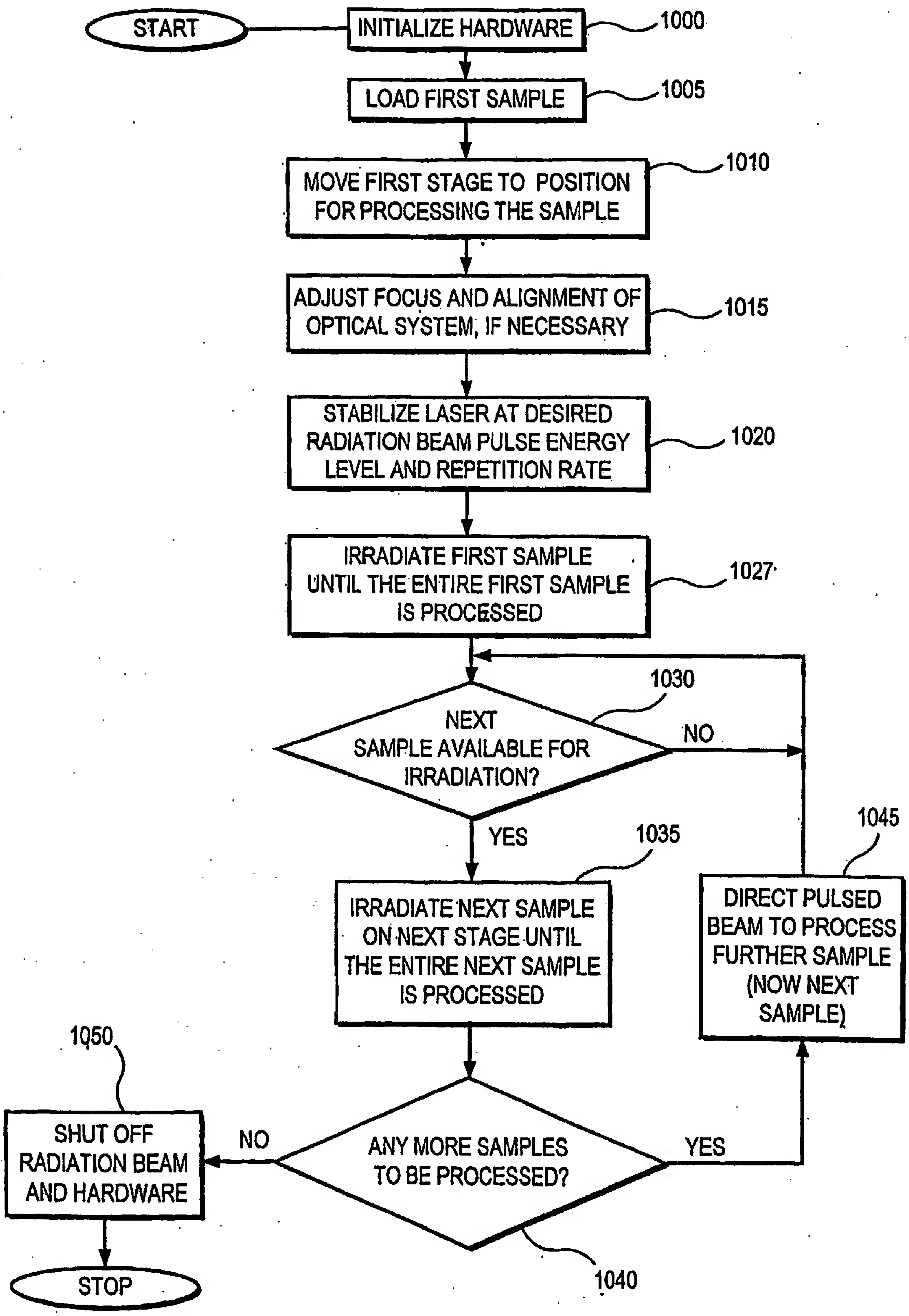

START
INITIALIZE HARDWARE
1000
LOAD FIRST SAMPLE
1005
MOVE FIRST STAGE TO POSITION FOR PROCESSING THE SAMPLE
1010
ADJUST FOCUS AND ALIGNMENT OF OPTICAL SYSTEM, IF NECESSARY
1015
STABILIZE LASER AT DESIRED RADIATION BEAM PULSE ENERGY LEVEL AND REPETITION RATE
1020
IRRADIATE FIRST SAMPLE UNTIL THE ENTIRE FIRST SAMPLE IS PROCESSED
1027
1030
NEXT SAMPLE AVAILABLE FOR IRRADIATION?
NO
YES
1035
IRRADIATE NEXT SAMPLE ON NEXT STAGE UNTIL THE ENTIRE NEXT SAMPLE IS PROCESSED
1045
DIRECT PULSED BEAM TO PROCESS FURTHER SAMPLE (NOW NEXT SAMPLE)
1050
SHUT OFF RADIATION BEAM AND HARDWARE
NO
ANY MORE SAMPLES TO BE PROCESSED?
YES
1040
STOP

FIG. 4

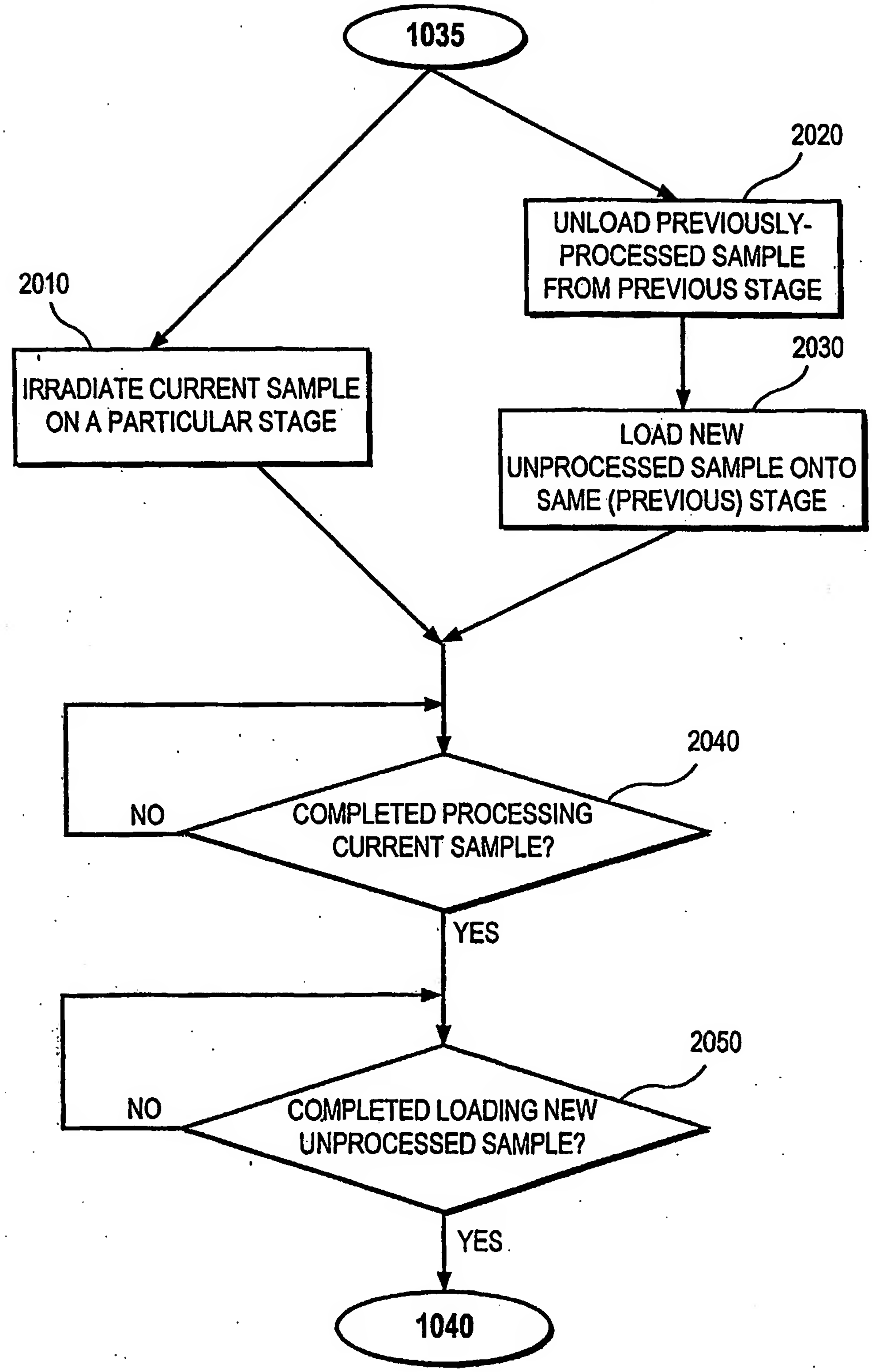

1035
2020
UNLOAD PREVIOUSLY-PROCESSED SAMPLE FROM PREVIOUS STAGE
2010
IRRADIATE CURRENT SAMPLE ON A PARTICULAR STAGE
2030
LOAD NEW UNPROCESSED SAMPLE ONTO SAME (PREVIOUS) STAGE
2040
NO
COMPLETED PROCESSING CURRENT SAMPLE?
YES
2050
NO
COMPLETED LOADING NEW UNPROCESSED SAMPLE?
YES
1040

FIG. 5

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G09G 3/36, H01L 21/20, 21/302, C30B 13/06

A1

(11) International Publication Number: WO 97/45827

(43) International Publication Date: 4 December 1997 (04.12.97)

(21) International Application Number: PCT/US96/07730

(22) International Filing Date: 28 May 1996 (28.05.96)

(81) Designated States: CA, JP, US.

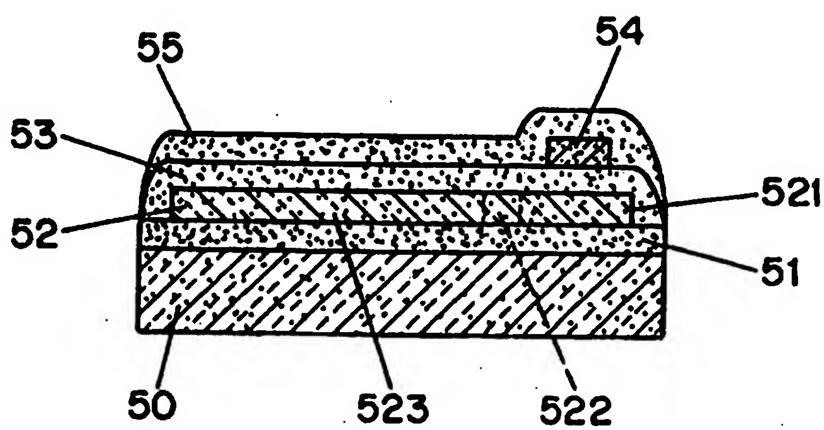
Published
With international search report.

(71) Applicant (*for all designated States except US*): THE TRUSTEES OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK [US/US]; Broadway & 116th Street, New York, NY 10027-6699 (US).

(72) Inventors; and
(75) Inventors/Applicants (*for US only*): IM, James, S. [US/US]; Apartment #74, 520 W. 114th Street, New York, NY 10027-6699 (US). SONG, Hyun, Jin [KR/US]; Apartment 3C, 500 W. 122nd Street, New York, NY 10027-6699 (US). SPOSILI, Robert, S. [US/US]; 63 Maria Lane, Yonkers, NY 10710-2007 (US). YOON, Jung, H. [KR/US]; Floor 2, 210 11th Street, Palisades Park, NJ 07650 (US).

(74) Agents: TANG, Henry et al.; Brumbaugh, Graves, Donohue & Raymond, 30 Rockefeller Plaza, New York, NY 10112 (US).

(54) Title: CRYSTALLIZATION PROCESSING OF SEMICONDUCTOR FILM REGIONS ON A SUBSTRATE, AND DEVICES MADE THEREWITH



(57) Abstract

Semiconductor integrated devices such as transistors are formed in a film of semiconductor material formed on a substrate. For improved device characteristics, the semiconductor material has regular, quasi-regular or single-crystal structure. Such a structure is made by a technique involving localized irradiation of the film with one or several pulses of a beam of laser radiation, locally to melt the film through its entire thickness. The molten material then solidifies laterally from a seed area of the film. The semiconductor devices can be included as pixel controllers and drivers in liquid-crystal display devices, and in image sensors, static random-access memories (SRAM), silicon-on-insulator (SOI) devices, and three-dimensional integrated circuit devices.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav	TM	Turkmenistan
BF	Burkina Faso	GR	Greece		Republic of Macedonia	TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's	NZ	New Zealand		
CM	Cameroon		Republic of Korea	PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

Crystallization Processing of Semiconductor Film Regions on a Substrate, and Devices Made Therewith

Technical Field

The invention relates to semiconductor materials processing for semiconductor integrated devices.

Background of the Invention

Semiconductor devices can be made in a layer or film of silicon on a quartz or glass substrate, for example. This technology is in use in the manufacture of image sensors and active-matrix liquid-crystal display (AMLCD) devices. In the latter, in a regular array of thin-film transistors (TFT) on an appropriate transparent substrate, each transistor serves as a pixel controller. In commercially available AMLCD devices, the thin-film transistors are formed in hydrogenated amorphous silicon films (a-Si:H TFTs).

In the interest of enhanced switching characteristics of TFTs, polycrystalline silicon has been used instead of amorphous silicon. A polycrystalline structure can be obtained by excimer-laser crystallization (ELC) of a deposited amorphous or microcrystalline silicon film, for example.

However, with randomly crystallized poly-silicon, the results remain unsatisfactory. For small-grained poly-silicon, device performance is hampered by the large number of high-angle grain boundaries, e.g., in the active-channel region of a TFT. Large-grained poly-silicon is superior in this respect, but significant grain-structure irregularities in one TFT as compared with another then result in non-uniformity of device characteristics in a TFT array.

Summary of the Invention

For improved device characteristics and device uniformity, a lateral solidification technique is applied to a semiconductor film on a substrate. The technique, which may be termed artificially controlled super-lateral growth (ACSLG), involves irradiating a portion of the film with a suitable radiation pulse, e.g. a laser beam pulse, locally to melt the film completely through its entire thickness. When the molten semiconductor material solidifies, a crystalline structure grows from a preselected portion of the film which did not undergo complete melting.

In a preferred first embodiment of the technique, an irradiated structure includes a substrate-supported first semiconductor film, a heat-resistant film on the first semiconductor film, and a second semiconductor film on the heat-resistant film. In this embodiment, both front and back sides of the structure are irradiated with a pulse.

In a preferred second embodiment, lateral solidification is from a first region via a constricted second region to a third region which is intended as a device region. One-sided irradiation is used in this embodiment, in combination with area heating through the substrate.

In a preferred third embodiment, a beam is pulsed repeatedly in forming an extended single-crystal region as a result of laterally stepping a radiation pattern for repeated melting and solidification.

Advantageously, the technique can be used in the manufacture of high-speed liquid crystal display devices, wherein pixel controllers or/and driver circuitry are made in single-crystal or regular/quasi-regular polycrystalline films. Other applications

include image sensors, static random-access memories (SRAM), silicon-on-insulator (SOI) devices, and three-dimensional integrated circuit devices.

Brief Description of the Drawings

Fig. 1 is a schematic representation of a projection irradiation system as can be used for the first embodiment of the technique.

Fig. 2 is a schematic, greatly enlarged side view of a sample structure for the first embodiment.

Figs. 3A and 3B are schematic, greatly enlarged top views of TFT device microstructures which can be made in semiconductor material of the first embodiment.

Fig. 4 is a schematic representation of an irradiation system as can be used for the second embodiment of the technique.

Fig. 5 is a schematic, greatly enlarged side view of a sample structure for the second embodiment.

Figs. 6A-6D are schematic top views of the sample structure of Fig. 5 at sequential stages of processing.

Fig. 7 ia a schematic representation of an irradiation system as can be used for the third embodiment.

Fig. 8 is a schematic, greatly enlarged side view of a sample structure for the third embodiment.

Figs. 9A-9F are schematic top views of a sample structure with side view as in Fig. 8 at sequential stages in a first version of a first variant of processing.

Figs. 10A-10F are schematic top views of a sample structure with side view as in Fig. 8 at sequential stages in a second version of the first variant of processing.

Figs. 11A-11C are schematic top views of a sample structure at sequential stages of a second variant of processing.

Fig. 12 is a schematic top view of a liquid-crystal display device in which TFTs are included.

Detailed Description of Preferred Embodiments

Described in the following are specific, experimentally realized examples, as well as certain variations thereof. Explicitly or implicitly, some variations are common to more than one of the embodiments, and further variations, within the scope of the claims, will be apparent to those skilled in the art. Included, e.g., is the use of semiconductor materials other than silicon, such as germanium, silicon-germanium, gallium arsenide or indium phosphide, for example. Included also is the use of a substrate of any suitable material, e.g., silicon, quartz, glass or plastic, subject to considerations of stability, inertness and heat resistance under processing conditions. And included is the use of a radiation beam other than a laser beam, e.g., an electron or ion beam.

First Embodiment

The projection irradiation system of Fig. 1 includes an excimer laser 11, mirrors 12, a beam splitter 13, a variable-focus field lens 14, a patterned projection mask 15, a two-element imaging lens 16, a sample stage 17, a variable attenuator 18 and a focusing lens 19. With this system, simultaneous radiation pulses can be applied to the front and back sides of a sample 10 on the stage 17.

For the first embodiment of the technique, a "dual-layer" (DL) sample structure was prepared as shown

in Fig. 2, including a transparent substrate 20, a first amorphous silicon film 21, an SiO_2 film 22, and a second amorphous silicon film 23. Film thicknesses were 100 nanometers for the amorphous silicon films and 500 nanometers for the SiO_2 film. Alternative heat-resistant materials such as, e.g., silicon nitride or a high-temperature glass may be used for the film 22.

With pattern projection onto the second or top silicon film 23 and broad-beam irradiation of the first or bottom silicon film 21, the first silicon film 21 can be regarded as a sacrificial layer which is included favorably to affect the thermal environment for maximized lateral crystal growth in the top silicon film 23. The roles of these films is reversed if, alternatively, the pattern is projected through the substrate onto the first film. In the pattern-irradiated film, large, laterally solidified grains will be formed, making the processed film well-suited for TFTs, for example.

Structures in accordance with Fig. 2 were prepared by sequential low-pressure chemical vapor deposition (LPCVD) of a-Si, SiO_2, and again a-Si on a quartz substrate. Other suitable deposition methods, for producing amorphous or microcrystalline deposits, include plasma-enhanced chemical vapor deposition (PECVD), evaporation or sputtering, for example.

Samples were placed onto the stage 17 of the projection irradiation system of Fig. 1. The mask 15 had a pattern of simple stripes 50 micrometers wide, with various separation distances from 10 to 100 micrometers.

The mask pattern was projected onto the samples with different reduction factors in the range from 3 to 6. The back-side energy density was controlled by the variable attenuator 18. Samples were irradiated at room temperature with a 30-nanosecond XeCl excimer laser pulse

having a wavelength of 308 nanometers, quartz being transparent at this wavelength. Such a laser is commercially available under the designation LambdaPhysik Compex 301. For a glass substrate, a longer wavelength would have been required, e.g., 348 nanometers.

Irradiation was with fixed front-side energy density and with various back-side energy densities. Estimated front-side energy density was approximately 1.0 J/cm^2 at the sample plane. The back-side energy densities were in the range from 170 to 680 mJ/cm^2.

For examination subsequent to irradiation, the films were thoroughly defect-etched using Secco etchant and examined using scanning electron microscopy (SEM). The largest, most uniform grains were obtained at a back-side energy density of 510 mJ/cm^2. These grains grew laterally from the two sides of stripe regions, forming two rows of grains with a well-defined grain boundary at the center line of the stripe.

Even if the resulting individual crystals may not be large enough to accommodate the entire active-channel region of a TFT, they form a regular or quasi-regular polycrystalline structure which can serve as active-channel region of a TFT, e.g., as illustrated in Fig. 3A or Fig. 3B. Shown are a source electrode 31, a drain electrode 32, a gate electrode 33 and an active-channel region 34. In Fig. 3A, the active-channel region includes both rows of grains produced as described above. With grains sufficiently large as in Fig. 3B, the active-channel region can be formed by a single row of grains.

In processing according to the first embodiment, the role of the sacrificial bottom film 21 may be understood as being that of a heat susceptor which stores energy when heated by the beam, the greatest benefit being obtained when this film melts. The stored

heat is released during solidification. This decreases the degree to which the top film 23 loses heat by conduction. Accordingly, for maximum benefit, care is called for in proper dimensioning of the irradiated structure. If the SiO_2 film 22 is too thin, the thermal evolution of the silicon films 21 and 23 will tend to track together, without significant benefit from the inclusion of the film 21. On the other hand, if the film 22 is too thick with respect to the thermal diffusion length of the physical process, the film 21 will have insufficient influence on the transformation in the top film 23. As to the bottom film 21, its thickness should be chosen for this film to have sufficient thermal mass. But the thicker the film 21, the more energy will be required for its melting.

As alternatives to projection of a pattern onto the silicon layer 23, a desired pattern may be defined there by a proximity mask, a contact mask, or a deposited mask layer which is patterned photo-lithographically, for example.

In one variant of masking, a mask layer may serve to reduce heating in the area beneath the mask, e.g., by absorbing or reflecting incident radiation. Alternatively, with a suitable mask material of suitable thickness, a complementary, anti-reflection effect can be realized to couple additional energy into the semiconductor film beneath the mask material. For example, an SiO_2 film can be used to this effect on a silicon film. This variant is advantageous further in that the mask layer can serve as a restraint on the molten semiconductor material, thus preventing the molten semiconductor layer from agglomerating or deforming under surface tension.

Second Embodiment

The irradiation system of Fig. 4 includes an excimer laser 41, a prism deflector 42, a focusing lens 43, a vacuum chamber 44 and a hot stage 45 on which a sample 40 is disposed.

For the second embodiment of the technique and using the irradiation system of Fig. 4, the sample structure of Fig. 5 includes a substrate 50, a thermal oxide film 51, a first patterned amorphous silicon film 52, an SiO_2 film 53, a second patterned silicon film 54, and a further deposited SiO_2 film 55. Typical thicknesses are 100 nanometers for the thermal oxide film 51, 100 nanometers for the a-Si film 52, 210 nanometers for the SiO_2 film 53, 120 nanometers for the a-Si film 54, and 170 nanometers for the SiO_2 film 55.

Such a sample structure was prepared by depositing the amorphous silicon film 52 by low-pressure chemical vapor deposition (LPCVD) onto the thermal oxide film 51 on a silicon wafer 50. The silicon film 52 was coated with a photoresist which was then exposed in a stepper and developed, and the silicon film 52 was reactively ion-etched in SF_6/O_2 plasma for patterning. The resulting pattern of a "first-level island" of the silicon film 52 is shown in Fig. 6A as viewed from the top. The pattern consists of three parts: a square "main-island" region 523 which is intended for eventual device use, a rectangular "tail" region 521, and a narrow "bottleneck" region 522 connecting the tail region 521 with the main-island region 523. Dimensions were chosen as follows: 20 by 10 micrometers for the tail region 521, 5 by 3 micrometers for the bottleneck region 522, and different dimensions in the range from 10 by 10 to 50 by 50 micrometers for the main-island region 521.

The first-level islands were encapsulated with the SiO_2 film 53 by plasma-enhanced chemical-vapor deposition (PECVD), and amorphous silicon was deposited on top. Photolithographic processing was used again, for patterning the amorphous silicon film as a "second-level island" 54 dimensioned 5 by 5 micrometers. The second-level island 54 is positioned directly above the tail region 521 to serve as a beam blocker during irradiation. Last, the entire structure was encapsulated with PECVD SiO_2.

For processing, a sample was placed on a resistively heated graphite hot stage inside a vacuum chamber at a pressure of 10^{-5} torr. Vacuum-processing can be dispensed with if a suitable alternative heater is available. Heating was to a substrate temperature of 1000 to 1200 °C, which required a ramp-up time interval of about three minutes. Before irradiation, the sample was held at the final substrate temperature for approximately two minutes. The sample temperature was monitored occasionally by a directly attached thermocouple and continuously by a digital infrared thermometer. The sample was irradiated with a single excimer-laser pulse at energy densities that were sufficiently high to completely melt all of the first-level island except for the beam-blocked area within the tail region.

For analysis of the microstructure, the irradiated samples were Secco-etched. For samples irradiated at a substrate temperature of 1150 °C, optical Nomarski micrographs of the Secco-etched samples showed complete conversion of islands 20 by 20, 40 by 40 and 50 by 50 micrometers into single-crystal islands (SCI). Defect patterns in the etched samples suggest that the main-island zones contain low-angle sub-boundaries

similar to those observed in zone melting recrystallization (ZMR), as well as planar defects which have been identified in SLG studies. At a lower substrate temperature, such as at 1100 °C, only the smaller, 20-by-20 micrometer islands were converted into single-crystal islands free of high-angle grain boundaries. And at still-lower substrate temperatures of 1050 °C and 1000 °C, high-angle grain boundaries appeared even in the 20 by 20 micrometer islands.

The solidification sequence in this second embodiment may be understood with reference to Figs. 6B-6D as follows: Upon irradiation, the second-level square 54 blocks most of the beam energy incident on the area, which prevents complete melting in the beam-blocked area of the tail region 521. The rest of the exposed first level regions melts completely as illustrated by Fig. 6B. As the film is conductively cooled through the substrate, the liquid-solid interface at the beam-blocked region undercools, and silicon grains 61 start to grow radially outward from the beam-blocked region. Within the tail region 521 , many of the grains 61 are quickly occluded, and only one or a few favorably located grains grow toward the bottleneck 522. The bottleneck 522 is configured such that just one of these grains expands through the bottleneck 522 into the main-island region 523. If the substrate temperature is high enough and the main island 523 is small enough to prevent nucleation in the super-cooled liquid, lateral growth of the one grain that grew through the bottleneck 522 converts the entire main island 523 into a single-crystal region.

Thus, successful conversion of the main-island region 523 into single-crystal form requires a suitable combination of substrate temperature and island size.

The molten silicon must be sustained at a temperature which is sufficiently high for the characteristic time of nucleation for a specific volume to be much longer than the characteristic time required for the complete conversion by lateral solidification. Since the characteristic conversion time depends mainly on the distance to be converted, i.e., the lateral dimension of the main island, the island size must be related to the substrate temperature such that the characteristic conversion time is commensurate with the average lateral growth distance that can be achieved before any nucleation is triggered within the liquid. As compared with zone-melting recrystallization, the present technique allows the recrystallization of very thin films, e.g., having a thickness of 100 nanometers or less.

Instead of by beam blocking, a seed region can be defined by complementary masking with an anti-reflection film, as described above for the first embodiment. Alternatively further, a seed region can be defined by projection.

Third Embodiment

The projection irradiation system of Fig. 7 includes an excimer laser 71, mirrors 72, a variable-focus field lens 74, a patterned mask 75, a two-element imaging lens 76, a sample stage 77, and a variable attenuator 78. A sample 70 is disposed on the sample stage 77. This system can be used to produce a shaped beam for stepped growth of a single-crystal silicon region in a sequential lateral solidification (SLS) process. Alternatively, a proximity mask or even a contact mask may be used for beam shaping.

The sample structure of Fig. 8 has a substrate 80, a thermal oxide film 81, and an amorphous silicon film 82.

In the following, the third embodiment of the technique is described with reference to Figs. 9A-9F and 10A-10F showing two versions of a first variant, and Figs. 11A-11B showing a second variant.

Starting with the amorphous silicon film 82, which in this exemplary embodiment is patterned as a rectangle (Fig. 9A), a region 91, bounded by two broken lines, of the silicon film 82 is irradiated with a pulse, to completely melt the silicon in that region (Fig. 9B), and then resolidify the molten silicon (Fig. 9C) in the region 91. Here, the region 91 is in the shape of a stripe, and irradiation of the region 91 may be by masked projection or by use of a proximity mask. Upon resolidification of the molten silicon in the region 91, two rows of grains grow explosively from the broken line boundaries of the region 91 towards the center of the region 91. Growth of the two rows of grains is over the characteristic lateral growth to a final distance 92. In any remainder of region 91, a fine grained polycrystalline region 93 is formed. Preferably, the width of the stripe is chosen such that, upon resolidification, the two rows of grains approach each other without converging. Greater width, which is not precluded, does not contribute to the efficacy of processing. Lesser width tends to be undesirable since the subsequent step may have to be reduced in length, and the semiconductor surface may become irregular where grains growing from opposite directions come together during the solidification process. An oxide cap may be formed over the silicon film to retard agglomeration and constrain the surface of the silicon film to be smooth.

A next region to be irradiated is defined by shifting (stepping) the sample with respect to the masked projection or proximity mask in the direction of crystal growth. The shifted (stepped) region 94 is bounded by two broken lines in Fig. 9D. The distance of the shift is such that the next region to be irradiated 92 overlaps the previously irradiated region 91 so as to completely melt one row of crystals while partially melting the other row of crystals, as shown in Fig. 9E. Upon resolidification, the partially melted row of crystals will become longer, as shown in Fig. 9F. In this fashion, by repeatedly shifting the irradiated portion, single crystalline grains of any desired length may be grown.

If the pattern of the irradiated region is not a simple stripe, but is in the shape of a chevron 101, as defined by the broken lines in Fig. 10A, the same sequence of shifting the irradiated region shown in Figs. 10B-10F will result in the enlargement of one grain growing from the apex of the trailing edge of the shifting (stepping) chevron pattern. In this manner, a single-crystal region can be grown with increasing width and length.

A large area single-crystal region can also be grown by applying sequentially shifted (stepped) irradiation regions to a patterned amorphous silicon film, such as that illustrated in Fig. 11A, having a tail region 111, a narrow bottleneck region 112 and a main island region 113. The cross-section of regions 111, 112 and 113 in Figs. 11A-11C is similar to that shown in Fig. 5, except that the radiation blocking amorphous silicon region 54 and the second silicon dioxide layer 55 are absent. The region of irradiation defined by masked projection or a proximity mask is illustrated by the

regions bounded by broken lines in Figs. 11A-11C, which also show the sequential lateral shifting (stepping) of the irradiated region to obtain the growth of a single grain from the tail region 111 through the bottleneck region 112 to produce a single crystal island region 113.

Sequential lateral melting and resolidification in the examples of Figs. 9A-9F, 10A-10F and 11A-11C were carried out on amorphous silicon films which had been deposited by chemical vapor deposition (CVD) on a silicon dioxide coated quartz substrate, with film thicknesses from 100 to 240 nanometers. The production of single-crystal stripes was confirmed in optical and scanning electron microscopic examination of defect-etched samples.

Optionally, the substrate may be heated, e.g., to reduce the beam energy required for melting or to lengthen the lateral growth distance per step. Such benefits may be realized also by two-sided irradiation of a sample on a stage as shown in Fig. 1.

Further Processing and Applications

With a semiconductor film processed by the present technique, integrated semiconductor devices can be manufactured by well-established further techniques such as pattern definition, etching, dopant implantation, deposition of insulating layers, contact formation, and interconnection with patterned metal layers, for example. In preferred thin-film semiconductor transistors, at least the active-channel region has a single-crystal, regular or at least quasi-regular microstructure, e.g., as illustrated by Figs. 3A and 3B.

Of particular interest is the inclusion of such TFTs in liquid-crystal display devices as schematically shown in Fig. 12. Such a device includes a substrate 120

of which at least a display window portion 121 is transparent. The display window portion 121 includes a regular array of pixels 122, each including a TFT pixel controller. Each pixel controller can be individually addressed by drivers 123. Preferably, pixel controllers or/and driver circuitry are implemented in semiconductor material processed in accordance with the technique of the present invention.

Other applications include image sensors, static random-access memories (SRAM), silicon-on-insulator (SOI) devices, and three-dimensional integrated circuit devices.

Claims

1. A method for making a polycrystalline region as a laterally extending portion of a supported film of semiconductor material, comprising:

simultaneously irradiating, with pulsed radiation which induces heat in the semiconductor material, front and back sides of a structure comprising a radiation-permeable substrate in back, a first semiconductor film on the substrate, a heat-resistant film on the first semiconductor film, and a second semiconductor film on the heat-resistant film, so as to melt all semiconductor material in a laterally extending region of the one of the semiconductor films which includes the portion,

so that, after the simultaneous irradiation, a polycrystalline microstructure is formed in the region by lateral solidification from a boundary of the region.

2. The method of claim 1, wherein the region is delimited by parallel edges.

3. The method of claim 2, wherein the parallel edges are spaced apart by a distance for which simultaneous lateral solidification from the edges results in complete crystallization of the region.

4. The method of claim 1, wherein the semiconductor material comprises silicon.

5. The method of claim 1, wherein the heat-resistant layer consists essentially of SiO_2.

6. The method of claim 1, wherein the substrate is a glass substrate.

7. The method of claim 1, wherein the substrate is a quartz substrate.

8. The method of claim 1, wherein the laterally extending portion is in the first semiconductor film.

9. The method of claim 1, wherein the laterally extending portion is in the second semiconductor film.

10. The method of claim 1, wherein the region has a shape defined by a mask pattern.

11. The method of claim 10, wherein the mask pattern is projected.

12. The method of claim 10, wherein the mask pattern is defined by a proximity mask.

13. The method of claim 10, wherein the mask pattern is defined by a contact mask.

14. The method of claim 1, wherein the radiation comprises laser radiation.

15. The method of claim 1, wherein the laterally extending region is encapsulated.

16. On a supporting substrate, a semiconductor film processed by the method of claim 1.

17. On a supporting substrate, a plurality of semiconductor devices in a semiconductor film processed by the method of claim 1.

18. On a supporting substrate, an integrated circuit comprising a plurality of thin-film transistors in which at least the active-channel region is processed by the method of claim 1.

19. A liquid-crystal display device comprising a plurality of pixel-controller thin-film transistors in which at least the active-channel region is processed by the method of claim 1.

20. A liquid-crystal display device comprising a pixel-driver integrated circuit which comprises a plurality of thin-film transistors in which at least the active-channel region is processed by the method of claim 1.

21. A method for making a laterally extending crystalline region in a film of semiconductor material on a substrate, comprising:

irradiating, with pulsed radiation which induces heat in the semiconductor material, a portion of the semiconductor film so as to entirely melt the semiconductor material in the portion, and

permitting the molten semiconductor material in the portion to solidify; wherein:

the portion is configured so as to include a first sub-portion, a second sub-portion which is contiguous to the first sub-portion, and a third sub-portion which is contiguous to the second sub-portion,

the first sub-portion being configured for nucleation of semiconductor crystals at its boundary,

the second sub-portion being configured such that just one of the nucleated crystals grows from the first sub-portion through the second sub-portion into the third sub-portion, and

the third sub-portion being configured such that the one crystal occupies the third sub-portion in its entirety.

22. The method of claim 21, wherein the first sub-portion is configured with an island portion for nucleation of semiconductor crystals.

23. The method of claim 21, wherein the configuration of the second sub-portion precludes a straight-line path between the first sub-portion and the third sub-portion.

24. The method of claim 21, wherein the semiconductor material comprises silicon.

25. The method of claim 21, wherein the substrate is heated.

26. The method of claim 21, wherein the substrate is a glass substrate.

27. The method of claim 21, wherein the substrate is a quartz substrate.

28. The method of claim 21, wherein the pulsed radiation is applied to front and back of the semiconductor film.

29. The method of claim 21, wherein the semiconductor film has a thickness not exceeding 100 nanometers.

30. The method of claim 22, wherein the island portion has a shape defined by a mask pattern.

31. The method of claim 30, wherein the mask pattern is projected.

32. The method of claim 30, wherein the mask pattern is defined by a proximity mask.

33. The method of claim 30, wherein the mask pattern is defined by a contact mask.

34. The method of claim 21, wherein the radiation comprises laser radiation.

35. The method of claim 21, wherein the portion is encapsulated.

36. On a supporting substrate, a semiconductor film processed by the method of claim 21.

37. On a supporting substrate, a plurality of semiconductor devices in a semiconductor film processed by the method of claim 21.

38. On a supporting substrate, an integrated circuit comprising a plurality of thin-film transistors in which at least the active-channel region is processed by the method of claim 21.

39. A liquid-crystal display device comprising a plurality of pixel-controller thin-film transistors in which at least the active-channel region is processed by the method of claim 21.

40. A liquid-crystal display device comprising a pixel-driver integrated circuit which comprises a plurality of thin-film transistors in which at least the active-channel region is processed by the method of claim 21.

41. A method for making a laterally extending crystalline region in a film of semiconductor material on a substrate, comprising:

(a) irradiating, with pulsed radiation which induces heat in the semiconductor material, a first portion of the film so as to melt the semiconductor material in the first portion throughout its thickness;

(b) permitting the semiconductor in the first portion to solidify, thereby forming at least one semiconductor crystal at a boundary of the first portion, the first portion then being a previous portion for further processing;

(c) irradiating a further portion of the semiconductor which is stepped from the previous portion in a stepping direction and which overlaps the at least one semiconductor crystal in part;

(d) permitting the molten semiconductor material in the further portion to solidify, thereby enlarging the semiconductor crystal by growth in the stepping direction;

(e) repeating steps (c) and (d) in combination, with the further portion of each step

becoming the previous portion for the next step, until a desired crystalline region is formed.

42. The method of claim 41, wherein the irradiated portions are stripes.

43. The method of claim 42, wherein the stripes have a width between edges such that simultaneous lateral solidification from the edges does not result in complete crystallization of the stripes.

44. The method of claim 41, wherein the semiconductor material comprises silicon.

45. The method of claim 41, wherein the irradiated portions are chevrons.

46. The method of claim 41, wherein the substrate is a glass substrate.

47. The method of claim 41, wherein the substrate is a quartz substrate.

48. The method of claim 41, wherein the laterally extending crystalline region is defined by patterning the film of semiconductor material.

49. The method of claim 48, wherein the pattern of the film comprises a tail portion, a bottleneck portion which is contiguous to the tail portion, and a main-island portion which is contiguous to the bottleneck portion.

50. The method of claim 41, wherein the irradiated portions are defined by a mask pattern.

51. The method of claim 50, wherein the mask pattern is projected.

52. The method of claim 50, wherein the mask pattern is defined by a proximity mask.

53. The method of claim 50, wherein the mask pattern is defined by a contact mask.

54. The method of claim 41, wherein the radiation comprises laser radiation.

55. The method of claim 41, wherein the laterally extending region is encapsulated.

56. On a supporting substrate, a semiconductor film processed by the method of claim 41.

57. On a supporting substrate, a plurality of semiconductor devices in a semiconductor film processed by the method of claim 41.

58. On a supporting substrate, an integrated circuit comprising a plurality of thin-film transistors in which at least the active-channel region is processed by the method of claim 41.

59. A liquid-crystal display device comprising a plurality of pixel-controller thin-film transistors in which at least the active-channel region is processed by the method of claim 41.

60. A liquid-crystal display device comprising a pixel-driver integrated circuit which comprises a plurality of thin-film transistors in which at least the active-channel region is processed by the method of claim 41.

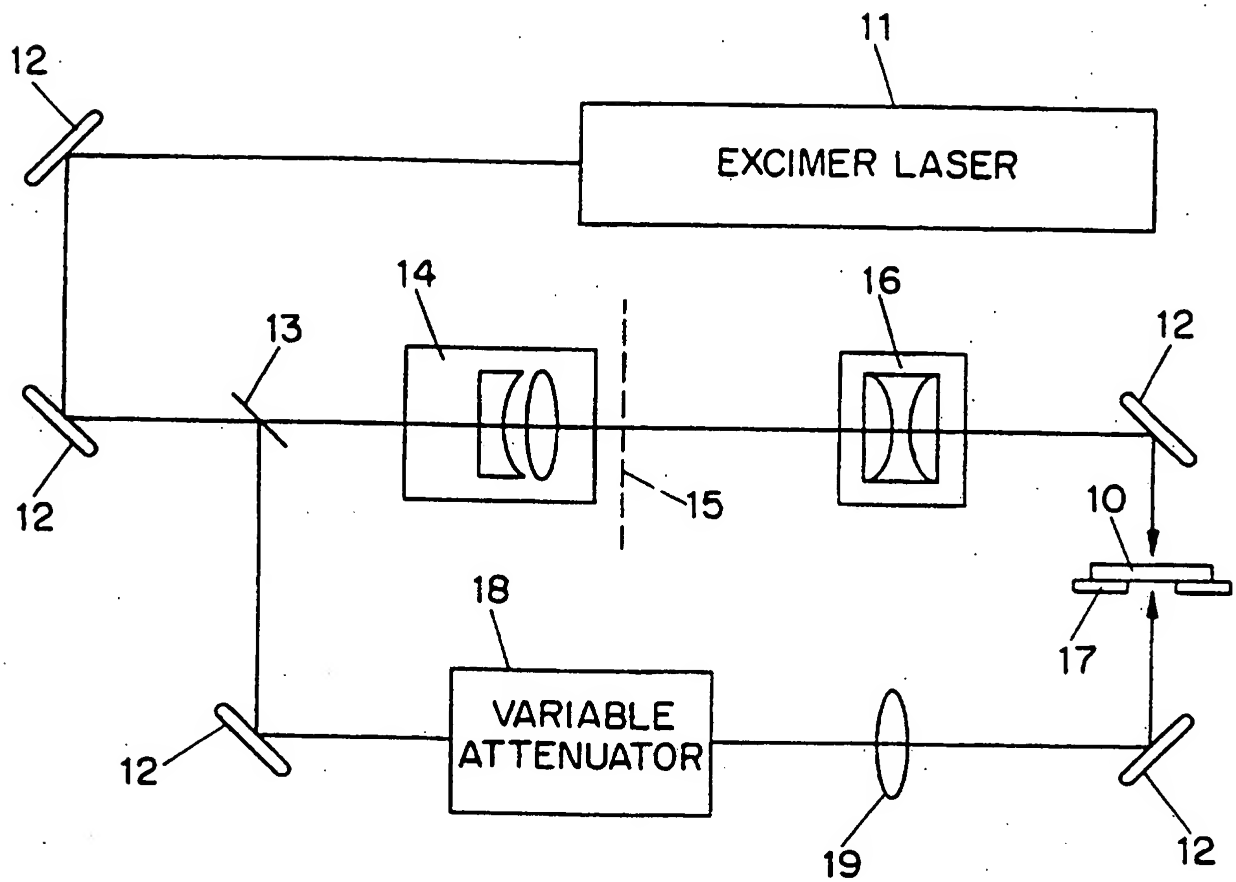

11
EXCIMER LASER
12
12
13
14
16
12
15
10
18
17
VARIABLE ATTENUATOR
12
19
12

FIG. 1

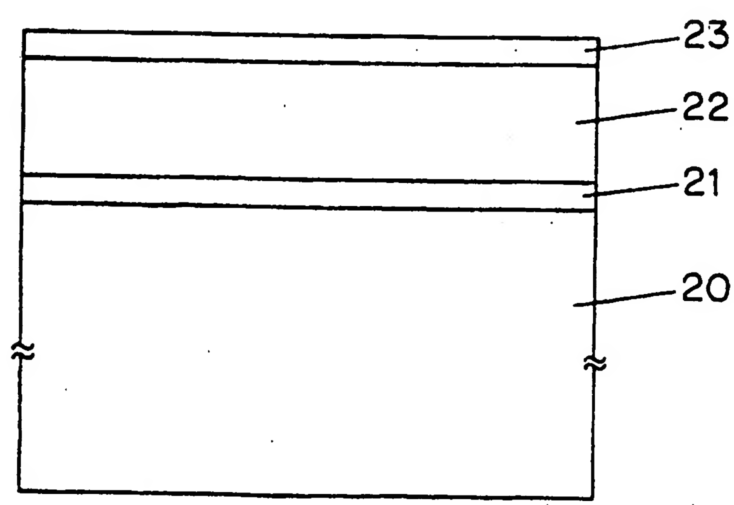

23
22
21
20

FIG. 2

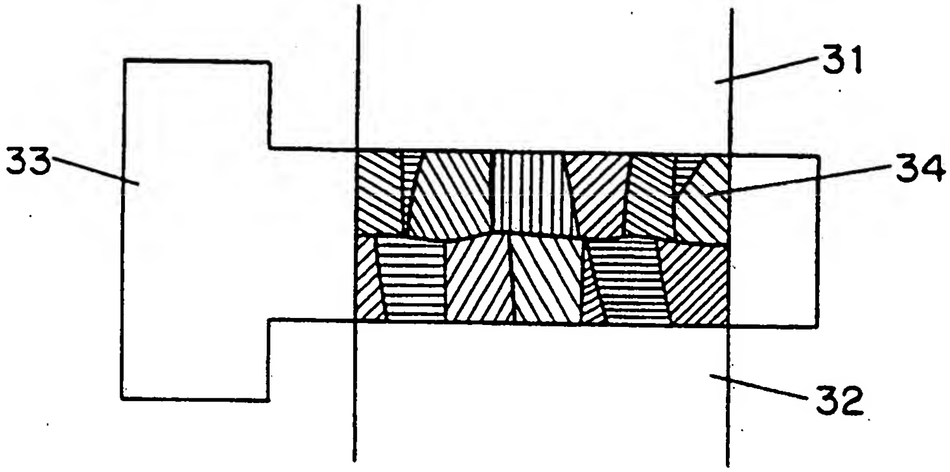


FIG. 3A

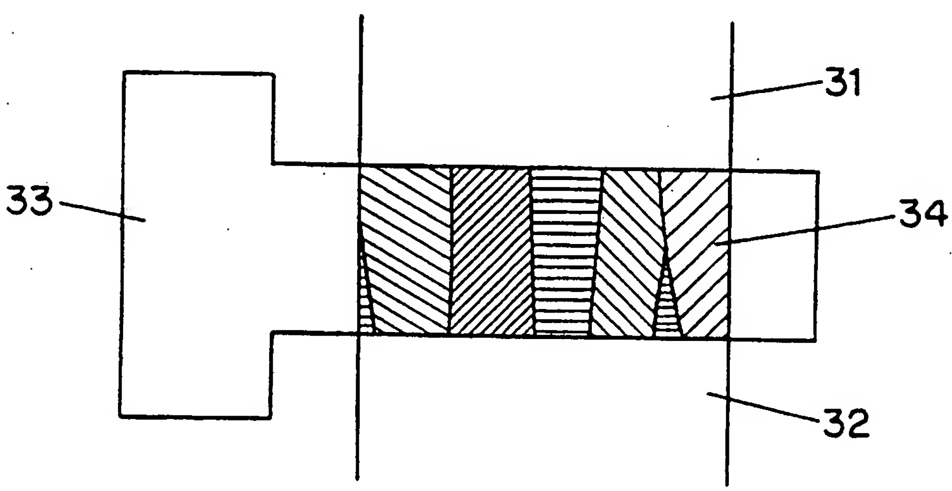


FIG. 3B

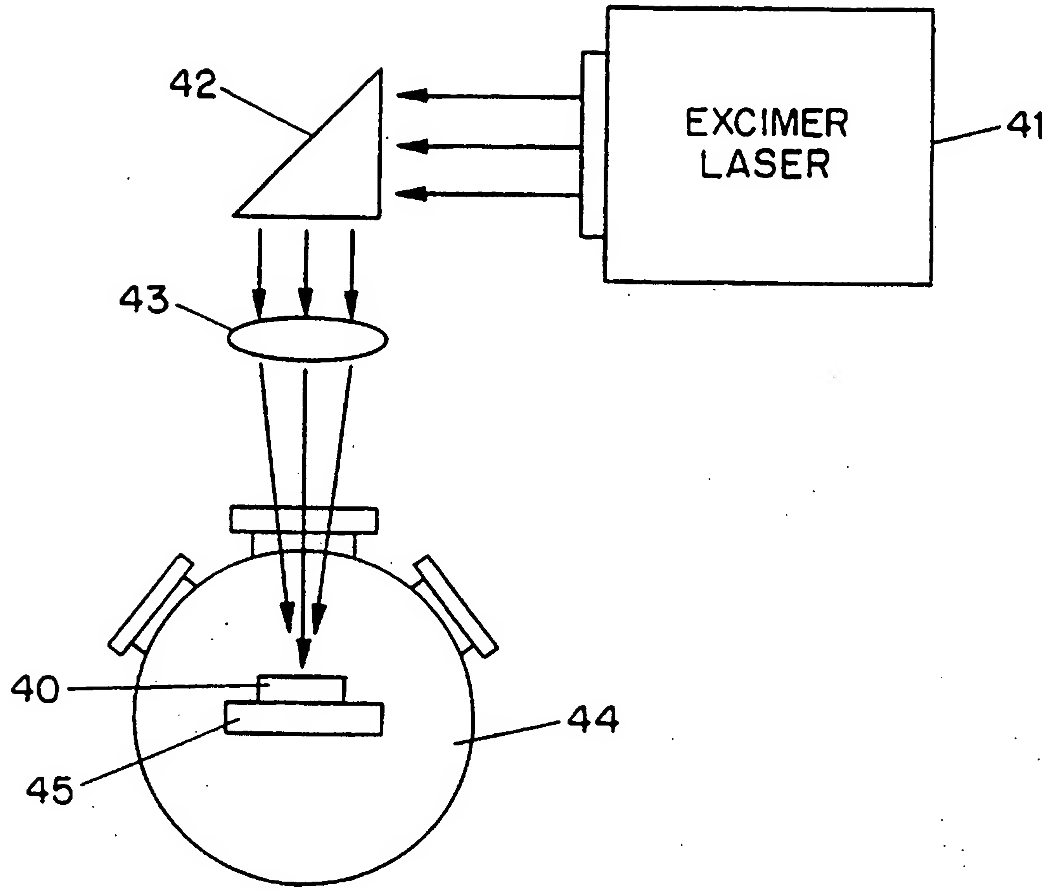


FIG. 4

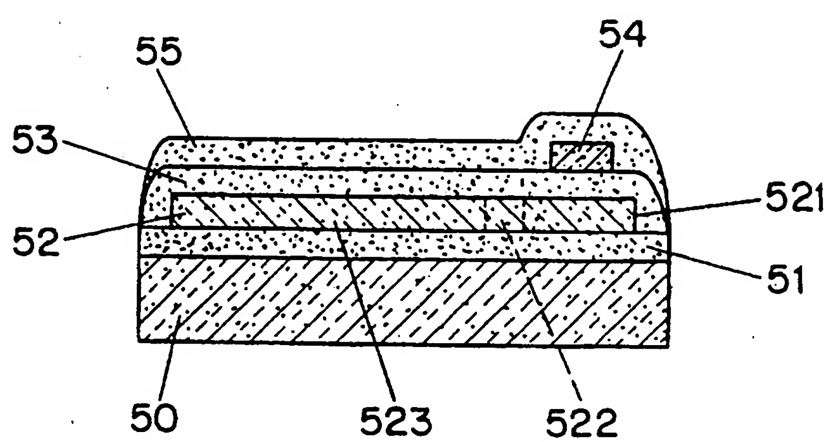


FIG. 5

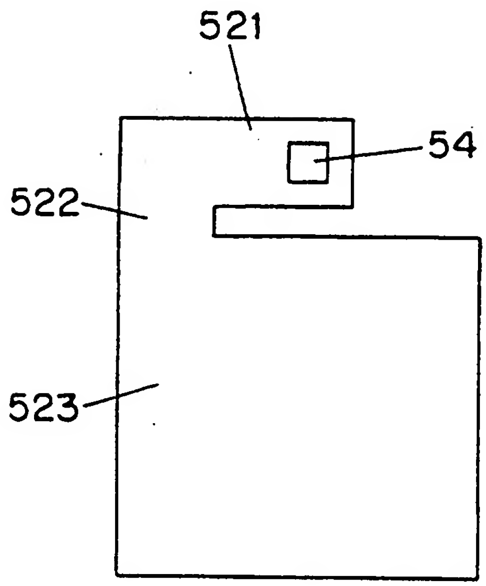


FIG. 6A

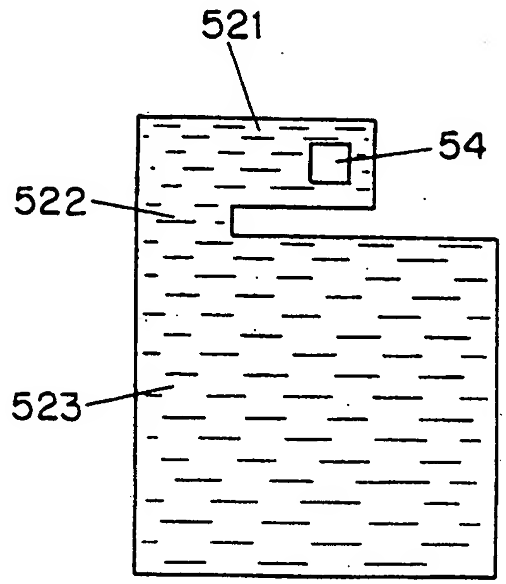


FIG. 6B

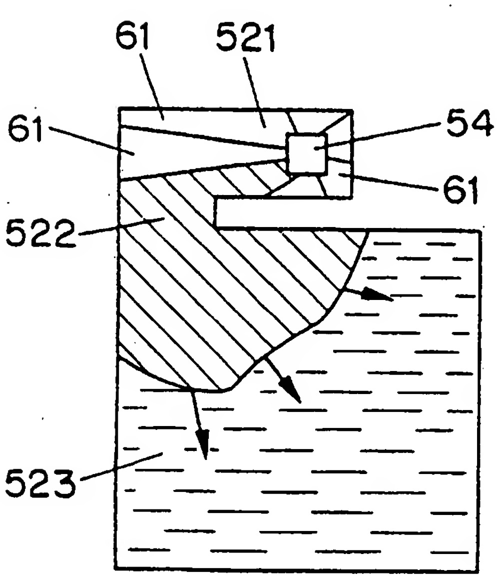


FIG. 6C

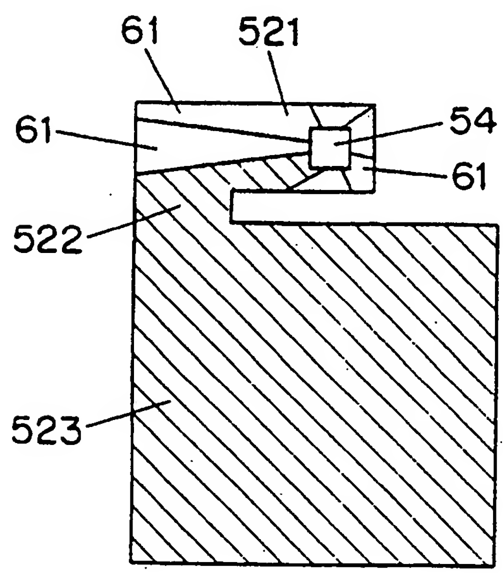


FIG. 6D

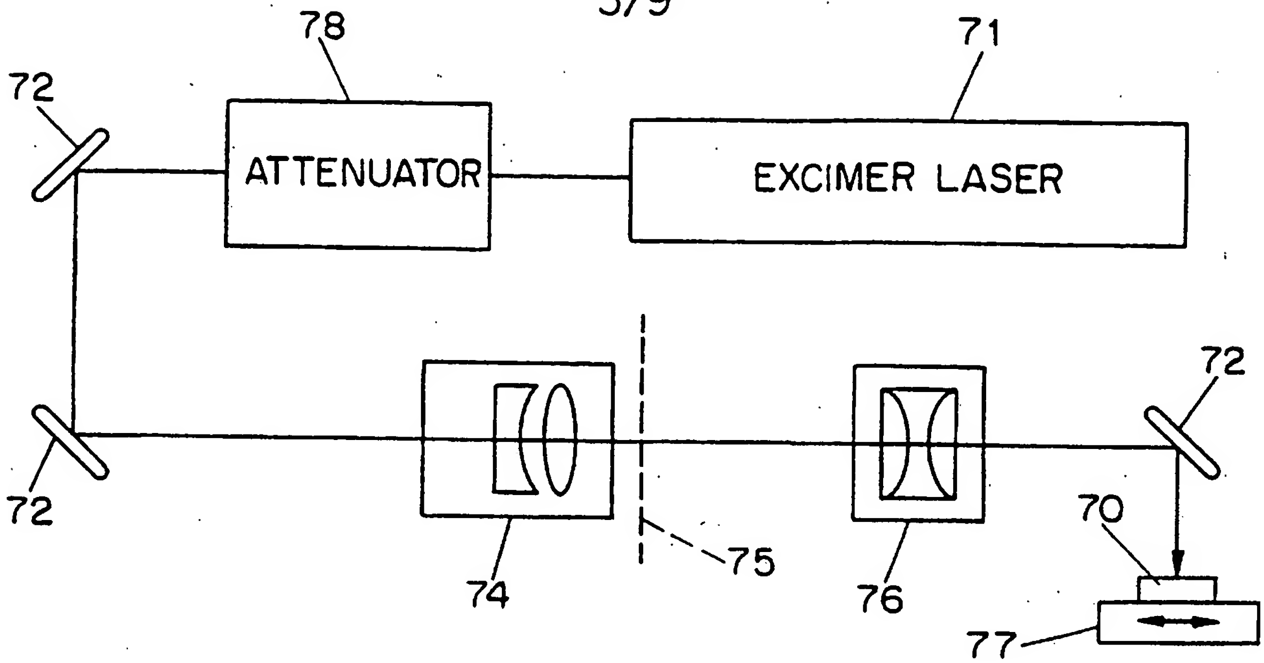


FIG. 7

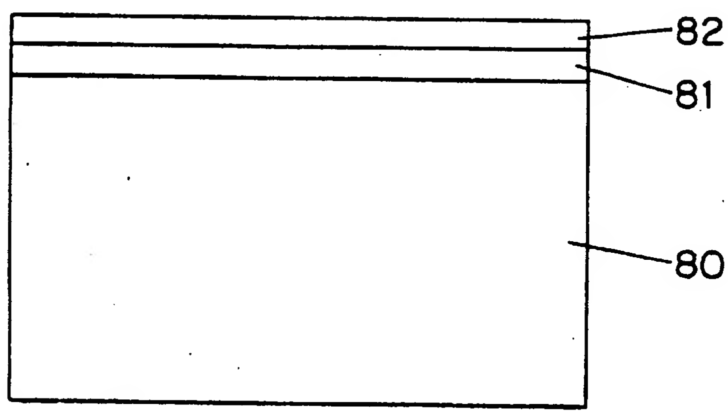


FIG. 8

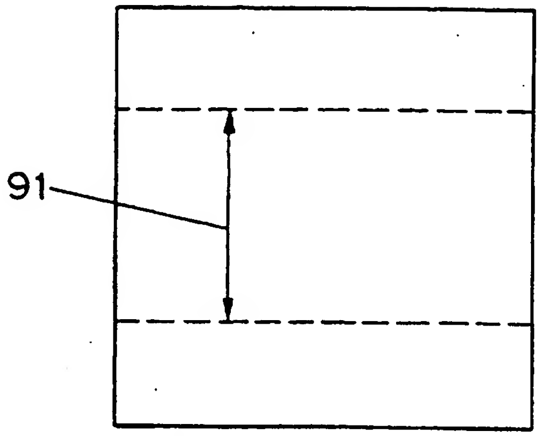


FIG. 9A

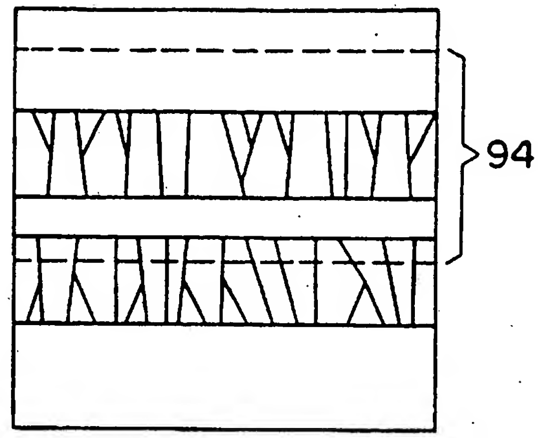


FIG. 9D

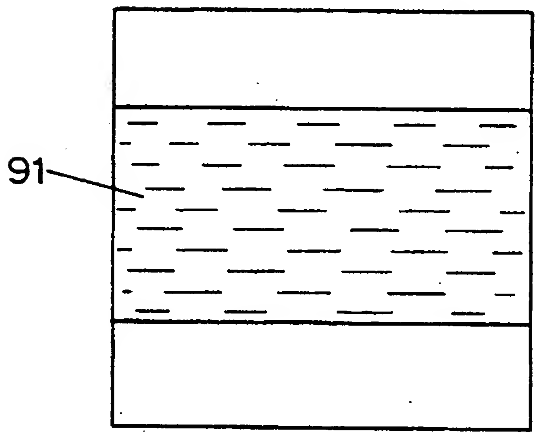


FIG. 9B

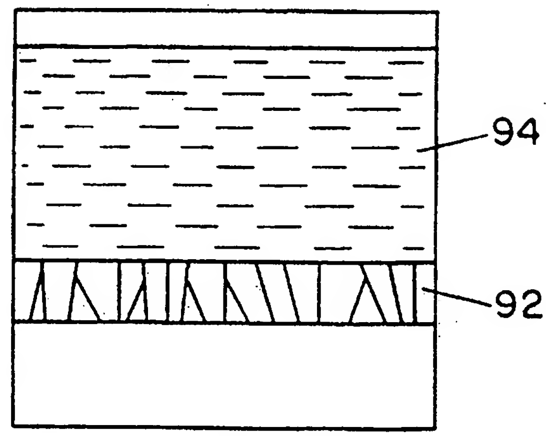


FIG. 9E

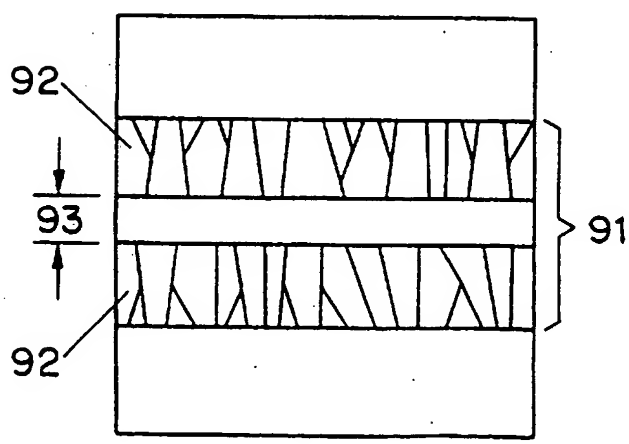


FIG. 9C

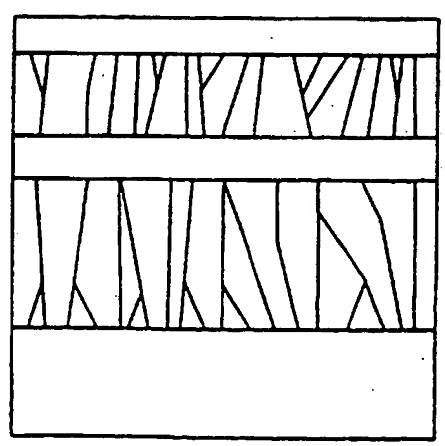


FIG. 9F

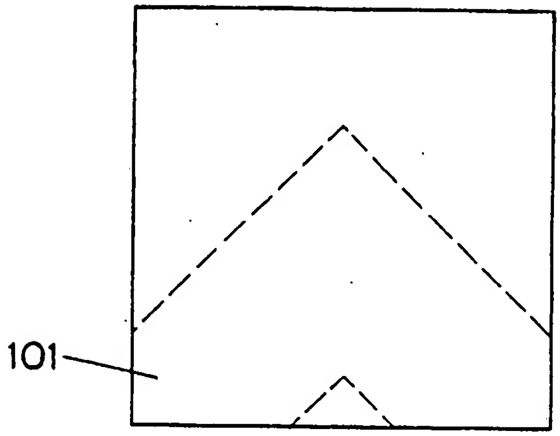


FIG. 10A

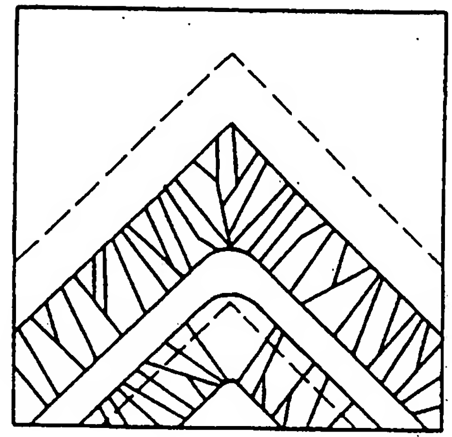


FIG. 10D

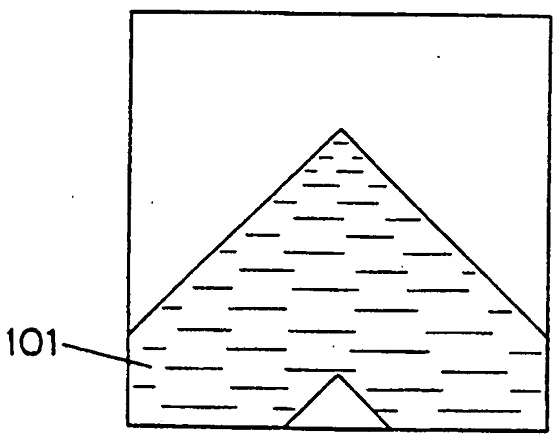


FIG. 10B

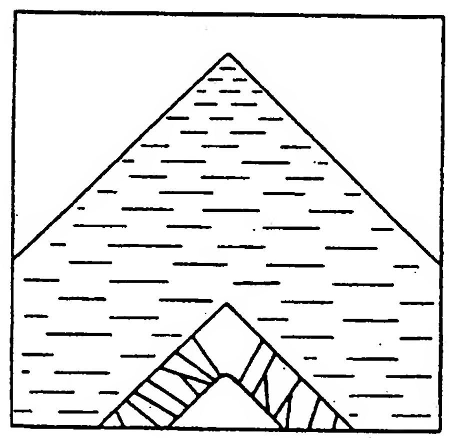


FIG. 10E

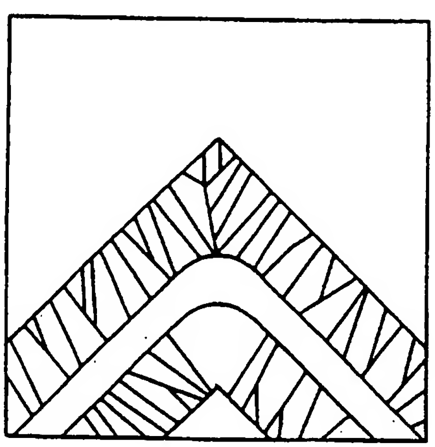


FIG. 10C

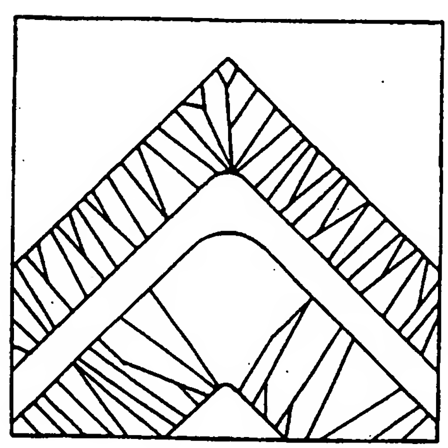


FIG. 10F

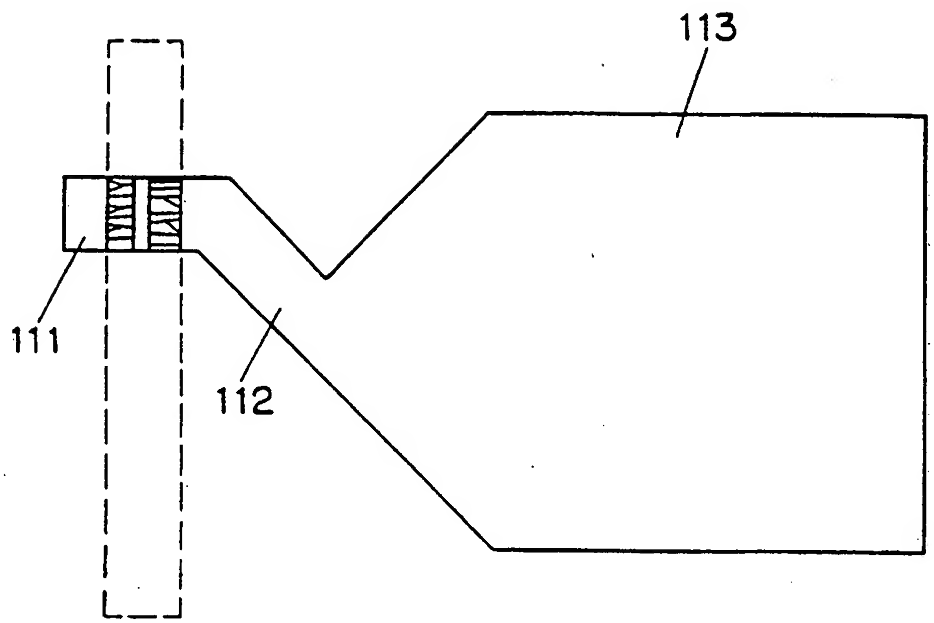


FIG. 11A

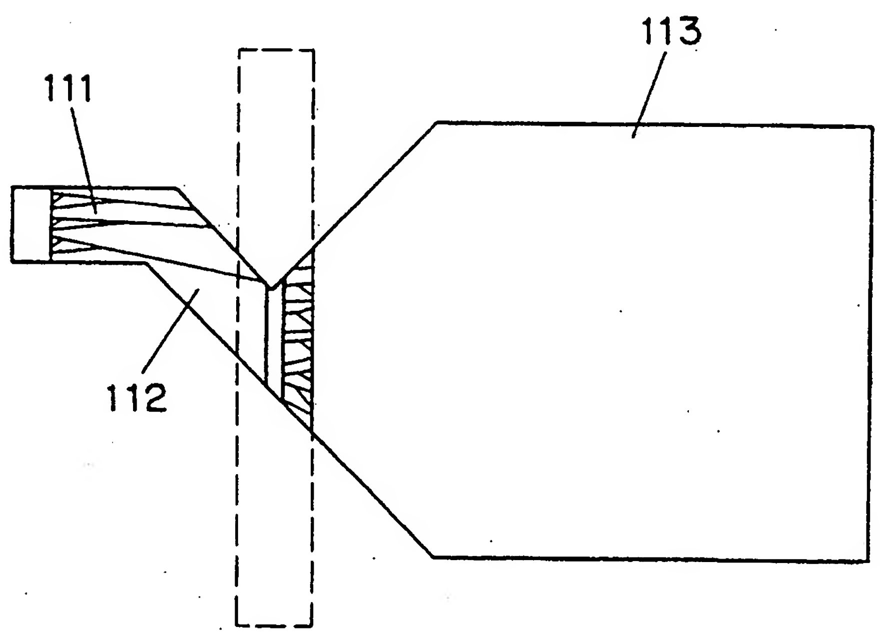


FIG. 11B

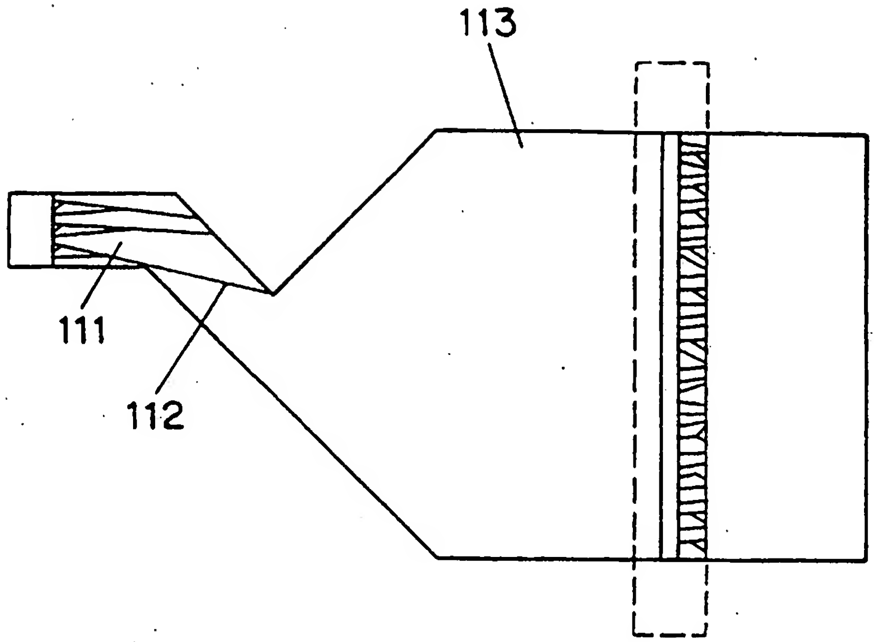


FIG. 11C

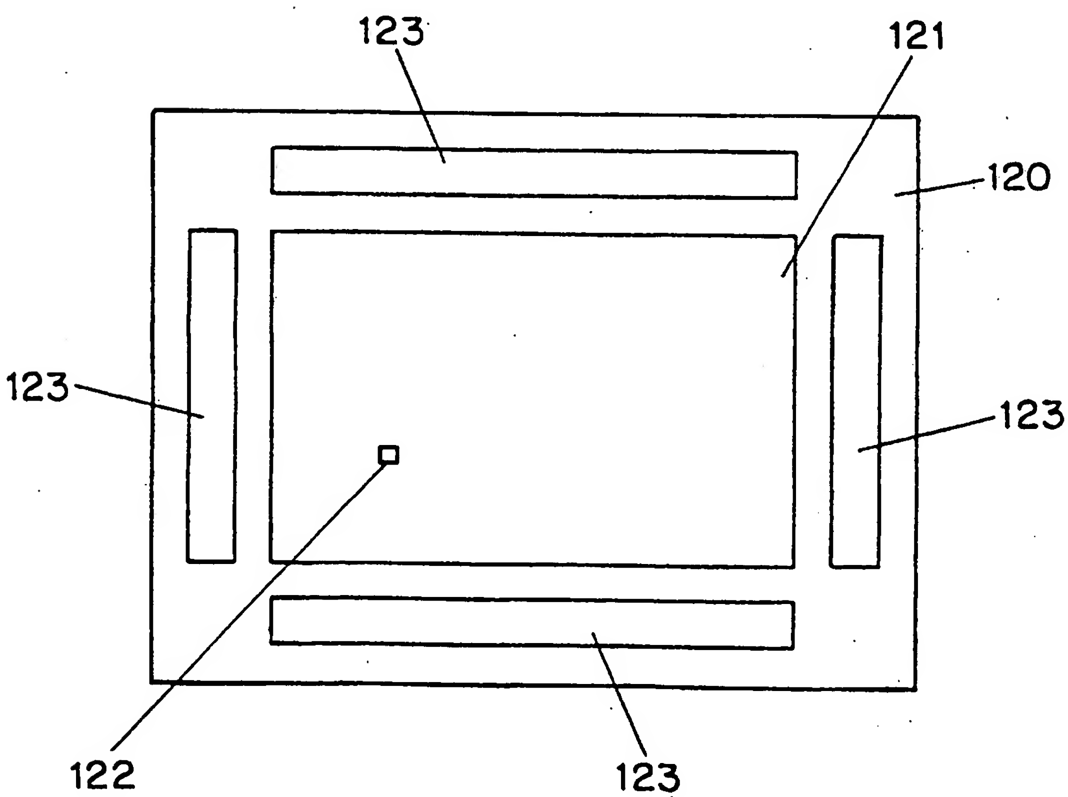


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/07730

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :G09G 3/36; H01L 21/20, 21/302; C30B 13/06.
US CL : 117/904; 427/ 89,109, 173, 174,973; 355/43/46/53
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 117/904; 427/ 89,109, 173, 174,973; 355/43/46/53

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,382,658 A (SHIELDS et al.) 10 May 1983.	NONE
A	US Re. 33,836 B (RESOR III et al.) 03 may 1992	NONE
A	US 5,204,659 A (SARMA) 20 April 1993.	NONE
A	US 5,061,655 A (IPPOSHI et al.) 29 October 1991.	NONE
A	US 5,409,867 A (ASANO) 25 April 1995	NONE
A,P	US 5,496,768 A (KUDO) 05 March 1996.	NONE
A,E	US 5,529,951 A (NOGUCHI et al.) 25 June 1996.	NONE

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 MARCH 1997	14 APR 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks	Authorized officer Upendra Roy

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/07730

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,855,014 A (KAKIMOTO ET AL.) 08 August 1989.	none
A	US 4,727,047 A (BOZLER et al.) 23 February 1988.	NONE

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 February 2004 (26.02.2004)

PCT

(10) International Publication Number
WO 2004/017379 A2

(51) International Patent Classification[7]: H01L

(21) International Application Number: PCT/US2003/025946

(22) International Filing Date: 19 August 2003 (19.08.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/405,084 19 August 2002 (19.08.2002) US

(71) Applicant (*for all designated States except US*): THE TRUSTEES OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK [US/US]; 116th Street and Broadway, New York, NY 10027 (US).

(72) Inventor; and
(75) Inventor/Applicant (*for US only*): IM, James, S. [US/US]; 520 West 114th Street, Apt. 74, New York, NY 10025 (US).

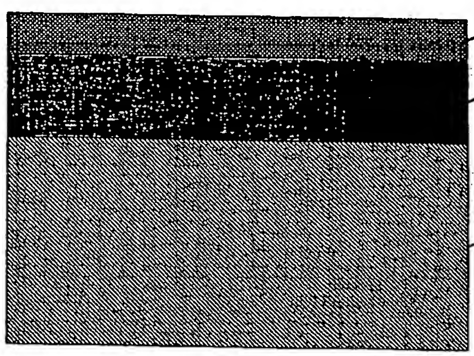
(74) Agents: TANG, Henry et al.; Baker & Botts, LLP, 30 Rockefeller Plaza, New York, NY 10112-4498 (US).

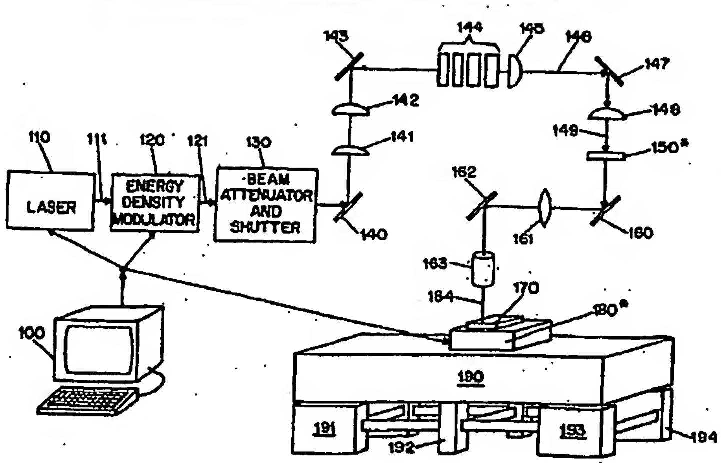
(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: PROCESS AND SYSTEM FOR LASER CRYSTALLIZATION PROCESSING OF FILM REGIONS ON A SUBSTRATE TO PROVIDE SUBSTANTIAL UNIFORMITY, AND A STRUCTURE OF SUCH FILM REGIONS





(57) Abstract: A process and system for processing a thin film sample (e.g., a semiconductor thin film), as well as the thin film structure are provided. In particular, a beam generator can be controlled to emit at least one beam pulse. With this beam pulse, at least one portion of the film sample is irradiated with sufficient intensity to fully melt such section of the sample throughout its thickness, and the beam pulse having a predetermined shape. This portion of the film sample is allowed to resolidify, and the re-solidified at least one portion is composed of a first area and a second area. Upon the re-solidification thereof, the first area includes large grains, and the second area has a region formed through nucleation. The first area surrounds the second area and has a grain structure which is different from a grain structure of the second area. The second area is configured to facilitate thereon an active region of an electronic device.

WO 2004/017379 A2

Published:
— *without international search report and to be republished upon receipt of that report*

PROCESS AND SYSTEM FOR LASER CRYSTALLIZATION PROCESSING OF FILM REGIONS ON A SUBSTRATE TO PROVIDE SUBSTANTIAL UNIFORMITY, AND A STRUCTURE OF SUCH FILM REGIONS

SPECIFICATION

RELATED APPLICATION

This application claims priority to United States Provisional Application No. 60/405,084, which was filed on August 19, 2002, and is incorporated by reference.

NOTICE OF GOVERNMENT RIGHTS

The U.S. Government may have certain rights in this invention pursuant to the terms of the Defense Advanced Research Project Agency award number N66001-98-1-8913.

FIELD OF THE INVENTION

The present invention relates to techniques for processing of films, and more particularly to techniques for processing films to obtain a substantially uniform grain region for placing at least an active region of a thin-film transistor ("TFT") therein.

BACKGROUND OF THE INVENTION

Semiconductor films, such as silicon films, are known to be used for providing pixels for liquid crystal display devices. Such films have previously been processed (i.e., irradiated by an excimer laser and then crystallized) via excimer laser annealing ("ELA") methods. However, the semiconductor films processed using such known ELA methods often suffer from microstructural non-uniformities, which manifest themselves in availing a non-uniform performance of thin-film transistor ("TFT") devices fabricated on such films. The non-uniformity generally stems from the intrinsic pulse-to-pulse variations in the output energy of the excimer lasers irradiating the semiconductor films. The above-described non-uniformity could

manifest itself in, for example, a noticeable difference in a brightness level of the pixels in one area of the display as compared to the brightness in other areas thereof.

Significant effort has gone into the refinement of "conventional" ELA (also known as line-beam ELA) processes in the attempt to reduce or eliminate the non-uniformity. For example, U.S. Patent No. 5,766,989 issued to Maegawa et al., the entire disclosure of which is incorporated herein in its entirety by reference, describes the ELA methods for forming polycrystalline thin film and a method for fabricating a thin-film transistor. This publication attempts to address the problem of non-uniformity of characteristics across the substrate, and provide certain options for apparently suppressing such non-uniformities.

However, the details of the beam-shaping approach used in conventional ELA methods make it extremely difficult to reduce the non-uniformities in the semiconductor films. This is especially because the energy fluence described above may be different for each beam pulse, and thus non-uniformity may be introduced into sections of the semiconductor thin film upon irradiation, solidification and crystallization.

Techniques for fabricating large grained single crystal or polycrystalline silicon thin films using sequential lateral solidification are known in the art. For example, in U.S. Patent No. 6,322,625 issued to Im and U.S. patent application serial no. 09/390,537, the entire disclosures of which are incorporated herein by reference, and which is assigned to the common assignee of the present application, particularly advantageous apparatus and methods for growing large grained polycrystalline or single crystal silicon structures using energy-controllable laser pulses and small-scale translation of a silicon sample to implement sequential lateral solidification have been described. In these patent documents, it has been discussed in great detail that at least portions of the semiconductor film on a substrate are irradiated with a suitable radiation pulse to completely melt such portions of the film throughout their thickness. In this manner, when the molten semiconductor material solidifies, a crystalline structure grows into the solidifying portions from selected areas of the semiconductor film which did not undergo a complete melting.

This publication mentions that the small grain growth in regions in which nucleation may occur. As is known in the art, such nucleation generates small grained material in the area of the nucleation.

As was previously known to those having ordinary skill in the art of a sequential lateral solidification ("SLS") as described in U.S. Patent No. 6,322,625, which utilizes the irradiation of a particular area using beam pulses whose cross-sectional areas are large, it is possible for the nucleation to occur in such areas before a lateral crystal growth is effectuated in such area. This was generally thought to be undesirable, and thus the placement of the TFT devices within these area was avoided.

While certain TFT devices do not require a high performance level, they require good uniformity in certain applications. Accordingly, it may be preferable to generate substrates which include the semiconductor films that allow uniform small-grained material to be produced therein, without the need for a multiple irradiation of the same area on the semiconductor thin film.

SUMMARY OF THE INVENTION

One of the objects of the present invention is to provide an improved process and system to which can produce generally uniform areas on the substrate films such that the TFT devices can be situated in such areas. Another object of the present invention is to allow such areas to be nucleated (based on the threshold behavior of the beam pulse), and then solidified, such that upon re-solidification, the nucleated area becomes a region with uniform small grained material. It is also another object of the present invention to increase the speed to process the semiconductor films for their use with the liquid crystal displays or organic light emitting diode displays. It is still another object of the present invention to allow each irradiated area of the semiconductor thin film to be irradiated once, without the need to re-irradiate a substantial portion thereof, while still providing a good uniform material therein.

In accordance with at least some of these objectives as well as others that will become apparent with reference to the following specification, it has now been determined that the nucleated and small grained material have an extremely good uniformity (e.g., uniform grains). It was also ascertained that the grain size in such nucleated areas does not vary even in a significant manner if the beam pulses melting these areas have fluctuating energy densities. This is particularly the case when the beam's energy density stays above the required threshold for fully melting these areas throughout their thickness. For example, in the case of a semiconductor film which has a thickness of approximately 0.1 µm, the energy density of each beam pulse should be above 50 mJ/cm^2. Further, the uniformity in the thin film was found to be insensitive to a spatial non-uniformity of the beam incident on the semiconductor film so long as the minimum intensity of the beam is above the above-described threshold.

In one exemplary embodiment of the present invention, a process and system for processing a semiconductor thin film sample are provided. In particular, a beam generator can be controlled to emit at least one beam pulse. With this beam pulse, at least one portion of the film sample is irradiated with sufficient intensity to fully melt such section of the sample throughout its thickness. Such beam pulse may have a predetermined shape. This portion of the film sample is allowed to re-solidify, and the re-solidified portion is composed of a first area and a second area. Upon the re-solidification thereof, the first area includes large grains, and the second area has a small-grained region formed through nucleation. The first area surrounds the second area and has a grain structure which is different from a grain structure of the second area. The second area is configured to facilitate thereon an active region of a thin-film transistor ("TFT").

In another exemplary embodiment of the present invention, the first area has a first border and a second border which is provided opposite and parallel to the first border of the first area. Also, the second area has a third border and a fourth border which is provided opposite and parallel to the third border of the second area. A distance between the first border and the second border is smaller than a distance between the third border and the fourth border. The second area preferably

corresponds to at least one pixel. In addition, the second area may have a cross-section for facilitating thereon all portions of the TFT. It is also possible for a portion of the first area to contain thereon a small section of the TFT. A size and a position of the first area with respect to the second area can be provided such that there is no effect or a negligible effect on a performance of the TFT by the first area.

According to yet another embodiment of the present invention, the thin film sample can be translated for a predetermined distance. With a further beam pulse, a further portion of the film sample can be irradiated. The further portion is provided at a distance from such portion that substantially corresponds to the predetermined distance. This further portion of the film sample is allowed to re-solidify, the re-solidified portion being composed of a third area and a fourth area. In addition, the third area can surround the fourth area, and at least one section of the third area at least partially overlaps at least one section of the first area. Further, upon the re-solidification thereof, the third area has laterally grown grains, and the fourth area has a nucleated region. The fourth area can also be composed of edges which are provided away from edges of the second area. Furthermore, the fourth area may be composed of edges which are approximately border edges of the second area, and the edges of the fourth area may not necessarily extend into any section of the first area. The beam pulse may have a fluence which is substantially the same as a fluence of the further beam pulse (or different therefrom).

In still another embodiment of the present invention, the thin film sample can be translated for a predetermined distance. Then, a further portion of the film sample can be irradiated using the beam pulse. The further portion is provided at a distance from such portion that substantially corresponds to the predetermined distance. The film sample may be a pre-patterned silicon thin film sample or a continuous silicon thin film sample. In addition, the thin film sample can be translated for a predetermined distance, and a further portion of the film sample may be irradiated using at least one beam pulse. The further portion is preferably provided at a distance from this portion that substantially corresponds to the predetermined distance. In addition, the film sample can be delivered to a first relative pre-calculated position of the further portion of the film sample to be irradiated. After

such delivery, the film sample may be provided at a second relative pre-calculated position whose distance is different from the predetermined distance.

According to further embodiment of the present invention, the thin film sample can again be translated for a predetermined distance. Then, the translation of the film sample may be stopped, and vibrations of the film sample to allowed to settle. Thereafter, a further portion of the thin film is irradiated using at least one beam pulse, with the further portion being provided at a distance from such portion that substantially corresponds to the predetermined distance. Then, the portion of the film sample is irradiated with a further beam pulse, and allowed to re-solidify. A fluence of the beam pulse is different from a fluence of the further beam pulse (e.g., less than the fluence of the beam pulse).

According to still further embodiment of the present invention, a location of the first area is determined so as to avoid a placement of the active region of the TFT thereon. The beam pulse preferably includes a plurality of beamlets, and the first and second areas are irradiated by the beamlets. The semiconductor thin film sample may be a silicon thin film sample, and possibly composed of silicon, germanium or an alloy thereof. The semiconductor thin film may have a thickness approximately between 100Å and 10,000Å. Portions of the beam pulse can be masked to produce at least one masked beam pulse, such that the masked beam pulse is used to irradiate the portion of the film sample. The large grains provided in the first area may be laterally-grown grains, and the laterally-grown grains of the first area can be equiaxed grains.

According yet another embodiment of the present invention, a semiconductor thin film sample is provided which has a first area and a second area. The first area preferably has large grains therein. The second area is surrounded by the first area and includes a region formed through nucleation of at least one section of the semiconductor thin film in which the second area is situated. The structure of the grains of the first area is different from a structure of the grains of the second area. The second area is preferably configured to facilitate thereon an active region of a thin-film transistor ("TFT").

The accompanying drawings, which are incorporated and constitute part of this disclosure, illustrate a preferred embodiment of the invention and serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a schematic block diagram of an exemplary embodiment of an irradiation system according to the present invention which irradiates particular areas of a semiconductor thin film of a sample so that they nucleate and solidify to produce uniform small grained regions;

Fig. 1B is an enlarged cross-sectional side view of the sample which includes the semiconductor thin film;

Fig. 2 is a top exploded view of an exemplary embodiment of the sample conceptually subdivided, and having a semiconductor thin film thereon on which a process according to the present invention is performed for the entire surface area a semiconductor thin film using the exemplary system of Fig. 1A;

Fig. 3 is a top view of a first exemplary embodiment of a mask according to the present invention which has a beam-blocking area surrounding one open or transparent area, and which can be used with the exemplary system of Fig. 1A to mask the beam pulses generated by a laser beam source into a patterned beam pulse, such that such masked beam pulses irradiate the particular areas on the semiconductor film;

Figs. 4A-4D are irradiations, by the radiation beam pulse which is masked by the mask of Fig. 3, and then re-solidifications and crystallizations of the particular portions of the semiconductor film provided on the sample for a first exemplary conceptual column of the sample at various sequential stages of the exemplary embodiment according to the process of the present invention;

Figs. 4E-4F are irradiations, by the radiation beam pulse which is masked by the mask of Fig. 3, and then re-solidifications and crystallizations of the particular portions of the semiconductor film provided on the sample for a second

exemplary conceptual column of the sample at two exemplary sequential stages of the processing according to the process of the present invention;

Fig. 5A is a top view of a second exemplary embodiment of the mask according to the present invention which has a beam-blocking area surrounding multiple small open or transparent areas or slits, and which can be used with the exemplary system of Fig. 1A to mask the beam pulses generated by a beam source into patterned beamlets, such that such masked beamlet pulses irradiate the particular areas on the semiconductor film;

Fig. 5B is an enlarged view of the beamlets of the second embodiment of the mask illustrated in Fig. 5A;

Figs. 6A-6D are irradiations, by the radiation beam pulse intensity pattern which is masked by the mask of Fig. 5, and then re-solidifications and crystallizations of the particular portions of the semiconductor film provided on the sample for the first exemplary conceptual column of the sample at various sequential stages of the first exemplary embodiment of the exemplary embodiment according to the process of the present invention;

Fig. 7 is an illustration of the semiconductor thin film provided on the sample, and such thin film being irradiated by the beam pulse having a cross-section that is patterned by a mask having a beam-blocking area surrounding one long and narrow open or transparent area, and which can be used with the exemplary system of Fig. 1A;

Fig. 8A is an illustration of the two particular areas irradiated, re-solidified and crystallized areas corresponding to the areas of Figs. 4D and 6D in which the entire TFT device is situated in the small uniformed grained region formed through nucleation;

Fig. 8B is an illustration of the two particular areas irradiated, re-solidified and crystallized areas corresponding to the areas of Figs. 4D and 6D in which only the entire cross-section of the active region of the TFT device is situated in the small uniformed grained region formed through nucleation, while other regions are provided over border areas between the crystallized areas;

Fig. 9 is a flow diagram representing an exemplary processing procedure of the present invention under at least partial control of a computing arrangement of Fig. 1A using the exemplary techniques of the present invention of Figs. 4A-4F and 6A-6D; and

Fig. 10 is a flow diagram representing another exemplary processing procedure of the present invention under at least partial control of a computing arrangement of Fig. 1A using the exemplary techniques of the present invention of Figs. 4A-4F and 6A-6D, and in which the beam source of Fig. 1A is triggered based on the positions of the semiconductor film with respect to the impingement of the beam.

DETAILED DESCRIPTION

It should be understood that various systems according to the present invention can be utilized to generate, nucleate, solidify and crystallize one or more areas on the semiconductor (e.g., silicon) film which have uniform material therein such that at least an active region of a thin-film transistor ("TFT") can be placed in such areas. The exemplary embodiments of the systems and process to achieve such areas, as well as of the resulting crystallized semiconductor thin films shall be described in further detail below. However, it should be understood that the present invention is in no way limited to the exemplary embodiments of the systems, processes and semiconductor thin films described herein.

Certain systems for providing a continuous motion SLS are described in U.S. Patent Application Serial No. 09/526,585 (the " '585 application"), the entire disclosure of which is incorporated herein by reference. Substantially similar systems according to the exemplary embodiment of the present invention can be employed to generate the nucleated, solidified and crystallized portions of the semiconductor film described above on which it is possible to situate the active regions of the TFT device. In particular, the system according to the present invention is used on a sample 170 which has an amorphous silicon thin film thereof that is being irradiated by irradiation beam pulses to promote the nucleation, subsequent solidification and crystallization of the particular areas of the semiconductor thin film. The exemplary system includes a

beam source 110 (e.g., a Lambda Physik model LPX-315I XeCl pulsed excimer laser) emitting an irradiation beam (e.g., a laser beam), a controllable beam energy density modulator 120 for modifying the energy density of the laser beam, a MicroLas two plate variable attenuator 130, beam steering mirrors 140, 143, 147, 160 and 162, beam expanding and collimating lenses 141 and 142, a beam homogenizer 144, a condenser lens 145, a field lens 148, a projection mask 150 which may be mounted in a translating stage (not shown), a 4×-6× eye piece 161, a controllable shutter 152, a multi-element objective lens 163 for focusing a radiation beam pulse 164 onto the sample 170 having the semiconductor thin film to be processed mounted on a sample translation stage 180, a granite block optical bench 190 supported on a vibration isolation and self-leveling system 191, 192, 193 and 194, and a computing arrangement 100 (e.g., a general purpose computer executing a program according to the present invention or a special-purpose computer) coupled to control the beam source 110, the beam energy density modulator 120, the variable attenuator 130, the shutter 152 and the sample translation stage 180.

The sample translation stage 180 is preferably controlled by the computing arrangement 100 to effectuate translations of the sample 170 in the planar X-Y directions, as well as in the Z direction. In this manner, the computing arrangement 100 controls the relative position of the sample 40 with respect to the irradiation beam pulse 164. The repetition and the energy density of the irradiation beam pulse 164 are also controlled by the computer 100. It should be understood by those skilled in the art that instead of the beam source 110 (e.g., the pulsed excimer laser), the irradiation beam pulse can be generated by another known source of short energy pulses suitable for completely melting throughout their entire thickness selected areas of the semiconductor (e.g., silicon) thin film of the sample 170 in the manner described herein below. Such known source can be a pulsed solid state laser, a chopped continuous wave laser, a pulsed electron beam and a pulsed ion beam, etc. Typically, the radiation beam pulses generated by the beam source 110 provide a beam intensity in the range of 10 mJ/cm^2 to 1J/cm^2, a pulse duration (FWHM) in the range of 10 to 103 nsec, and a pulse repetition rate in the range of 10 Hz to 104 Hz.

While the computing arrangement 100, in the exemplary embodiment of the system shown in Fig. 1A, controls translations of the sample 170 via the sample stage 180 for carrying out the processing of the semiconductor thin film of the sample 170 according to the present invention, the computing arrangement 100 may also be adapted to control the translations of the mask 150 and/or the beam source 110 mounted in an appropriate mask/laser beam translation stage (not shown for the simplicity of the depiction) to shift the intensity pattern of the irradiation beam pulses 164, with respect to the semiconductor thin film of the sample 170, along a controlled beam path. Another possible way to shift the intensity pattern of the irradiation beam pulse is to have the computer 100 control a beam steering mirror. The exemplary system of Fig. 1 may be used to carry out the processing of the silicon thin film of the sample 170 in the manner described below in further detail. The mask 150 should be used by the exemplary system of the present invention to well define the profile of the resulting masked beam pulse 164 and to reduce the edge regions of the portions of the semiconductor thin film when these portions are irradiated by such masked beam pulse 164 and then crystallized.

As illustrated in Fig. 1B, the semiconductor thin film 175 of the sample 170 can be directly situated on e.g., a glass substrate 172, and may be provided on one or more intermediate layers 177 there between. The semiconductor thin film 175 can have a thickness between 100Å and 10,000Å (1μm) so long as at least certain necessary areas thereof can be completely melted throughout their entire thickness. According to an exemplary embodiment of the present invention, the semiconductor thin film 175 can be composed of silicon, germanium, silicon germanium (SeGe), all of which preferably have low levels of impurities. It is also possible to utilize other elements or semiconductor materials for the semiconductor thin film 175. The intermediary layer 177, which is situated immediately underneath the semiconductor thin film 175, can be composed of silicon oxide (SiO_2), silicon nitride (Si_3N_4), and/or mixtures of oxide, nitride or other materials that are suitable for promoting nucleation and small grain growth within the designated areas of the semiconductor thin film 175 of the sample 170. The temperature of the glass substrate 172 can be between room temperature and 800°C. Higher temperatures of the glass substrate 172 can be

accomplished by preheating the substrate 172 which would effectively allow larger grains to be grown in the nucleated, re-solidified, and then crystallized areas of the semiconductor thin film 175 of the sample 170 due to the proximity of the glass substrate 172 to the thin film 175.

Fig. 2 shows an enlarged view of an exemplary embodiment of the semiconductor thin film 175 (e.g., an amorphous silicon thin film) of the sample 170, and the relative translation paths of the beam pulse 164 with respect to the locations on the sample 170. This exemplary sample 170 has exemplary dimensions of 40 cm in the Y direction by 30 cm in the X direction. The sample 170 can be conceptually subdivided into a number of columns (e.g., a first conceptual column 205, a second conceptual column 206, a third conceptual column 207, etc.). The location/size of each conceptual column may be stored in a storage device of the computing arrangement 100, and utilized by the computing arrangement 100 for later controlling the translation of the sample 170, and/or firing of the beam by the beam source 110 on these locations of the semiconductor thin film 175, or on other locations that are based on the stored locations. Each of the columns 205, 206, 207, etc. is dimensioned, e.g., ½ cm in the Y direction by 30 cm in the X direction. Thus, if the sample 170 is sized 40 cm in the Y direction, the sample 150 may be conceptually subdivided into eighty (80) columns. The sample 170 may also be conceptually subdivided into such columns having other dimensions (e.g., 1 cm by 30 cm columns, 2 cm by 30 cm columns, 2 cm by 30 cm columns, etc.). In fact, there is absolutely no restrictions on the dimensions of the conceptual columns of the sample 170 so long as the beam pulse 164 is capable of irradiating and completely melting certain areas of the semiconductor thin film 175 in such columns so as to promote nucleation, solidification, and small grain growth within such areas for forming uniform areas on the film sample 175 to allow at least the active region of the TFT device to be placed completely therein without a concern of non-uniformity therein. The location/dimension of each column, and the locations thereof, are stored in the storage device of the computing arrangement 100, and utilized by such computing arrangement 100 for controlling the translation of the translation stage 180 with

respect to the beam pulse 164 and/or the firing of the beam 111 by the beam source 110.

The semiconductor thin film 175 can be irradiated by the beam pulse 164 which is patterned using the mask 150 according to a first exemplary embodiment of the present invention as shown in Fig. 3. The first exemplary mask 150 is sized such that its cross-sectional area is larger than that of the cross-sectional area of the beam pulse 164. In this manner, the mask 150 can pattern the pulsed beam to have a shape and profile directed by the open or transparent regions of the mask 150. In this exemplary embodiment, the mask 150 includes a beam-blocking section 155 and an open or transparent section 157. The beam-blocking section 155 prevents those areas of the pulsed beam impinging such section 155 from being irradiated there-through, thus preventing the further entering the optics of the exemplary system of the present invention shown in Fig. 1A to irradiate the corresponding areas of the semiconductor thin film 175 provided on the sample 170. In contrast, the open or transparent section 157 allows the portion of the beam pulse 164 whose cross-section corresponds to that of the section 157 to enter the optics of the system according to the present invention, and irradiate the corresponding areas of the semiconductor thin film 175. In this manner, the mask 150 is capable of patterning the beam pulse 164 so as to impinge the semiconductor thin film 175 of the sample 170 at predetermined portions thereof as shall be described in further detail below.

A first exemplary embodiment of the process according to the present invention shall now be described with reference to the irradiation of the semiconductor thin film 175 of the sample 170 as illustrated in Figs. 4A-4F. In this exemplary process of the present invention, the beam 111 is shaped by the exemplary mask 150 of Fig. 3, and the exemplary irradiation and/or impingement of the semiconductor thin film 175 of the sample 170 is shown in Fig. 2. For example, the sample 170 may be translated with respect to the beam pulse 164, either by moving the mask 150 or the sample translation stage 180, in order to irradiate selective areas of the semiconductor thin film 175 of the sample 170. For the purposes of the foregoing, the length and width of the laser beam 149 may be greater than 1 cm in the X-direction by ½ cm in the Y-direction (e.g., a rectangular shape) so that it can be

shaped by the mask 150 of Fig. 3. However, it should be understood the pulsed laser beam 149 is not limited to such shape and size. Indeed, other shapes and/or sizes of the laser beam 149 are, of course, achievable as is known to those having ordinary skill in the art (e.g., shapes of a square, triangle, circle, etc.).

After the sample 170 is conceptually subdivided into columns 205, 206, 207, etc., a pulsed laser beam 111 is activated (by actuating the beam source 110 using the computing device 100 or by opening the shutter 130), and produces the pulsed laser beamlets 164 which impinges on a first location 220 which is away from the semiconductor thin film 175. Then, the sample 170 is translated and accelerated in the forward X direction under the control of the computing arrangement 100 to reach a predetermined velocity with respect to the fixed position beamlets in a first beam path 225.

In one exemplary variation of the process of the present invention, the pulsed beamlets 164 can reach a first edge 210' of the sample 170 preferably when the velocity of the movement of the sample 170 with respect to the pulsed laser beam 149 reaches the predetermined velocity. Then, the sample 170 is continuously (i.e., without stopping) translated in the -X direction at the predetermined velocity so that the pulsed beamlets 164 continue irradiating successive portions of the sample 170 for an entire length of a second beam path 230.

After passing the first edge 210', the beam pulse 164 impinges and irradiates a first area 310 of the semiconductor thin film 175, preferably with enough intensity to completely melt such area throughout its thickness, as illustrated in Fig. 4A. Then, as shown in Fig. 4B, this first area 310 is allowed to solidify and crystallize, thereby forming two regions therein – a first small-grained region 315 and a first laterally-grown region 318. The first small-grained region 315 is formed after the nucleation of the large section within the first area 310. The dimensions of this region 315 are slightly smaller that the dimensions of the beam pulse 164 irradiating the first area 310, with the first small-grained region 315 being surrounded by the first laterally-grown region 318 (the details of which are described herein below).

The first laterally-grown region 318 is formed by laterally growing the grains from the borders between the unmelted portions of the semiconductor thin film 175 and the first melted area 310. The grains in the first laterally-grown region 318 grown from these borders toward the center of the first melted area for a predetermined distance, to reach the first small-grained region 315 and form a border there between. This predetermined distance is controlled by the rate of re-solidification of the first melted area 310. For example, the predetermined distance can be between 1 μm and 5 μm. Therefore, the first laterally-grown region 318 is significantly smaller that the first small-grained region 315 which it surrounds. Generally, the grains of the region 315 are smaller than the grains of the region 318. However, the small-grained material in the first small-grained region 315 provides a good uniformity for the placement of the TFT devices, and at least the active regions thereof, in such uniform small-grained region. For the purposes of the present invention, it is undesirable to position the active regions of the TFT devices on such small-grained regions.

Thereafter, as shown in Fig. 4C, the sample 170 is continued to be translated (or the mask 150 is configured to be adjusted) such that the beam pulse 164 irradiates and completely melts (throughout its thickness) a second area 320 of the semiconductor thin film 175. This second area 320 which can be a subsequent area immediately following the first area 320 in the first conceptual column 205 along the +X direction. Similarly to the first area 310, the second area 320 re-solidifies and crystallizes into a second small-grained region 325 and a second laterally-grown region 328, which correspond to the characteristics and dimensions of the first small-grained region 315 and the first laterally-grown region 318, respectively. If, during the irradiation of the second area 320, the beam pulse 164 slightly overlaps the first laterally-grown region 318, then upon re-solidification, the grains in this region 318 seed and laterally grow a portion of the completed melted second area 320 which is immediately adjacent to the first laterally-grown region 318. In this manner, the adjacent section of the second laterally-grown region 328 is seeded by the first laterally-grown region 318 to laterally grow grains therefrom. The resultant crystallized second area 320 is illustrated in Fig. 4D. It is also within the scope of the

present invention for the second area 320 to be provided at a distance from the crystallized first area 310. Accordingly, the sections of the second laterally-grown region 328 which is situated closest to the crystallized first laterally-grown region 318 is seeded by the grains from an un-irradiated section between the first area 310 and the second area.

The translation and irradiation of the first conceptual column 205 of the semiconductor thin film 175 continues until all areas 310, 320, ..., 380, 390 (and their respective small-grained regions 315, 325, ..., 385, 395 and laterally-grown regions 318, 328, ..., 388, 398) in this first conceptual column 205 is continued until the pulsed beamlets 164 reach a second edge 210" of the sample 170, as illustrated in Fig. 4E. The crystallization of the areas 310, 320, ..., 380, 390 along the first conceptual column 205 is performed in a substantially repetitive manner. When the beam pulse 164 passes the second edge 210", the translation of the sample 170 may be slowed with respect to the beam pulse 164 (in a third beam path 235) to reach a second location 240 (Fig. 2). It should be noted that it is not necessary to shut down the pulsed beam 111 after the beam pulse 164 has crossed the second edge 210" of the sample 170 because it is no longer irradiating the sample 170.

While being away from the sample 170 and the second edge 210", the sample is translated in a -Y direction to a third location 247 via a fourth beam path 245 so as to be able to irradiate the sections of the semiconductor thin film 175 along the second conceptual column 206. Then, the sample 170 is allowed to settle at that location 247 to allow any vibrations of the sample 170 that may have occurred when the sample 170 was translated to the third location 247 to cease. Indeed, for the sample 170 to reach the second conceptual column 206, it is translated approximately ½ cm for the columns having a width (in the -Y direction) of ½ cm. The sample 170 is then accelerated to the predetermined velocity via a fourth beam path 250 in the –X direction so that the impingement of the semiconductor thin film 175 by the beam pulse 164 reaches, and then bypasses the second edge 210".

Thereafter, the sample 170 is translated along a fifth beam path 255, and the exemplary process described above with respect to the irradiation of the first

column 205 may then be repeated for the second conceptual column 206 to irradiate further areas 410, 420, and their respective small-grained regions 415, 425 and laterally-grown regions 418, 428 while translating the sample in the +X direction. In this manner, all conceptual columns of the sample 170 can be properly irradiated. Again, when the beam pulse 164 reaches the first edge 210', the translation of the sample 170 is decelerated along a sixth beam path 260 to reach a fourth location 265. At that point, the sample 170 is translated in the –Y direction along the seven beam path 270 for the beam pulse to be outside the periphery of the sample 170 to reach fifth location 272, and the translation of the sample 170 is allowed to be stopped so as to remove any vibrations from the sample 170. Thereafter, the sample 170 is accelerated along the eighth beam path 275 in the –X direction so that the beam pulse 164 reaches and passes the first edge 210' of the sample 170, and the beam pulse 164 irradiates and completely melts certain areas in the third conceptual column 207 so that they can crystallize in substantially the same manner as described above for the areas 310, 320, ..., 380, 390 of the first conceptual column 205 and the areas 410, 420, ... of the second conceptual column 206.

This procedure may be repeated for all conceptual columns of the semiconductor thin film 175, for selective columns of particular sections of the thin film 175 which are not necessarily conceptually subdivided into columns. In addition, it is possible for the computing arrangement 100 to control the firing of the beam 111 by the beam source 110 based on the predefined location stored in the storage device of the computing arrangement 100 (e.g., instead of irradiating the semiconductor thin film 175 by setting predetermined pulse durations). For example, the computing arrangement 100 can control the beams source 110 to generate the beam 111 and irradiate only at the predetermined locations of certain areas of the thin film 175 with its corresponding beam pulse 164, such that these locations are stored and used by the computing arrangement 100 to initiate the firing of the beam 111 which results in the irradiation by the beam pulse only when the sample 170 is translated to situate those areas directly in the path of the beam pulse 164. The beam source 110 can be fired via the computing arrangement 100 based on the coordinates of the location in the X direction.

In addition, it is possible to translate the sample 170 in a manner which is not necessary continuous, when the path of the irradiation of the beam pulse 164 points to the areas on the semiconductor thin film 175 to be melted and crystallized. Thus, it is possible for the translation of the sample 170 to be stopped in the middle of the sample 170, with the area in the middle being irradiated, completely melted, and then re-solidified and crystallized. Thereafter, the sample 170 can be moved so that another section of the semiconductor thin film 175 is arranged in the path of the beam pulse 164, such that the translation of the sample is then stopped again and the particular section is irradiated and completely melted in accordance with the exemplary embodiment of the process described in great detail above, as well as the embodiments of the process which shall be described below.

According to the present invention, any mask described and shown herein and those described and illustrated in the '535 application may be used for the process and system according to the present invention. For example, instead of using the mask shown in Fig. 3 which allows the semiconductor thin film 175 to be flood-irradiated, a second exemplary embodiment of the mask 150' illustrated in Fig. 5A can be utilized. In contrast to the mask 150 of Fig. 3 which has a single open or transparent region 157, the mask 150' has multiple open or transparent regions 450 which are separated from one another by beam-blocking regions 455. The open or transparent regions 450 of the mask 150' can also be referred to as "slits." These slits permit small beam pulses (or beamlets) to irradiate there-through and completely melt the areas of the semiconductor thin film 175 that they impinge. An enlarged illustration of one of the slits 450 is provided in Fig. 5B, which shows that the dimensions of the slits 450 can be 0.5 μm by 0.5 μm. It should be clearly understood that other dimensions of the slits are possible, and are within the scope of the present invention. For example, the slits can have a rectangular shape, a circular shape, a triangular shape, a chevron shape, a diamond shape, etc.

Figs. 6A-6D show an exemplary progression of a second embodiment of the process according to the present invention in which a plurality of successive areas along the first conceptual column 205 of the semiconductor thin film 175 is irradiated by the beam pulse 164 (comprised of beamlets) which is shaped by the

mask 150' of Fig. 5A. The translation of the sample 170 with respect to the impingement thereof by the beam pulse 164 is substantially the same as the translation described above with reference to Figs. 4A-4F. The difference between the irradiation of the areas 310, 320, ..., 380, 390, 410, 420 by the beam pulse 164 shaped by the mask 150 of Fig. 3 and the areas 460, 470 by the beam pulse 164 shaped by the mask 150' is that substantially the entire areas 310, 320, ... , 380, 390, 410, 420 are irradiated and completely melted, as opposed to only certain small portions 462 of the areas 460, 470 are irradiated and completely melted throughout their entire thickness.

Similarly to the area 310 in Fig. 4A, the portions 462 of the area 460 are irradiated and completely melted as illustrated in Fig. 6A. Thereafter, the portions 462 are re-solidified to form the small-grained regions 465 (due to nucleation), and the laterally grown regions 468 as shown in Fig. 4B. Similarly to the first small-grained regions 315, the small-grained regions 465 of the respective portions 462 have small grain uniform materials therein, and are sized such that at least an active region of the TFT device (and possible the entire TFT device) can be placed within each such region 465. The small grain uniform material of the region 465 is formed due to the nucleation and re-solidification of this region. As shown in Fig. 6C, upon the translation of the sample 170 in the –X direction, portions 472 of the area 470 are irradiated and completely melted in a substantially the same manner as the portions 462. In such manner, the small-grained regions 475 and the laterally-grown regions 478 of the area 470 are formed.

In addition, it is possible to utilize a third embodiment of a mask 150" according to the present invention as shown in Fig. 7 which has a long and narrow open or transparent region 490 so as to pattern and shape the beam 149 into the beam pulse 164. For example, the length of the region 490 can be 0.5 cm and the width thereof may be 0.1 mm. In this manner, each conceptual column of the sample 170 illustrated in Fig. 2 can be irradiated by the beam pulse 164 shaped by this mask 150". In addition, it may be possible for the length of the region 490 to be 30 cm. Thus, instead of subdividing the semiconductor thin film 175 into a number of conceptual columns, and irradiating each column separately, it is possible to irradiate and

completely melt selected portions of the semiconductor thin film 175 by translating the sample 170 in the –Y direction from one edge of the sample 170 to the opposite edge thereof. It is important that the small-grained uniform regions be formed using such processing technique such that it would be possible to situate the active regions of the respective TFT devices thereon.

Fig. 8A shows an illustration of the first and second irradiated, re-solidified and crystallized areas 510 and 520 possibly corresponding to the first and second areas 310, 320 of Figs. 4D and/or the adjacent portions 462 of the area 460 of Fig. 6D. In particular, Fig. 8A shows that the entire TFT devices 610, 620 can be situated within the respective uniform small-grained regions 515, 525 of the areas 510, 520. The first TFT device 610 situated in the small-grained region 515 of the area 510 includes a gate 612, a drain 614, a source 616 and an active region 618, all of which are provided away from the laterally-grown region 518. Similarly, for the second TFT device 610, its gate 622, drain 624, source 626, and especially active region 628 are also situated that they do not overlap the respective laterally-grown region 528 of the area 520.

Fig. 8B shows an illustration of the first and second irradiated, re-solidified and crystallized areas 510 and 520 also possibly corresponding to the adjacent portions 462 of the area 460 of Fig. 6D with the respective TFT devices 610', 620' provided thereon. In this exemplary embodiment, only respective active regions 618', 628' of the areas 510, 520 are provided within the respective uniform small-grained regions 515, 525 of the areas 510, 520, while other portions of the TFT devices 610', 620' are situated on the respective laterally-grown regions 518, 528 of the areas 510, 520. In particular, the first TFT device 610' includes an active region 618' which entirely situated in the small-grained region 515 of the area 510, while a gate 612', a drain 614' and a source 616' of this TFT device 610' overlap the laterally-grown region 518. Also, for the second TFT device 610', an active region 628' thereof is entirely situated within the respective small-grained region 525 of the area 520, while a gate 622', a drain 624' and a source 626' of the second TFT device 620' are provided directly on the respective laterally-grown regions 528 of the area 520. Also, the gate 622', is provided on a border region 500 between the small-grained

region 515 of the area 510 and the small-grained region 525 of the area 520. It should be understood that any one of the gate 612, 612', 622, 622', drain 614, 614', 624, 624' and source 616, 616', 626, 626' can be provided on the laterally-grown regions 518, 528 and the border region 500. In addition, according to still another embodiment of the present invention, it is possible to situate a small portion of the active regions 618', 628' of the respective TFT devices 610', 620' on the border region 500 or the laterally-grown regions 518, 528, while still having the major portions of these active regions 618', 628' provided within the small-grained regions 515, 525.

Fig. 9 show a flow diagram representing a first exemplary processing procedure of the present invention under at least a partial control of a computing arrangement of Fig. 1A which uses the techniques of the present invention of Figs. 4A-4F and 6A-6D. In step 1000, the hardware components of the system of Fig. 1A, such as the beam source 110, the energy beam modulator 120, and the beam attenuator and shutter 130 are first initialized at least in part by the computing arrangement 100. The sample 170 is loaded onto the sample translation stage 180 in step 1005. It should be noted that such loading may be performed either manually or automatically using known sample loading apparatus under the control of the computing arrangement 100. Next, the sample translation stage 180 is moved, preferably under the control of the computing arrangement 100, to an initial position in step 1010. Various other optical components of the system are adjusted and/or aligned either manually or under the control of the computing arrangement 100 for a proper focus and alignment in step 1015, if necessary. In step 1020, the irradiation/laser beam 111 is stabilized at a predetermined pulse energy level, pulse duration and repetition rate. In step 1024, it is preferably determined whether each beam pulse 164 has sufficient energy to fully melt the irradiated portions of the semiconductor thin film 175 without over-melting them. If that is not the case, the attenuation of the beam 111 is adjusted by the beams source 110 under the control of the computing arrangement 100 in step 1025, and step 1024 is executed again to determine if the there is sufficient energy to melt the portions of the semiconductor thin film.

In step 1027, the sample 170 is positioned to point the beam pulse 164 to impinge the first column of the semiconductor thin film. Then, in step 1030, the portions of the semiconductor thin film are irradiated and fully melted throughout their entire thickness using a masked intensity pattern or a shaped beam pulse (e.g., using the mask 150 or merely shaping the beam). Thereafter, the irradiated portions of the semiconductor thin film are allowed to solidify and crystallize such that the certain areas of the solidified portions have been nucleated and include uniform material therein so as to allow at least the active regions of the TFT devices to be placed entirely therein. In step 1035, it is determined whether the irradiation for the current conceptual column by the beam pulse has been completed. If no, in step 1045, the sample is continued to be irradiated with the next beam pulse 164. However, if in step 1035, it is determined that the irradiation and crystallization of the current conceptual column is completed, then it is determined in step 1045 whether there are any further conceptual columns of the sample 170 to be processed. If so, the process continues to step 1050 in which the sample 170 is translated to that the beam pulse 164 is pointed to the next conceptual column to be processed according to the present invention. Otherwise, in step 1055, the exemplary processing has been completed for the sample 170, and the hardware components and the beam 111 of the system shown in Fig. 1A can be shut off, and the process is terminated.

Fig. 10 shows a flow diagram representing a second exemplary processing procedure of the present invention under at least a partial control of a computing arrangement of Fig. 1A using the techniques of the present invention of Figs. 4A-4F and 6A-6D, in which it is preferable to irradiate the sample 170 based on preassigned locations on the semiconductor thin film 175. Steps 1100-1120 of this exemplary procedure are substantially the same as the steps 1000-1020 of the procedure of Fig. 9, and thus shall not be described herein in further detail. In step 1024, however, it is determined whether each beam 111 has enough energy to irradiate at least portions of the semiconductor thin film 175 such that the irradiated portion crystallize. If not, in step 1125, the attenuation for the beam pulse is adjusted, and the energy fluence is verified again. Upon the verification of the energy fluence of the beam pulse, the sample is moved to impinge a first column of the sample 170.

Then, in step 1130, the resultant beam 149 is passed through the mask 159 to shape the beam pulse, and shape the edge portions of the resultant pulse. Then, the sample 170 is continuously translated along the current column in step 1135. In step 1140, during the translation of the sample 170, the portions of the semiconductor thin film 175 are irradiated, and fully melted throughout their entire thickness, e.g., using a masked intensity pattern beam pulse to allow the irradiated portions to be crystallized. This irradiation of the portions of the semiconductor thin film 175 can be performed when the beam pulses 164 reach particular locations on the sample 170, which are pre-assigned by the computing arrangement 100 and stored in the storage device thereof. Thus, the beam source 110 can be fired upon the sample 170 reaching these locations with respect to the beam pulses 164. Thereafter, the irradiated portions of the semiconductor thin film 175 are allowed to solidify and crystallize such that the certain areas of the solidified portions have been nucleated, and include the uniform material therein so as to allow the active regions of the TFT devices to be placed thereon. Such processing is continued until the end of the current conceptual column on the semiconductor thin film 175 (e.g., the edge of the sample 170) is reached. In step 1145, it is determined whether there are any further conceptual columns of the sample 170 are to be processed. If so, the process continues to step 1150 in which the sample is translated so that the beam pulse 164 is pointed to the next conceptual column to be processed according to the present invention. Otherwise, in step 1155 is performed, which is substantially the same as that of step 1055 of Fig. 9.

The foregoing merely illustrates the principles of the invention. Various modifications and alterations to the described embodiments will be apparent to those skilled in the art in view of the teachings herein. For example, while the above embodiment has been described with respect to at least partial lateral solidification and crystallization of the semiconductor thin film, it may apply to other materials processing techniques, such as micro-machining, photo-ablation, and micro-patterning techniques, including those described in International patent application no. PCT/US01/12799 and U.S. patent application serial nos. 09/390,535, 09/390,537 and 09/526,585, the entire disclosures of which are incorporated herein by reference. The

various mask patterns and intensity beam patterns described in the above-referenced patent application can also be utilized with the process and system of the present invention. It should also be understood that while the systems and processes described above are directed for processing, e.g., semiconductor thin films, these techniques and systems can also be used to process other films, including metal thin films, etc.

It will thus be appreciated that those skilled in the art will be able to devise numerous systems and methods which, although not explicitly shown or described herein, embody the principles of the invention and are thus within the spirit and scope of the present invention.

What Is Claimed Is:

1. A method for processing a thin film sample, comprising the steps of:

(a) controlling a beam generator to emit at least one beam pulse;

(b) with the at least one beam pulse, irradiating at least one portion of the film sample with sufficient intensity to fully melt the at least one section of the sample throughout its thickness; and

(c) allowing the at least one portion of the film sample to re-solidify, the re-solidified at least one portion being composed of a first area and a second area, wherein, upon the re-solidification thereof, the first area includes large grains, and the second area has a small-grained region formed through nucleation,

wherein the first area surrounds the second area and has a grain structure which is different from a grain structure of the second area, and wherein the second area is configured to facilitate thereon an active region of an electronic device.

2. The method according to claim 1,

wherein the first area has a first border and a second border which is provided opposite and parallel to the first border of the first area,

wherein the second area has a third border and a fourth border which is provided opposite and parallel to the third border of the second area, and

wherein a distance between the first border and the second border is smaller than a distance between the third border and the fourth border.

3. The method according to claim 2, wherein the second area corresponds to at least one pixel.

4. The method according to claim 1, wherein the second area has a cross-section for facilitating thereon all portions of the electronic device.

5. The method according to claim 1, wherein a size and a position of the first area with respect to the second area are provided such that the first area provides either no effect or a negligible effect on a performance of the electronic device.

6. The method according to claim 1, further comprising the steps of:

(d) translating the thin film sample for a predetermined distance;

(e) with a further beam pulse, irradiating a further portion of the film sample, wherein the further portion is provided at a distance from the at least one portion that substantially corresponds to the predetermined distance; and

(f) allowing the further portion of the film sample to re-solidify, the re-solidified at least one portion being composed of a third area and a fourth area,

wherein the third area surrounds the fourth area, and wherein at least one section of the third area at least partially overlaps at least one section of the first area, and

wherein, upon the re-solidification thereof, the third area has laterally grown grains, and the fourth area has a nucleated region.

7. The method according to claim 6, wherein the fourth area is composed of edges which are provided away from edges of the second area.

8. The method according to claim 6, wherein the fourth area is composed of edges which approximately border edges of the second area, and wherein the edges of the fourth area do not extend into any section of the first area.

9. The method according to claim 6, wherein the at least one beam pulse has a fluence which is substantially the same as a fluence of the further beam pulse.

10. The method according to claim 6, wherein the at least one beam pulse has a fluence which is different from a fluence of the further beam pulse.

11. The method according to claim 1, further comprising the steps of:

(g) translating the thin film sample for a predetermined distance; and

(h) irradiating a further portion of the film sample using at least one beam pulse, wherein the further portion is provided at a distance from the at least one portion that substantially corresponds to the predetermined distance, and wherein steps (d) and (e) are provided to control a width of the first area.

12. The method according to claim 1, wherein the film sample is one of a pre-patterned silicon thin film sample and a continuous silicon thin film sample.

13. The method according to claim 1, wherein the electronic device is a thin film transistor.

14. The method according to claim 1, further comprising the steps of:

(i) translating the thin film sample for a predetermined distance;

(j) irradiating a further portion of the film sample using at least one beam pulse, wherein the further portion is provided at a distance from the at least one portion that substantially corresponds to the predetermined distance; and

(k) repeating steps (i) and (j) for additional portions of the film sample without stopping the translation of the film sample after the completion of the repeated step (j).

15. The method according to claim 14, wherein step (i) delivers the film sample to a first relative pre-calculated position of the further portion of the film sample to be irradiated, and wherein, after step (k), the film sample is provided at a second relative pre-calculated position whose distance is different from the predetermined distance.

16. The method according to claim 1, further comprising the steps of:

(l) translating the thin film sample for a predetermined distance;

(m) stopping the translation of the film sample, and allowing vibrations of the film sample to settle; and

(n) after step (m), irradiating a further portion of the thin film using at least one beam pulse, wherein the further portion is provided at a distance from the at least one portion that substantially corresponds to the predetermined distance.

17. The method according to claim 1, further comprising the steps of:

(o) after step (c), irradiating the at least one portion of the film sample with a further beam pulse; and

(p) after step (o), allowing the at least one portion of the film sample to re-solidify.

18. The method according to claim 17, wherein a fluence of the at least one beam pulse is different from a fluence of the further beam pulse.

19. The method according to claim 18, wherein the fluence of the further beam pulse is less than the fluence of the at least one beam pulse.

20. The method according to claim 1, further comprising the step of:

(a) after step (c), determining a location of the first area so as to avoid a placement of the active region of the electronic device thereon.

21. The method according to claim 1, wherein the at least one beam pulse includes a plurality of beamlets, and wherein the first and second areas are irradiated by the beamlets.

22. The method according to claim 1, wherein the film sample is one of a silicon thin film sample and a metal thin film sample.

23. The method according to claim 1, wherein the thin film sample is composed of at least one of silicon, germanium, and a compound of silicon germanium.

24. The method according to claim 1, wherein the thin film has a thickness approximately between 100Å and 10,000Å.

25. The method according to claim 1, further comprising the step of:

(r) before step (b), masking portions of the at least one beam pulse to produce at least one masked beam pulse, wherein the at least one masked beam pulse is used to irradiate the at least one portion of the film sample in step (b).

26. The method according to claim 1, wherein the large grains provided in the first area are laterally-grown grains.

27. The method according to claim 26, wherein the laterally-grown grains of the first area are equiaxed grains.

28. A method for processing a thin film sample, comprising the steps of:

(a) controlling a beam generator to emit at least one beam pulse;

(b) with the at least one beam pulse, irradiating at least one portion of the film sample with an intensity that is sufficient to fully melt at least one section of the film sample throughout its thickness, the at least one beam pulse having a predetermined shape;

(c) allowing the at least one portion of the film sample to re-solidify, the re-solidified at least one portion being composed of a first area and a second area, wherein the first area surrounds the second area, and wherein, upon the re-solidification thereof, the first area has large grains, and the second area has a small-grained region formed through nucleation;

(d) translating the thin film sample for a predetermined distance; and

(e) irradiating a further portion of the thin film using a further beam pulse, wherein the further portion is provided at a distance from the at least one portion that substantially corresponds to the predetermined distance, wherein steps (b) though (e) are provided to control a width of the first area, and wherein the second area has a

cross-section to allow an active region of an electronic device to be facilitated thereon.

29. The method according to claim 28, wherein the second area corresponds to at least one pixel.

30. The method according to claim 28,

wherein the first area has a first border and a second border which is provided opposite and parallel to the first border of the first area,

wherein the second area has a third border and a fourth border which is provided opposite and parallel to the third border of the second area, and

wherein a distance between the first border and the second border is smaller than a distance between the third border and the fourth border.

31. The method according to claim 28, wherein the second area has a cross-section for facilitating thereon all portions of the electronic device.

32. The method according to claim 28, wherein a size and a position of the first area with respect to the second area are provided such that the first area provides either no effect or a negligible effect on a performance of the electronic device.

33. The method according to claim 28, further comprising the steps of:

(f) after step (e), allowing the further portion of the film sample to re-solidify, the re-solidified at least one portion being composed of a third area and a fourth area,

wherein the third area surrounds the fourth area, and wherein at least one section of the third area at least partially overlaps at least one section of the first area, and

wherein, upon the re-solidification thereof, the third area has laterally grown grains, and the fourth area has a nucleated region.

34. The method according to claim 33, wherein the fourth area is composed of edges which are provided away from edges of the second area.

35. The method according to claim 33, wherein the fourth area is composed of edges which approximately border edges of the second area, and wherein the edges of the fourth area do not extend into any section of the first area.

36. The method according to claim 28, wherein the at least one beam pulse has a fluence which is substantially the same as a fluence of the further beam pulse.

37. The method according to claim 28, wherein the at least one beam pulse has a fluence which is different from a fluence of the further beam pulse.

38. The method according to claim 28, wherein the film sample is one of a pre-patterned silicon thin film sample and a continuous silicon thin film sample.

39. The method according to claim 28, wherein the electronic device is a thin film transistor.

40. The method according to claim 28, further comprising the steps of:

(g) repeating steps (d) and (e) on additional portions of the film sample without stopping the translation of the film sample.

41. The method according to claim 40, wherein step (d) delivers the film sample to a first relative pre-calculated position of the further portion of the film sample to be irradiated, and wherein, after step (e), the film sample is provided at a second relative pre-calculated position whose distance is different from the predetermined distance.

42. The method according to claim 28, further comprising the steps of:

(h) after step (d), stopping the translation of the film sample, and allowing vibrations of the film sample to settle; and

(i) after step (h), irradiating a further portion of the thin film using at least one beam pulse, wherein the further portion is provided at a distance from the at least one portion that substantially corresponds to the predetermined distance.

43. The method according to claim 42, wherein a fluence of the at least one beam pulse is different from a fluence of the further beam pulse.

44. The method according to claim 43, wherein the fluence of the further beam pulse is less than the fluence of the at least one beam pulse.

45. The method according to claim 28, wherein the at least one beam pulse includes a plurality of beamlets, and wherein the first and second areas are irradiated by the beamlets.

46. The method according to claim 28, wherein the film sample is one of a silicon thin film sample and a metal thin film sample.

47. The method according to claim 28, wherein the thin film sample is composed of at least one of silicon, germanium, and a compound of silicon germanium.

48. The method according to claim 28, wherein the thin film has a thickness approximately between 100Å and 10,000Å.

49. The method according to claim 28, further comprising the step of:

(j) before step (b), masking portions of the at least one beam pulse to produce at least one masked beam pulse, wherein the at least one masked beam pulse is used to irradiate the at least one portion of the film sample in step (b).

50. The method according to claim 28, wherein the large grains provided in the first area are laterally-grown grains.

51. The method according to claim 50, wherein the laterally-grown grains of the first area are equaled grains.

52. A system for processing a thin film sample, comprising:

a processing arrangement which is configured to:

(a) control a beam generator to emit at least one beam pulse which is sufficient to fully melt at least one section of the film sample throughout its thickness,

(b) control a translation stage such that at least one portion of the film sample is irradiated with the at least one beam pulse, the at least one beam pulse having a predetermined cross section,

wherein the at least one portion of the film sample is allowed to re-solidify, the re-solidified at least one portion being composed of a first area and a second area,

wherein, upon the re-solidification thereof, the first area has large grains, and the second area has a small-grained region formed through nucleation,

wherein the first area surrounds the second area and has a grain structure which is different from a grain structure of the second area, and

wherein the second area is configured to facilitate thereon an active region of an electronic device.

53. The system according to claim 52, wherein the second area corresponds to at least one pixel.

54. The system according to claim 52,

wherein the first area has a first border and a second border which is provided opposite and parallel to the first border of the first area,

wherein the second area has a third border and a fourth border which is provided opposite and parallel to the third border of the second area, and

wherein a distance between the first border and the second border is smaller than a distance between the third border and the fourth border.

55. The system according to claim 52, wherein the second area has a cross-section for facilitating thereon all portions of the electronic device.

56. The system according to claim 52, wherein a size and a position of the first area with respect to the second area are provided such that the first area provides either no effect or a negligible effect on a performance of the electronic device.

57. The system according to claim 52, wherein the processing arrangement is further configured to:

(c) control the translation stage to translate the thin film sample for a predetermined distance, and

(d) control the laser beam generator to irradiating a further portion of the film sample with a further beam pulse, the further portion being provided at a distance from the at least one portion that substantially corresponds to the predetermined distance,

wherein the further portion of the film sample is allowed to re-solidify, the re-solidified at least one portion being composed of a third area and a fourth area,

wherein the third area surrounds the fourth area, and wherein at least one section of the third area at least partially overlaps at least one section of the first area, and

wherein, upon the re-solidification thereof, the third area has laterally grown grains, and the fourth area has a nucleated region.

58. The system according to claim 57, wherein the fourth area is composed of edges which are provided away from edges of the second area.

59. The system according to claim 57, wherein the fourth area is composed of edges which approximately border edges of the second area, and wherein the edges of the fourth area do not extend into any section of the first area.

60. The system according to claim 52, wherein the at least one beam pulse has a fluence which is substantially the same as a fluence of the further beam pulse.

61. The system according to claim 52, wherein the at least one beam pulse has a fluence which is different from a fluence of the further beam pulse.

62. The system according to claim 52, wherein the processing arrangement is further configured to:

(e) control the translation stage to translate the thin film sample for a predetermined distance, and

(f) control the laser beam generator to irradiate a further portion of the film sample using at least one beam pulse, wherein the further portion is provided at a distance from the at least one portion that substantially corresponds to the predetermined distance, and wherein the processing arrangement irradiates the at least one portion and allows the at least one portion to re-solidify to control a width of the first area.

63. The system according to claim 52, wherein the film sample is one of a pre-patterned silicon thin film sample and a continuous silicon thin film sample.

64. The system according to claim 52, wherein the electronic device is a thin film transistor.

65. The system according to claim 52, wherein the processing arrangement is further configured to:

(g) control the translation stage to translate the thin film sample for a predetermined distance,

(h) control the laser beam generator to irradiate a further portion of the film sample using at least one beam pulse, wherein the further portion is provided at a distance from the at least one portion that substantially corresponds to the predetermined distance; and

(i) repeat procedures (g) and (h) for additional portions of the film sample without stopping the translation of the film sample after the completion of the repeated procedure (i).

66. The system according to claim 65, wherein the processing arrangement performs procedure (g) to deliver the film sample to a first relative pre-calculated position of the further portion of the film sample to be irradiated, and wherein, after the processing arrangement performs procedure (i), the film sample is provided at a second relative pre-calculated position whose distance is different from the predetermined distance.

67. The system according to claim 52, wherein the processing arrangement is further configured to:

(j) control the translation stage to translate the thin film sample for a predetermined distance, stop the translation of the film sample, and allow vibrations of the film sample to settle, and

(k) after procedure (j), control the laser beam generator to irradiate a further portion of the thin film using at least one beam pulse, wherein the further portion is provided at a distance from the at least one portion that substantially corresponds to the predetermined distance.

68. The system according to claim 52, wherein the processing arrangement is further configured to:

(l) after procedure (b), control the laser beam generator to irradiate the at least one portion of the film sample with a further beam pulse, and

(m) after procedure (l), allow the at least one portion of the film sample to re-solidify.

69. The system according to claim 58, wherein a fluence of the at least one beam pulse is different from a fluence of the further beam pulse.

70. The system according to claim 69, wherein the fluence of the further beam pulse is less than the fluence of the at least one beam pulse.

71. The system according to claim 52, wherein the at least one beam pulse includes a plurality of beamlets, and wherein the first and second areas are irradiated by the beamlets.

72. The system according to claim 52, wherein the film sample is one of a silicon thin film sample and a metal thin film sample.

73. The system according to claim 52, wherein the thin film sample is composed of at least one of silicon, germanium, and a compound of silicon germanium.

74. The system according to claim 52, wherein the thin film has a thickness approximately between 100Å and 10,000Å.

75. The system according to claim 52, wherein the processing arrangement is further configured to:

(l) during procedure (b), mask portions of the at least one beam pulse to produce at least one masked beam pulse, wherein the at least one masked beam pulse is used to irradiate the at least one portion of the film sample in procedure (b).

76. The system according to claim 52, wherein the large grains provided in the first area are laterally-grown grains.

77. The system according to claim 76, wherein the laterally-grown grains of the first area are equiaxed grains.

78. A system for processing a thin film sample, comprising:

a processing arrangement which is configured to:

(a) control a beam generator to emit at least one beam pulse which has an intensity which is sufficient to fully melt at least one section of the film sample throughout its entire thickness,

(b) control a translation stage such that at least one portion of the film sample is irradiated with the at least one beam pulse, the at least one beam pulse having a predetermined cross section, wherein the at least one portion of the film sample is allowed to re-solidify, the re-solidified at least one position being composed of a first area and a second area, and wherein, upon the re-solidification thereof, the first area has large grains, and the second area has a small-grained region formed through nucleation,

(c) control the translation stage to translate the thin film sample for a predetermined distance, and

(d) control the laser beam generator to irradiate a further portion of the thin film using a further beam pulse, the further portion being provided at a distance from the at least one portion that substantially corresponds to the predetermined distance,

wherein procedures (b) through (d) are provided to control a width of the first area, and

wherein a width of the second area is configured to facilitate thereon an active region of an electronic device.

79. The system according to claim 78, wherein the second area corresponds to at least one pixel.

80. The system according to claim 78,

wherein the first area has a first border and a second border which is provided opposite and parallel to the first border of the first area,

wherein the second area has a third border and a fourth border which is provided opposite and parallel to the third border of the second area, and

wherein a distance between the first border and the second border is smaller than a distance between the third border and the fourth border.

81. The system according to claim 80, wherein, upon the re-solidification of the film sample, a nucleated region is formed in the second area.

82. The system according to claim 78, wherein the second area has a cross-section for facilitating thereon all portions of the electronic device.

83. The system according to claim 78, wherein a size and a position of the first area with respect to the second area are provided such that the first area provides either no effect or a negligible effect on a performance of the electronic device.

84. The system according to claim 78,

wherein the further portion of the film sample is allowed to re-solidify, the re-solidified at least one portion being composed of a third area and a fourth area, and wherein the third area surrounds the fourth area,

wherein at least one section of the third area at least partially overlaps at least one section of the first area, and

wherein, upon the re-solidification thereof, the third area has laterally grown grains, and the fourth area has a nucleated region.

85. The system according to claim 84, wherein the fourth area is composed of edges which are provided away from edges of the second area.

86. The system according to claim 84, wherein the fourth area is composed of edges which approximately border edges of the second area, and wherein the edges of the fourth area do not extend into any section of the first area.

87. The system according to claim 78, wherein the at least one beam pulse has a fluence which is substantially the same as a fluence of the further beam pulse.

88. The system according to claim 78, wherein the at least one beam pulse has a fluence which is different from a fluence of the further beam pulse.

89. The system according to claim 78, wherein the film sample is one of a pre-patterned silicon thin film sample and a continuous silicon thin film sample.

64. The system according to claim 78, wherein the electronic device is a thin film transistor.

91. The system according to claim 78, wherein the processing arrangement is further configured to:

(e) repeat procedures (c) and (d) on additional portions of the film sample without stopping the translation of the film sample.

92. The system according to claim 89, wherein procedure (c) delivers the film sample to a first relative pre-calculated position of the further portion of the film sample to be irradiated, and wherein, after procedure (d), the film sample is provided at a second relative pre-calculated position whose distance is different from the predetermined distance.

93. The system according to claim 78, wherein the processing arrangement is further configured to:

(f) after procedure (e), control the translation stage to stop the translation of the film sample, and allow vibrations of the film sample to settle, and

(g) after procedure (f), control the laser beam generator to irradiate a further portion of the thin film using at least one beam pulse, wherein the further portion is provided at a distance from the at least one portion that substantially corresponds to the predetermined distance.

94. The system according to claim 93, wherein a fluence of the at least one beam pulse is different from a fluence of the further beam pulse.

95. The system according to claim 93, wherein the fluence of the further beam pulse is less than the fluence of the at least one beam pulse.

96. The system according to claim 78, wherein the at least one beam pulse includes a plurality of beamlets, and wherein the first and second areas are irradiated by the beamlets.

97. The system according to claim 78, wherein the film sample is one of a silicon thin film sample and a metal thin film sample.

98. The system according to claim 78, wherein the thin film sample is composed of at least one of silicon, germanium, and a compound of silicon germanium.

99. The system according to claim 78, wherein the thin film has a thickness approximately between 100Å and 10,000Å.

100. The system according to claim 78, wherein the processing arrangement is further configured to:

(l) during procedure (b), mask portions of the at least one beam pulse to produce at least one masked beam pulse, wherein the at least one masked beam pulse is used to irradiate the at least one portion of the film sample in procedure (b).

101. The system according to claim 78, wherein the large grains provided in the first area are laterally-grown grains.

102. The system according to claim 101, wherein the laterally-grown grains of the first area are equiaxed grains.

103. A thin film sample, comprising:

at least one section irradiated by at least one beam pulse which fully melts the at least one section of the sample throughout its thickness,

wherein the at least one portion of the film sample is re-solidified to include a first area and a second area,

wherein, upon the re-solidification of the at least one section, the first area includes large grains, and the second area includes a region formed through nucleation,

wherein the first area surrounds the second area and has a grain structure which is different from a grain structure of the second area, and

wherein the second area is configured to facilitate thereon an active region of an electronic device.

104. A thin film sample, comprising:

a first area having large grains; and

a second area being surrounded by the first area and including a region formed through nucleation of at least one section of the thin film in which the second area is situated,

wherein the first area has a grain structure which is different from a grain structure of the second area, and

wherein the second area is configured to facilitate thereon an active region of an electronic device.

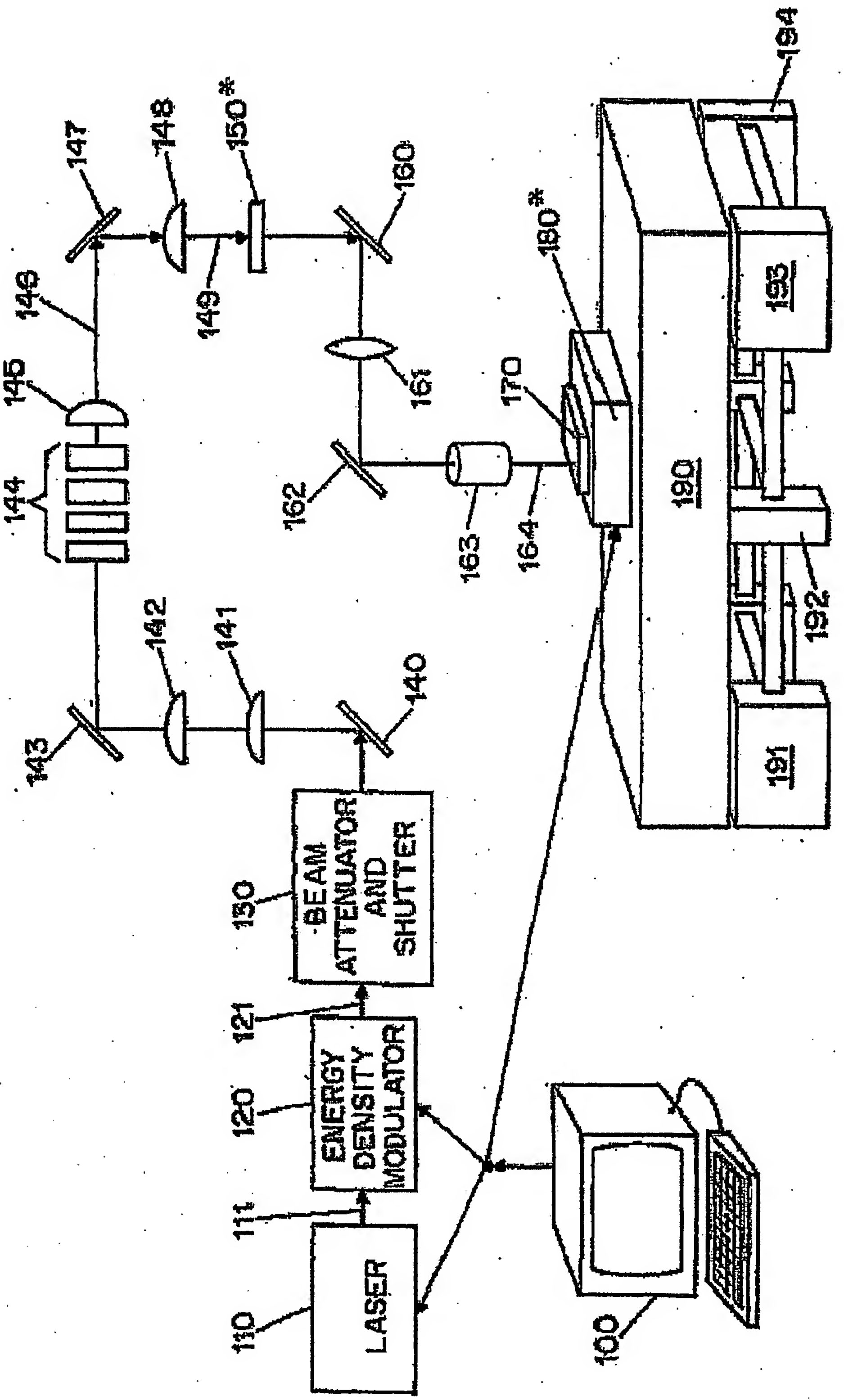

LASER
ENERGY DENSITY MODULATOR
BEAM ATTENUATOR AND SHUTTER
110
111
120
121
130
140
141
142
143
144
145
146
147
148
149
150*
160
161
162
163
164
170
180*
190
191
192
194
195
100

FIG. 1A

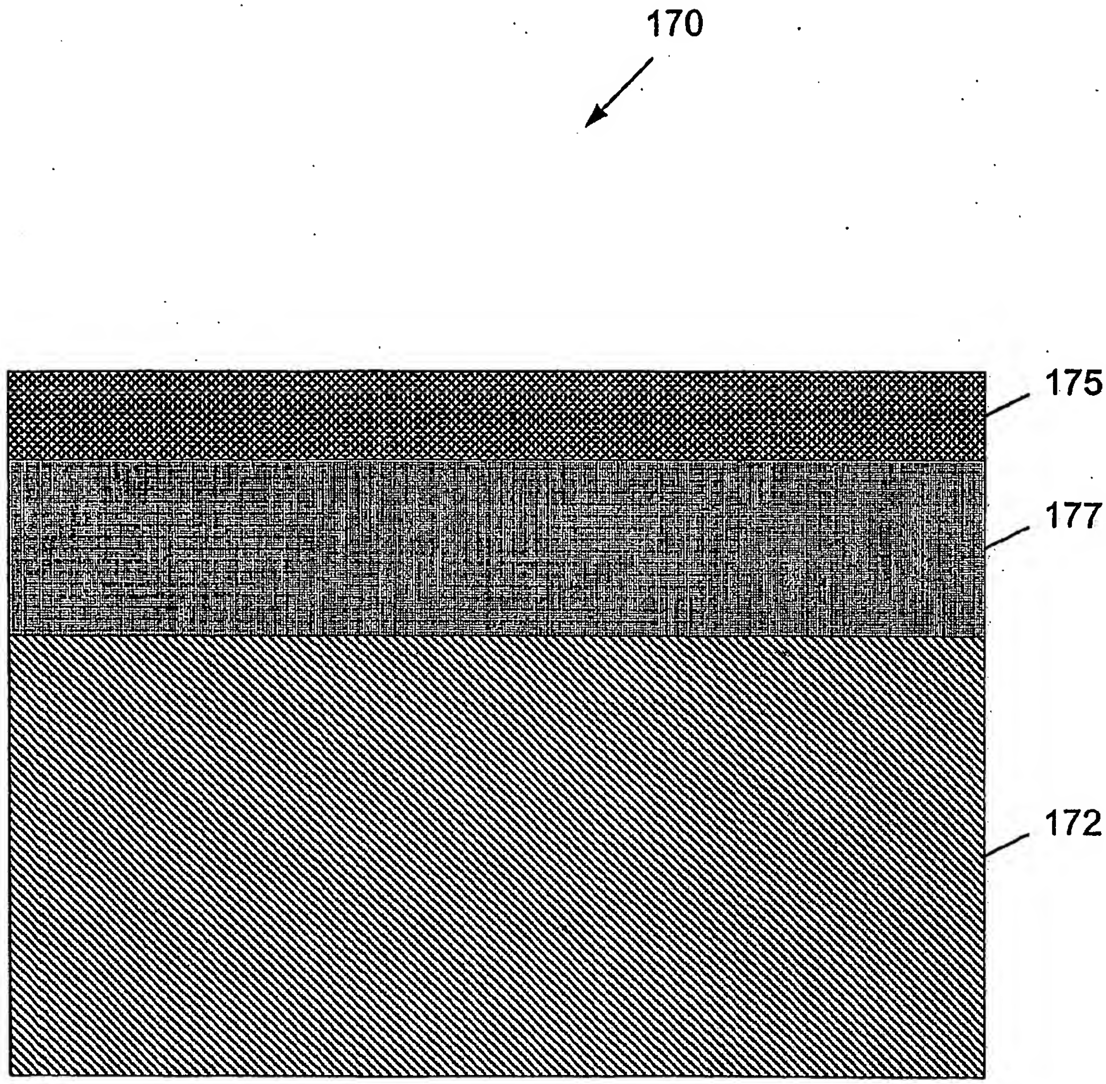
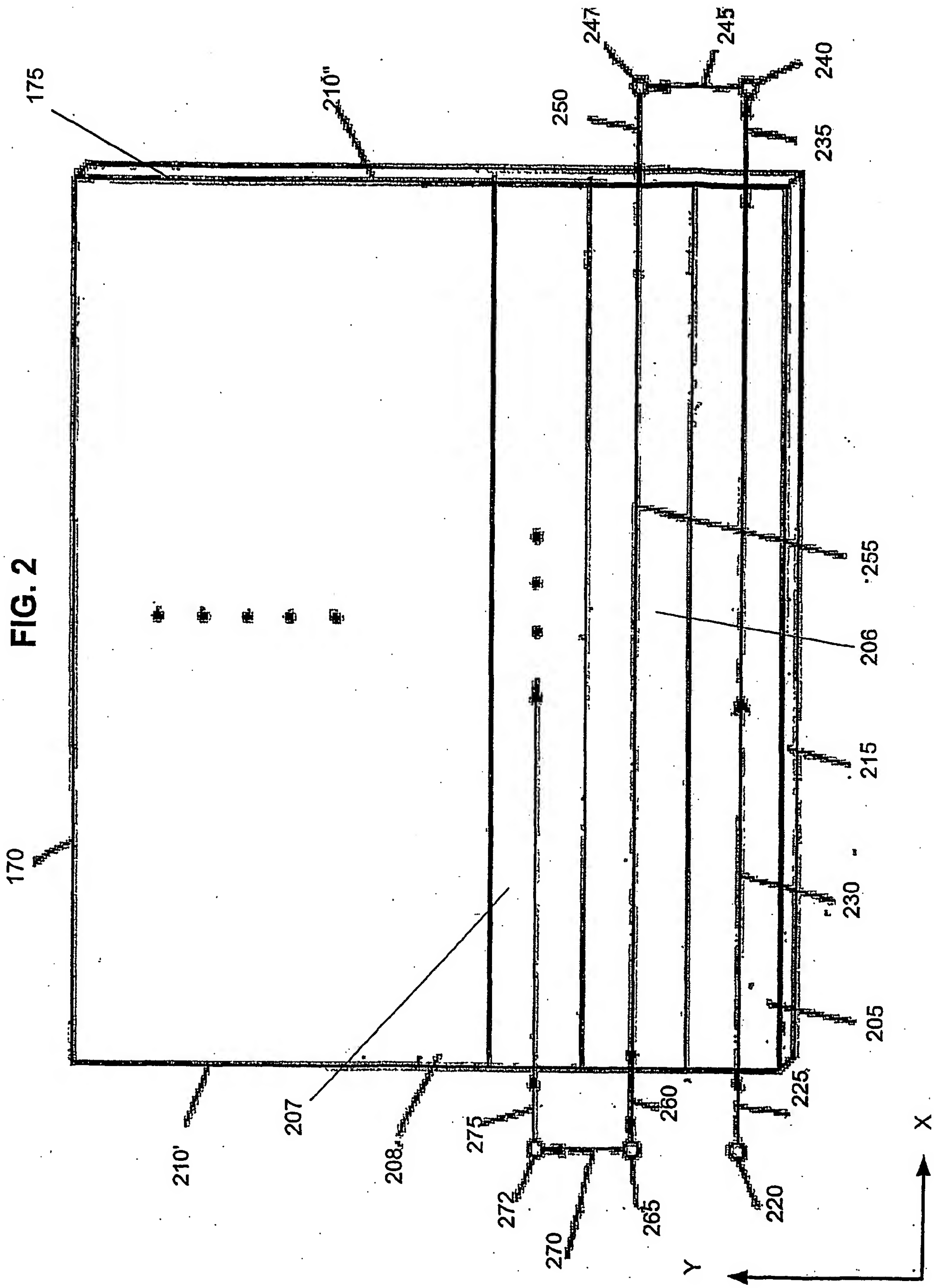


FIG. 1B

FIG. 2


175
210"
250
247
245
240
235
255
206
215
230
205
225
220
265
270
272
260
275
208
207
210'
170
X
Y

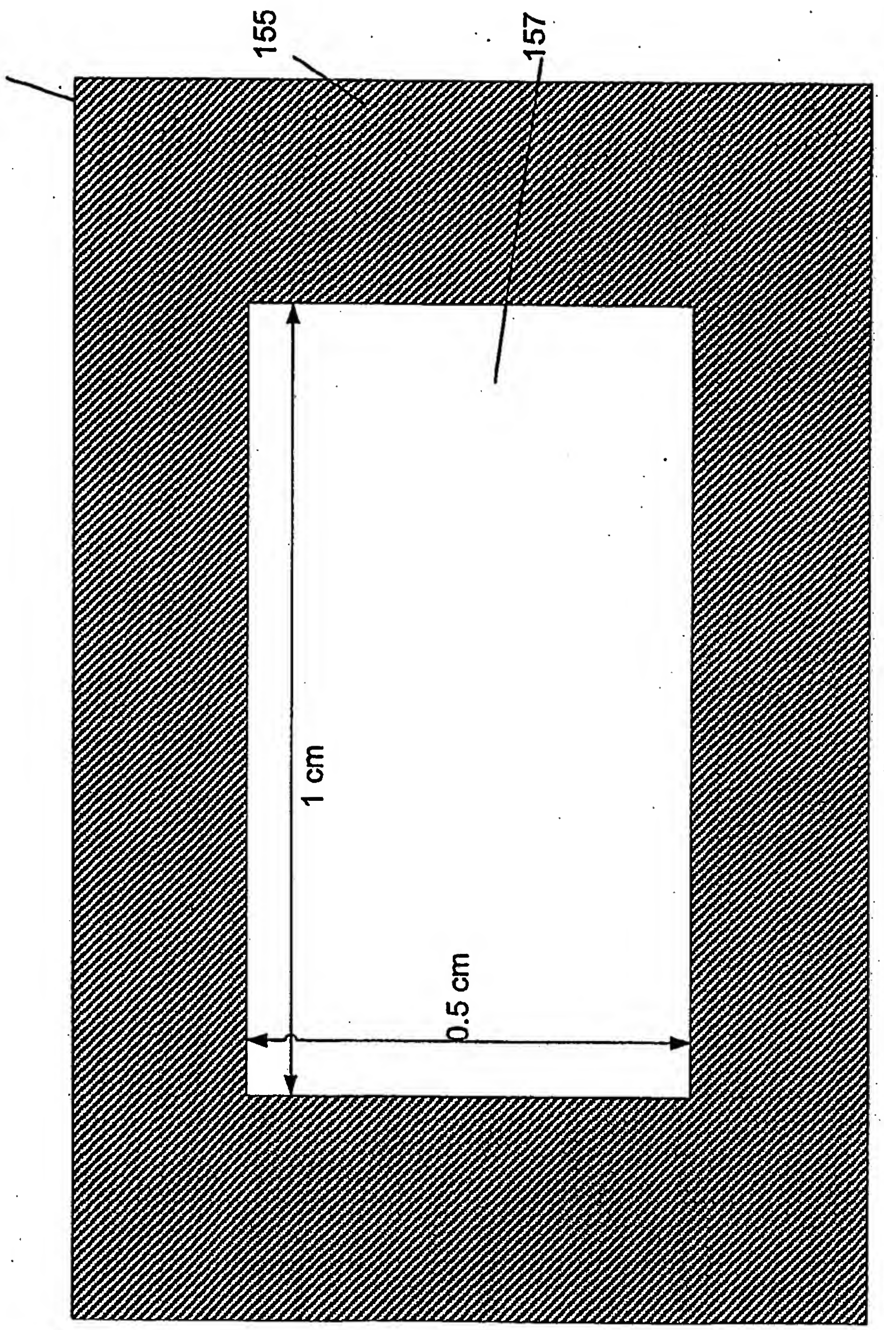


FIG. 3

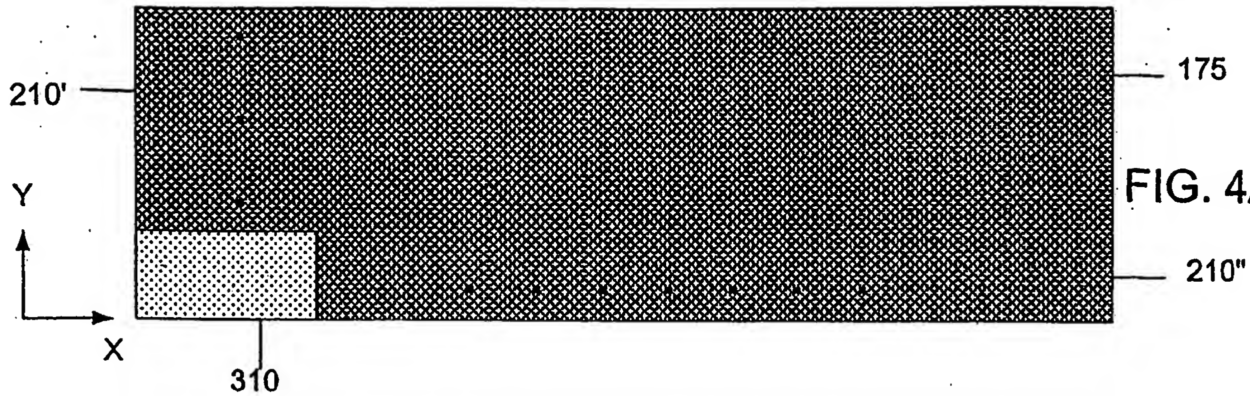


FIG. 4A

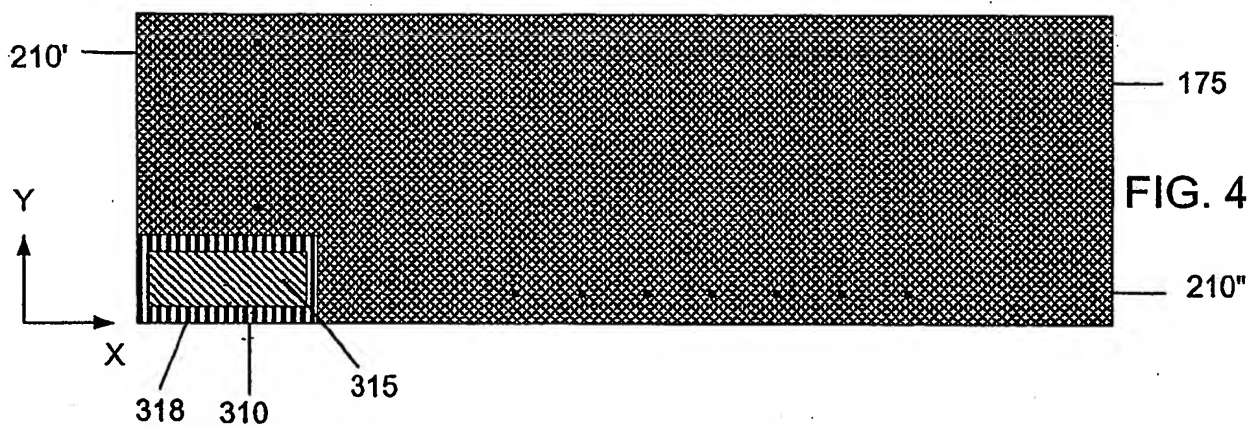


FIG. 4B

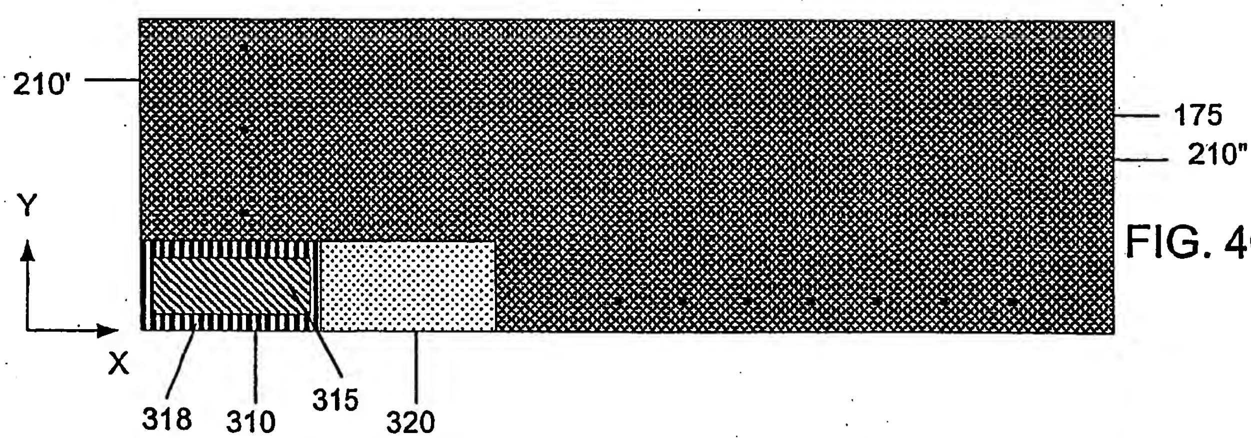


FIG. 4C

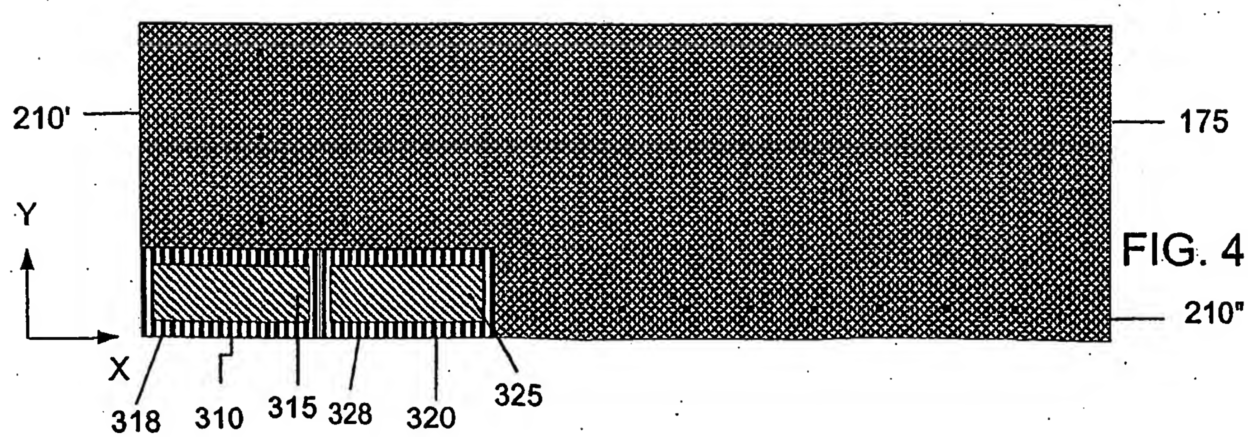


FIG. 4D

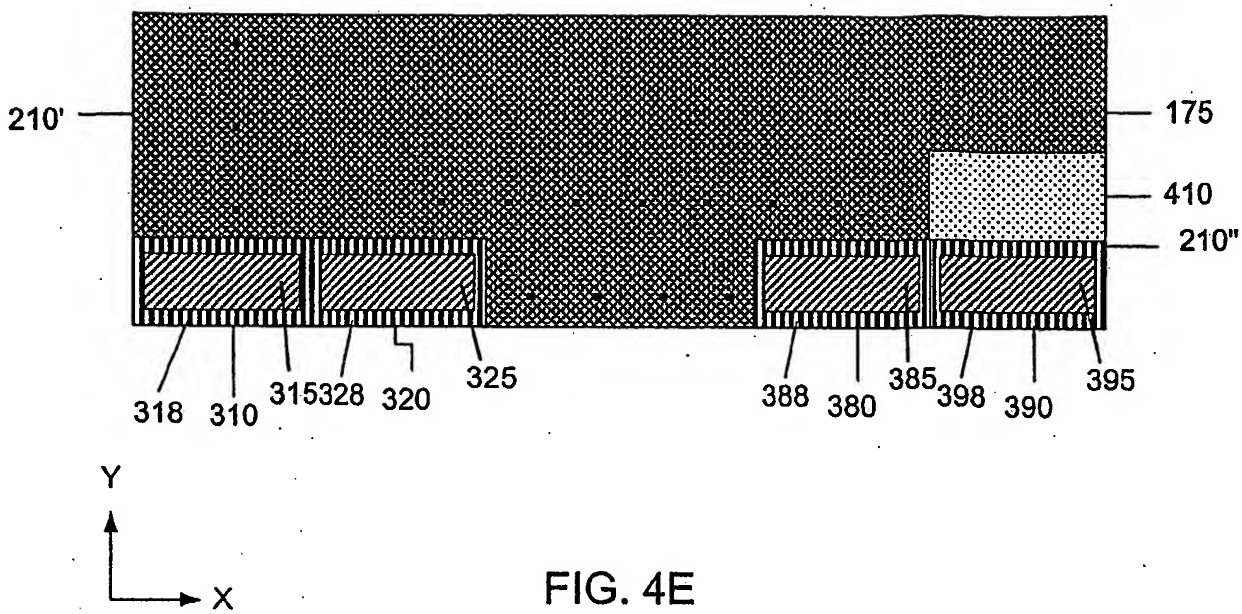

210'
175
410
210"
318
310
315
328
320
325
388
380
385
398
390
395
Y
X

FIG. 4E

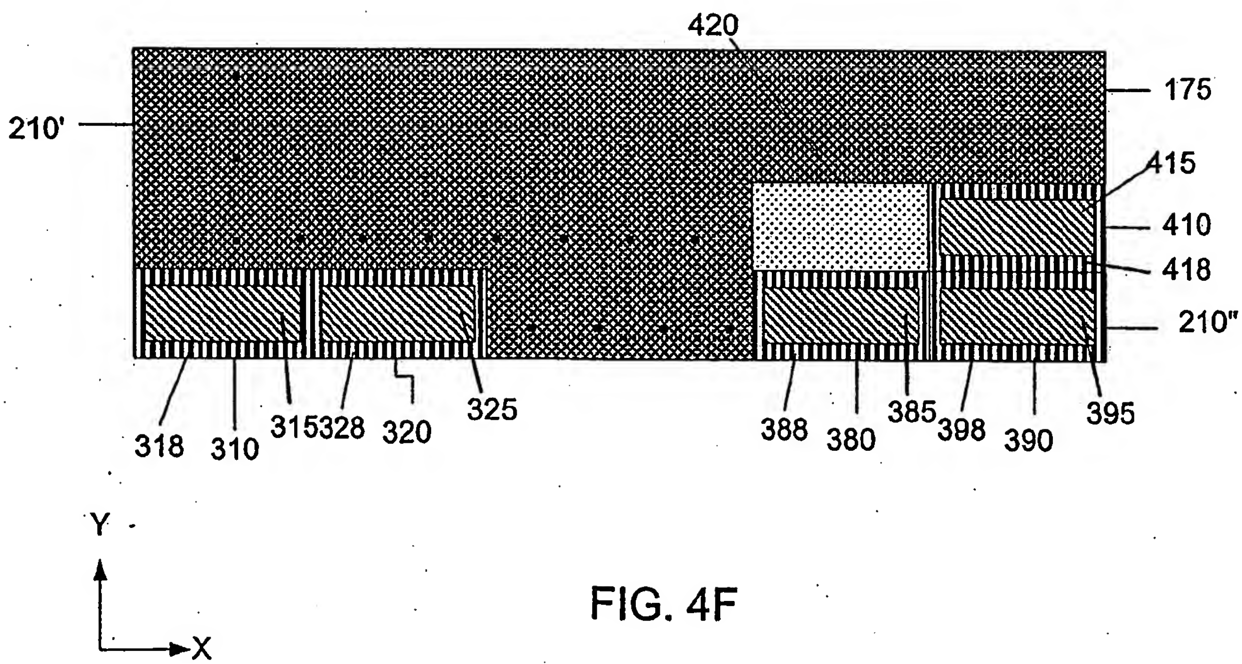
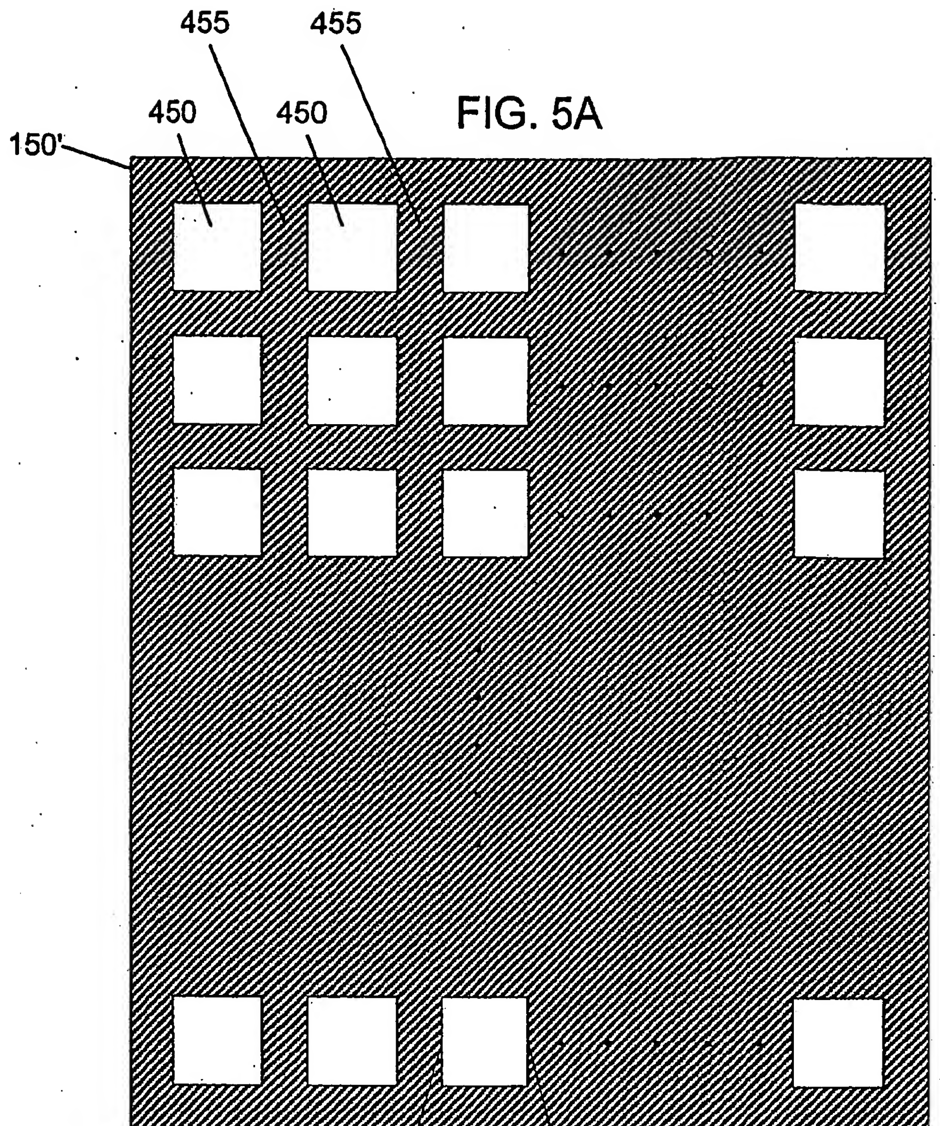

420
210'
175
415
410
418
210"
318
310
315
328
320
325
388
380
385
398
390
395
Y
X

FIG. 4F

FIG. 5A



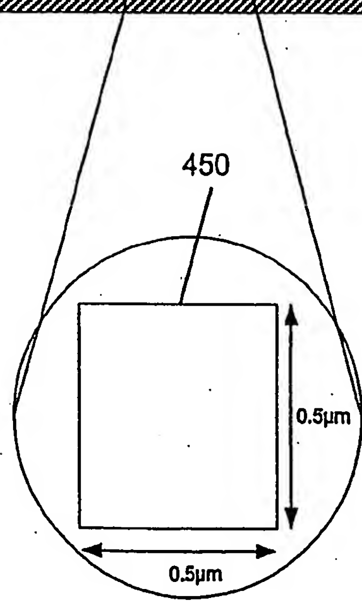


FIG. 5B

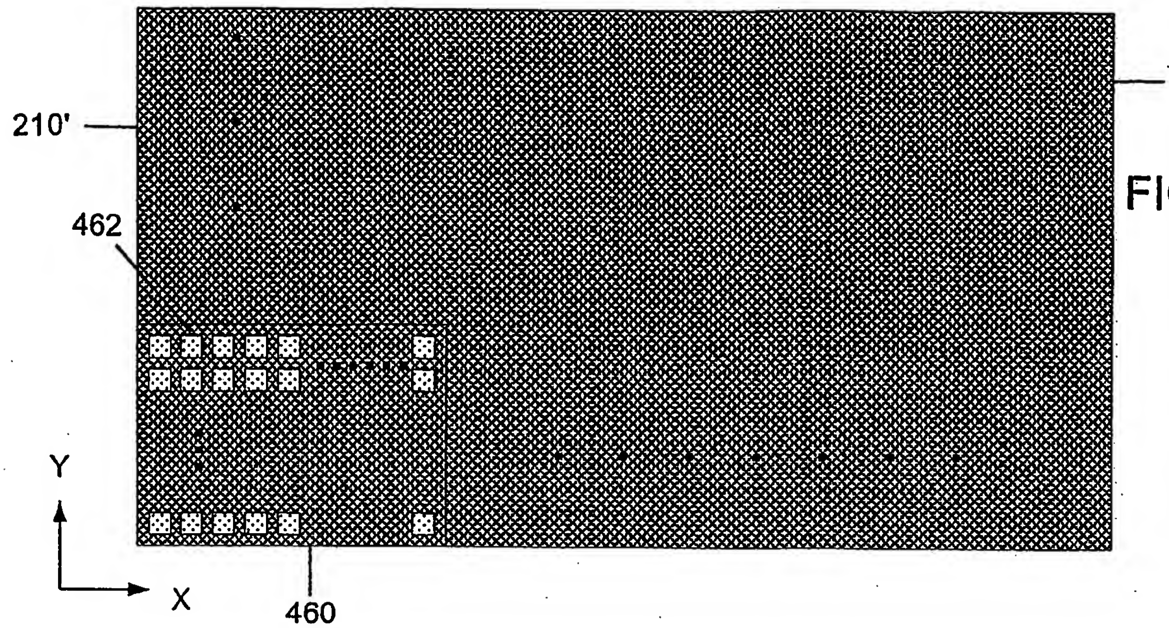


FIG. 6A

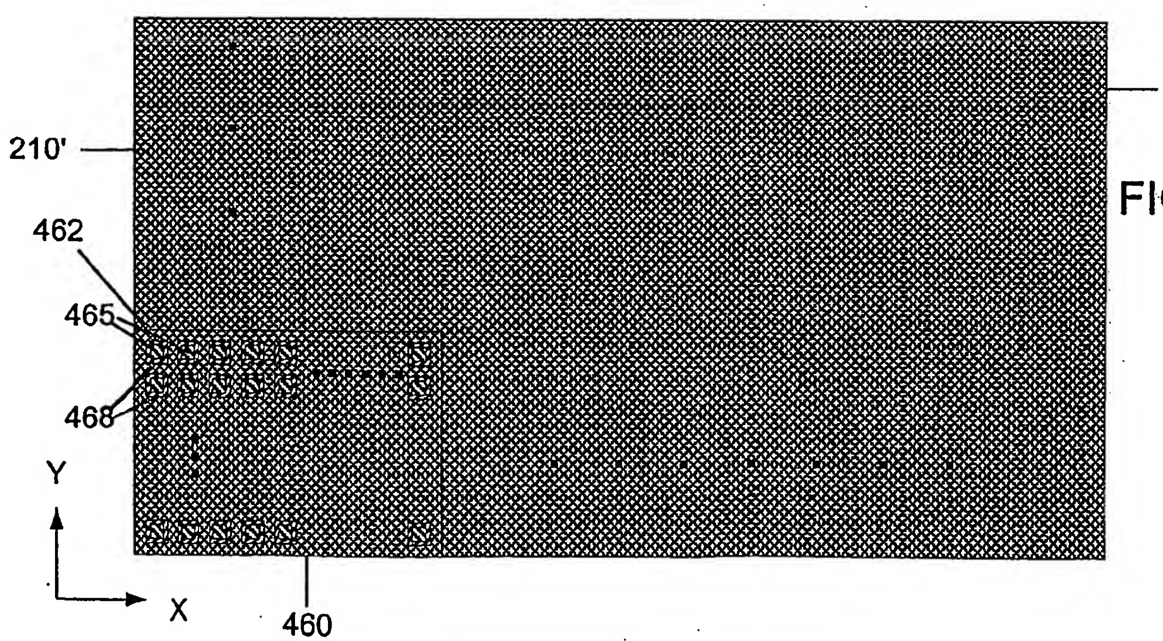


FIG. 6B

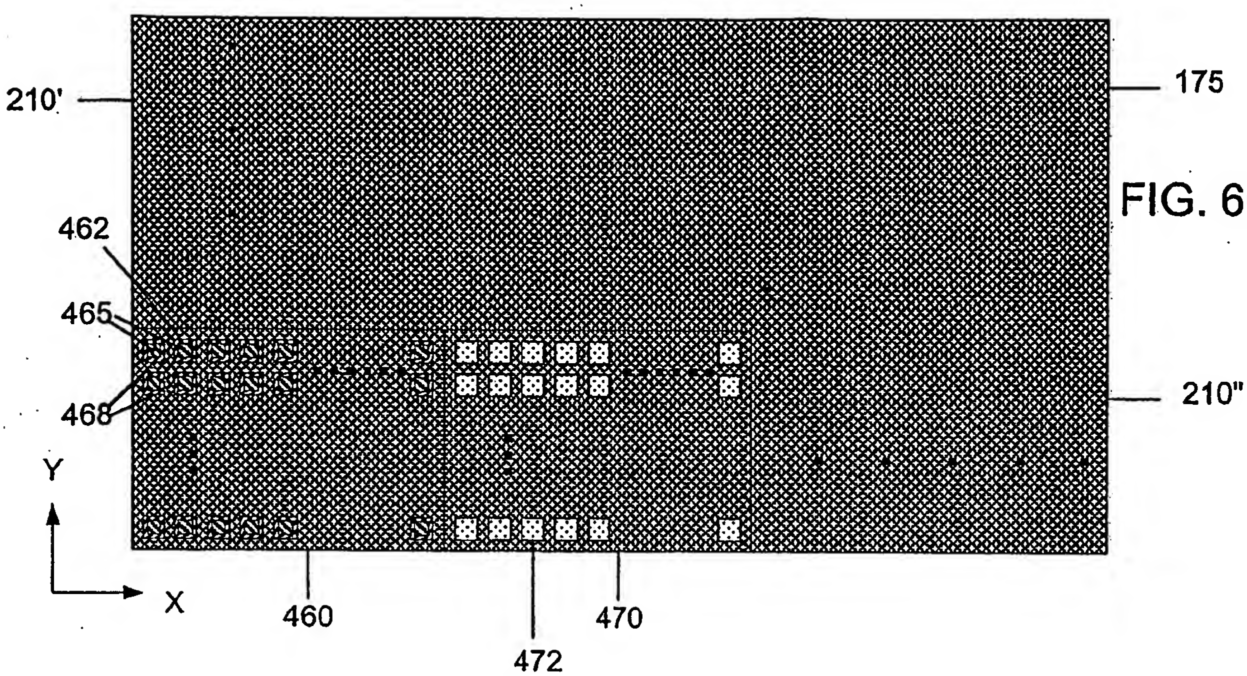

210'
175
462
465
468
210"
Y
X
460
472
470

FIG. 6C

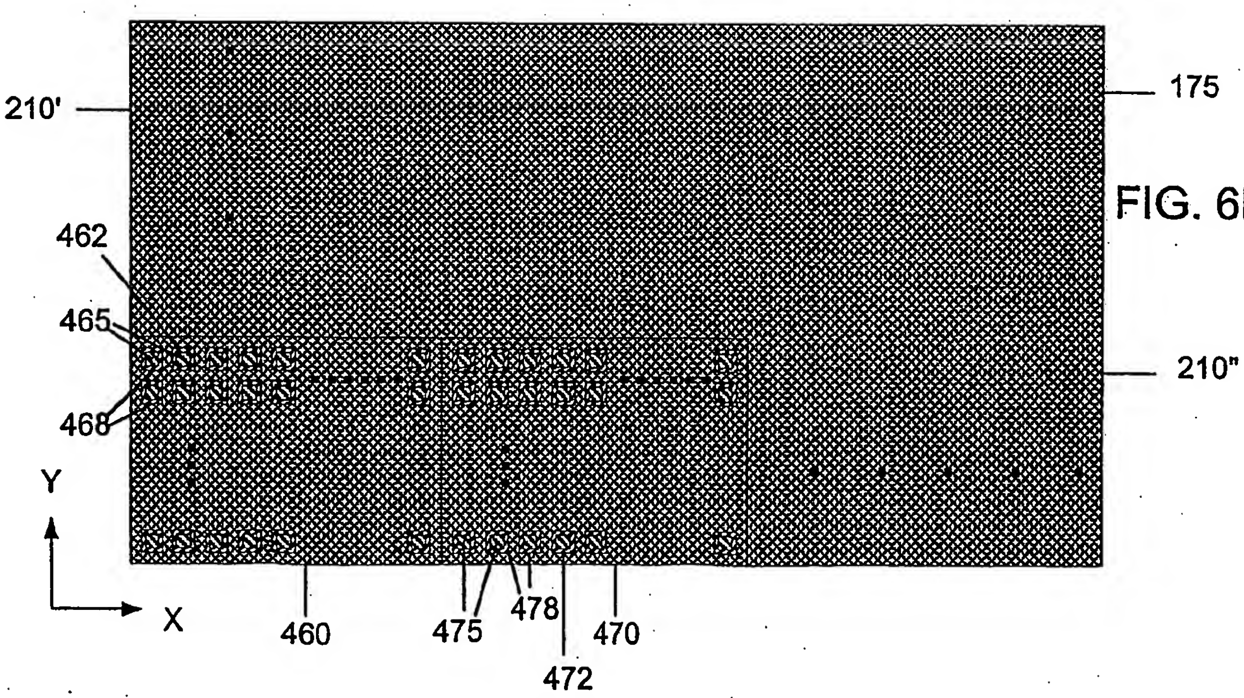

210'
175
462
465
468
210"
Y
X
460
475
478
470
472

FIG. 6D

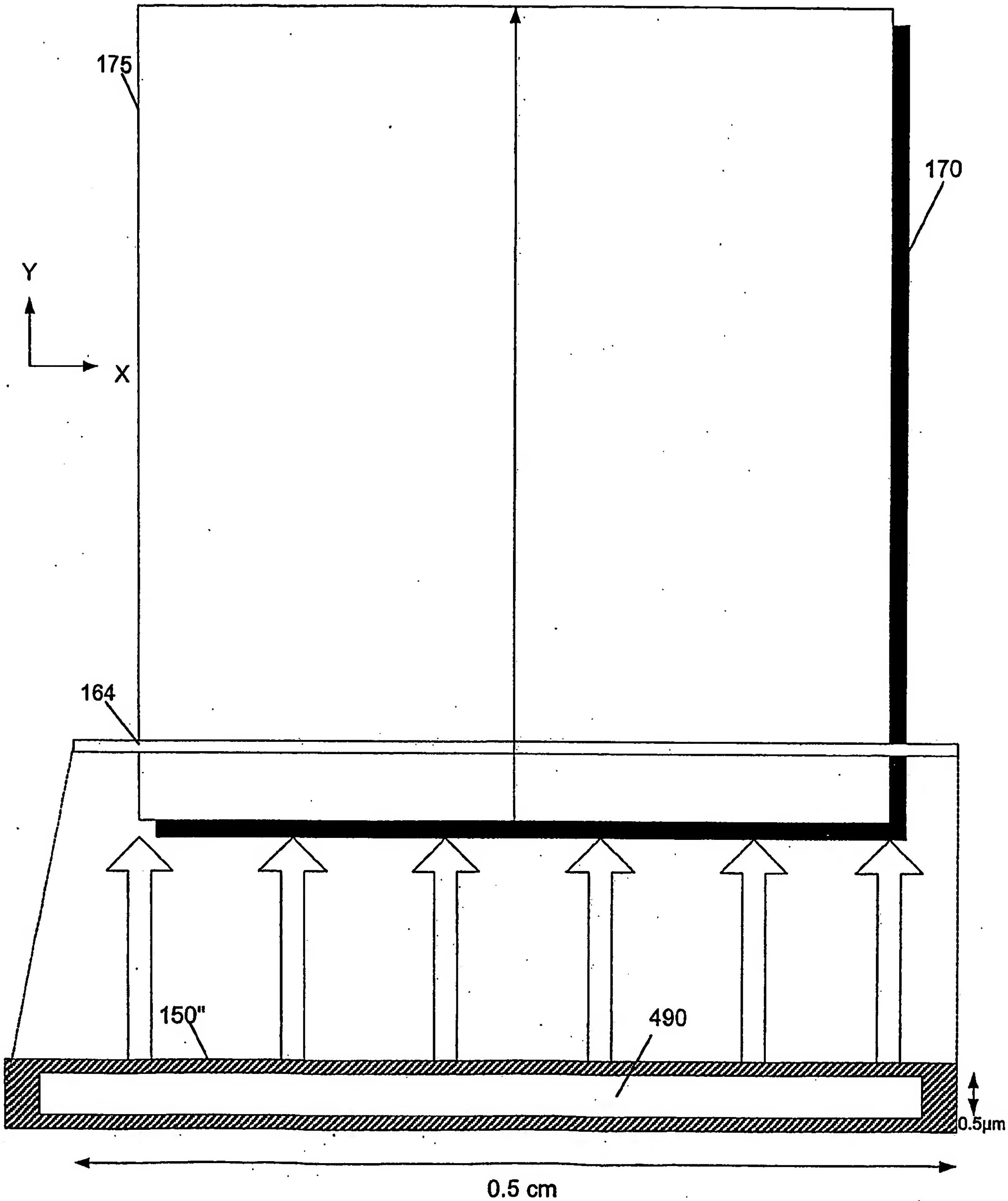


FIG. 7

FIG. 8A

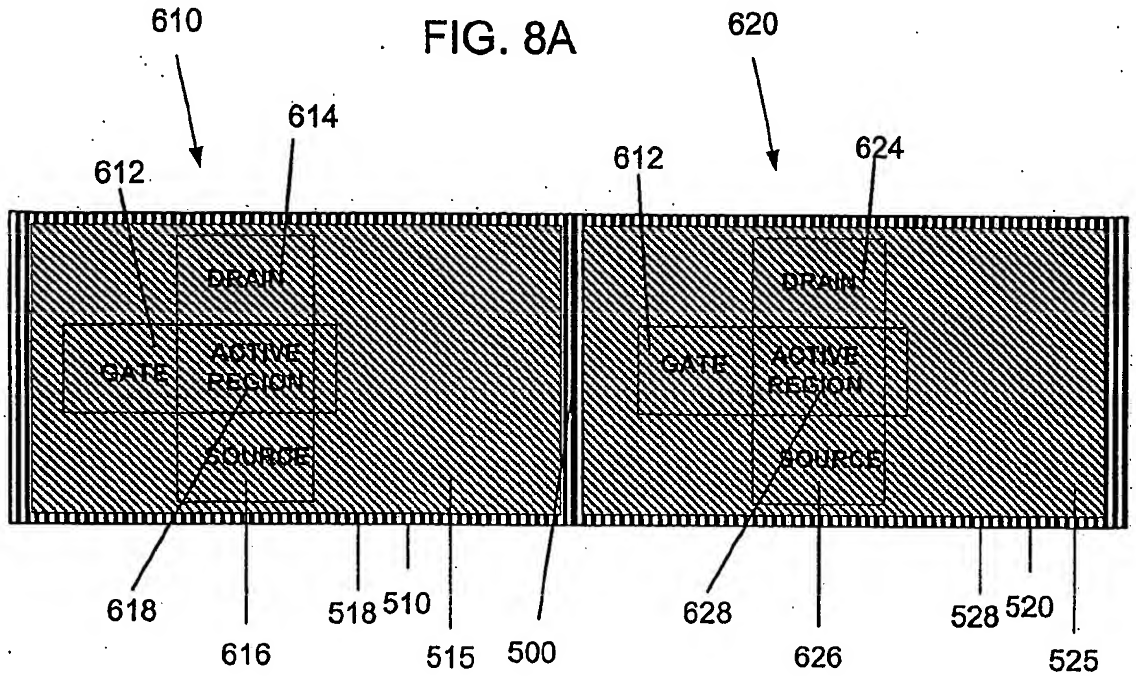

610
620
614
612
612
624
DRAIN
GATE
ACTIVE REGION
SOURCE
DRAIN
GATE
ACTIVE REGION
SOURCE
618
616
518
510
515
500
628
626
528
520
525

FIG. 8B

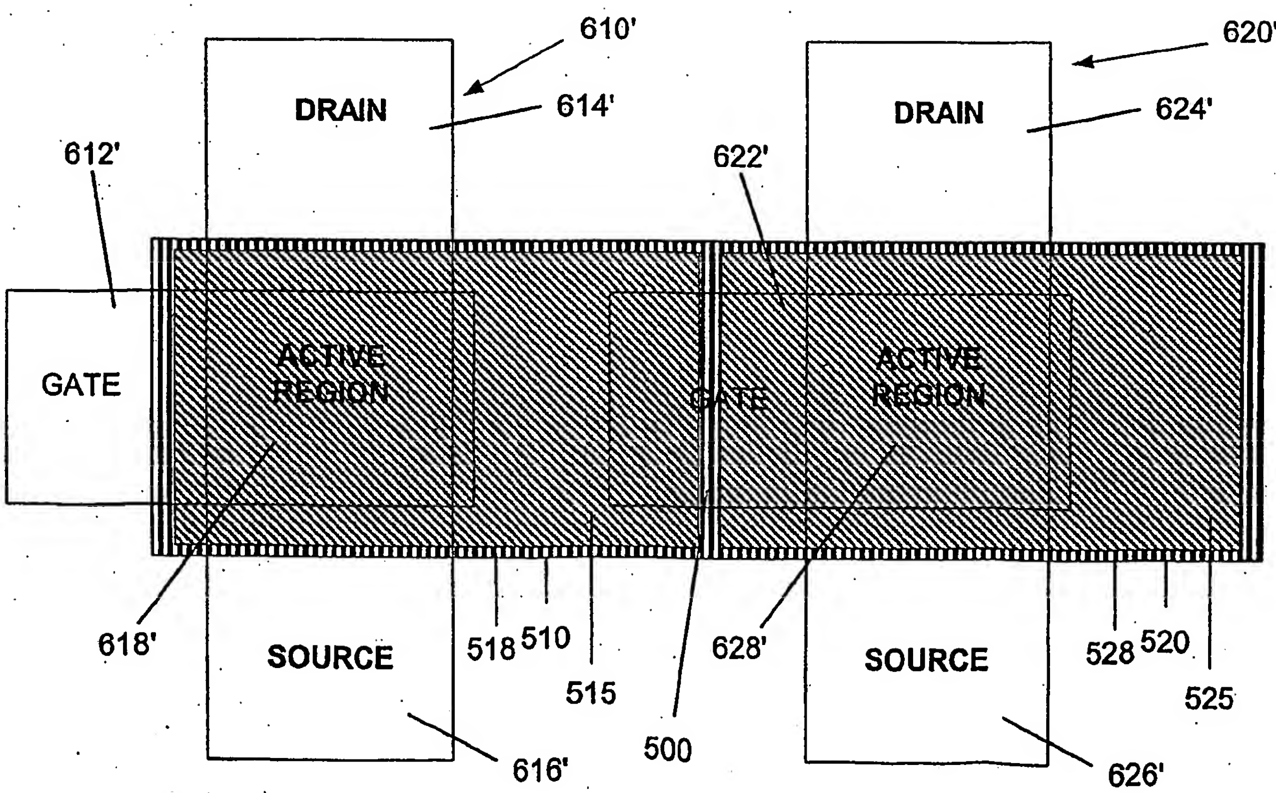

610'
614'
620'
624'
DRAIN
DRAIN
612'
622'
GATE
ACTIVE REGION
GATE
ACTIVE REGION
618'
SOURCE
518
510
515
500
628'
SOURCE
528
520
525
616'
626'

FIG. 9

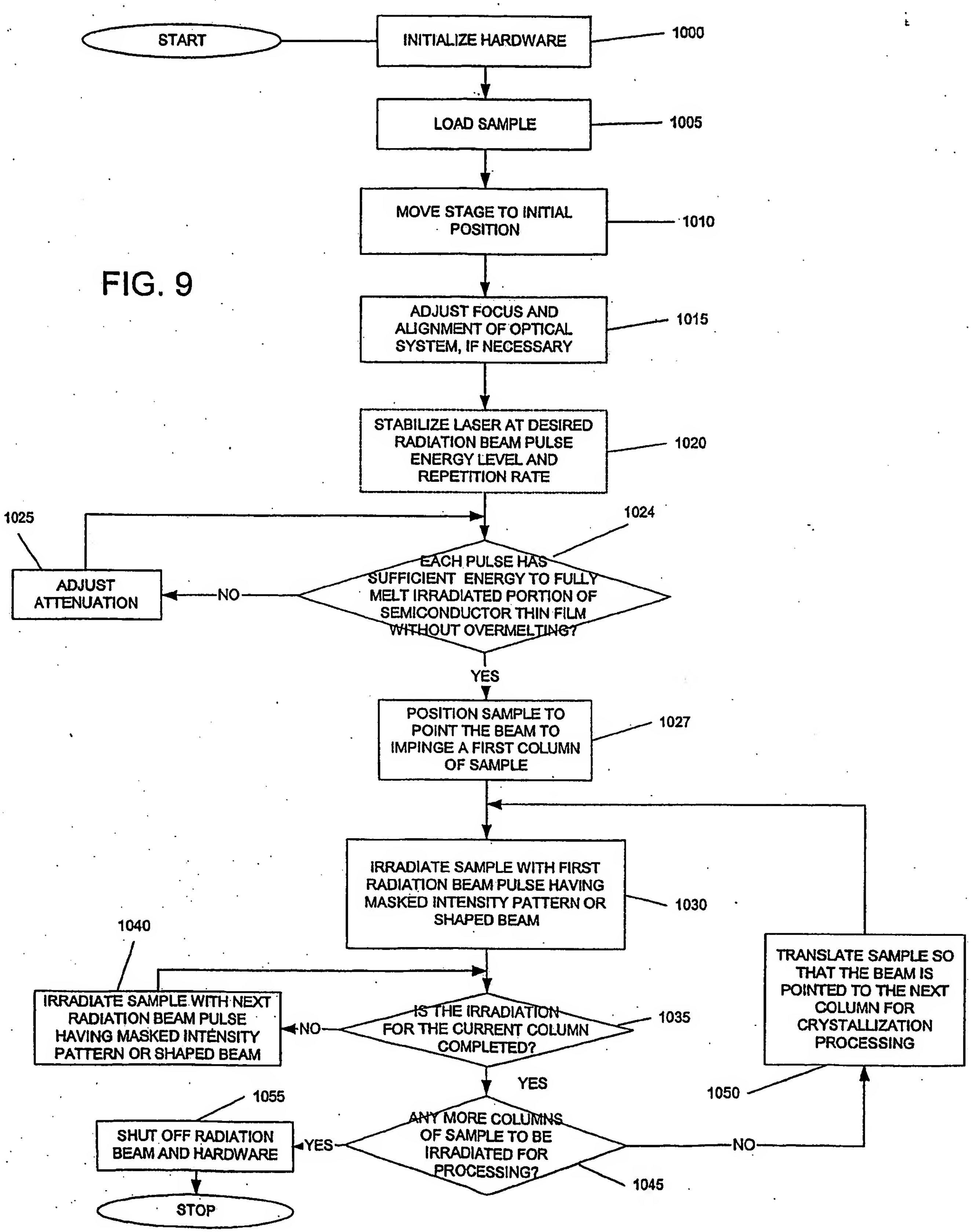
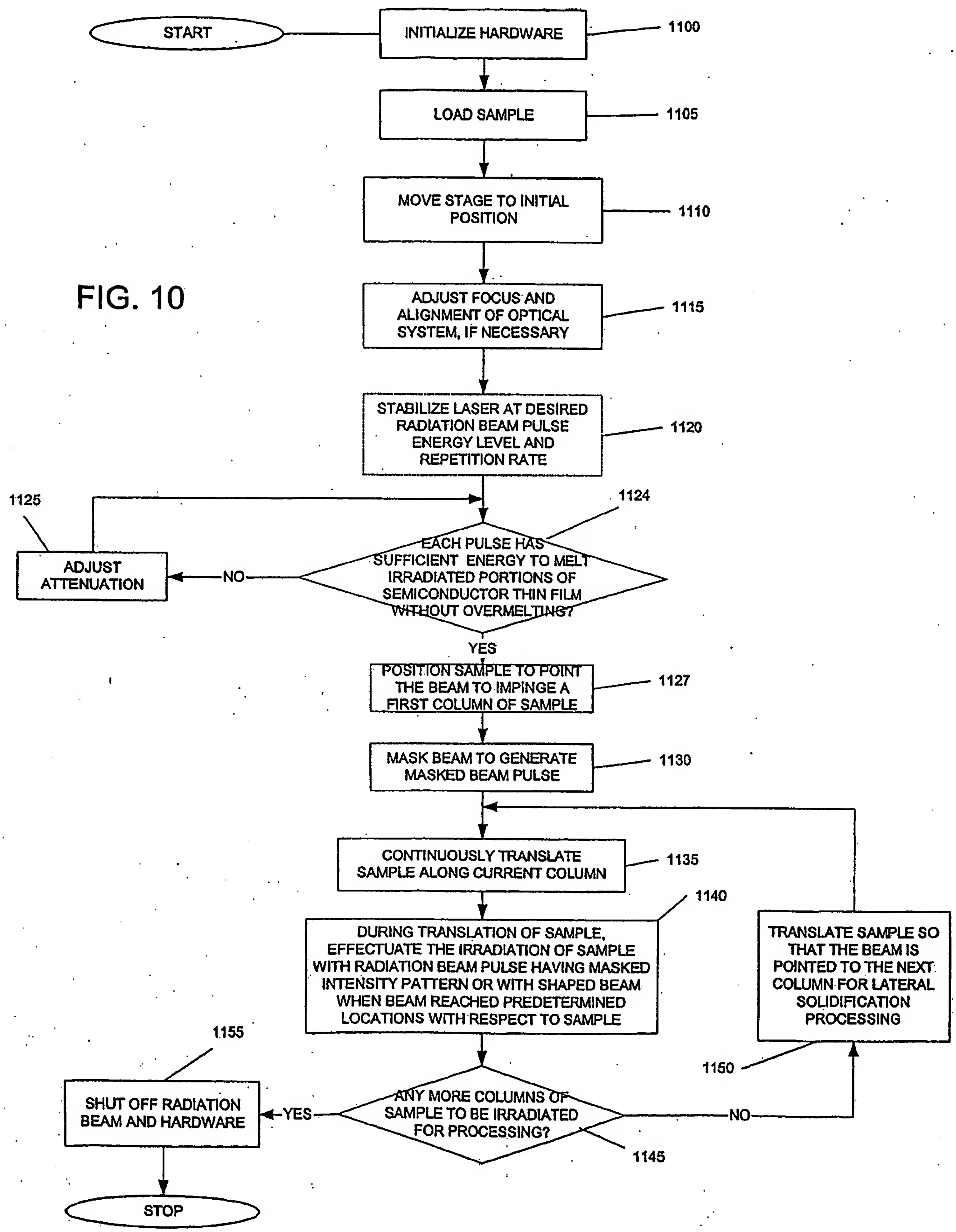

START
INITIALIZE HARDWARE
1000
LOAD SAMPLE
1005
MOVE STAGE TO INITIAL POSITION
1010
ADJUST FOCUS AND ALIGNMENT OF OPTICAL SYSTEM, IF NECESSARY
1015
STABILIZE LASER AT DESIRED RADIATION BEAM PULSE ENERGY LEVEL AND REPETITION RATE
1020
1025
ADJUST ATTENUATION
NO
EACH PULSE HAS SUFFICIENT ENERGY TO FULLY MELT IRRADIATED PORTION OF SEMICONDUCTOR THIN FILM WITHOUT OVERMELTING?
1024
YES
POSITION SAMPLE TO POINT THE BEAM TO IMPINGE A FIRST COLUMN OF SAMPLE
1027
IRRADIATE SAMPLE WITH FIRST RADIATION BEAM PULSE HAVING MASKED INTENSITY PATTERN OR SHAPED BEAM
1030
1040
IRRADIATE SAMPLE WITH NEXT RADIATION BEAM PULSE HAVING MASKED INTENSITY PATTERN OR SHAPED BEAM
NO
IS THE IRRADIATION FOR THE CURRENT COLUMN COMPLETED?
1035
TRANSLATE SAMPLE SO THAT THE BEAM IS POINTED TO THE NEXT COLUMN FOR CRYSTALLIZATION PROCESSING
YES
1050
1055
SHUT OFF RADIATION BEAM AND HARDWARE
YES
ANY MORE COLUMNS OF SAMPLE TO BE IRRADIATED FOR PROCESSING?
NO
1045
STOP

FIG. 10


START
INITIALIZE HARDWARE
1100
LOAD SAMPLE
1105
MOVE STAGE TO INITIAL POSITION
1110
ADJUST FOCUS AND ALIGNMENT OF OPTICAL SYSTEM, IF NECESSARY
1115
STABILIZE LASER AT DESIRED RADIATION BEAM PULSE ENERGY LEVEL AND REPETITION RATE
1120
1125
1124
ADJUST ATTENUATION
NO
EACH PULSE HAS SUFFICIENT ENERGY TO MELT IRRADIATED PORTIONS OF SEMICONDUCTOR THIN FILM WITHOUT OVERMELTING?
YES
POSITION SAMPLE TO POINT THE BEAM TO IMPINGE A FIRST COLUMN OF SAMPLE
1127
MASK BEAM TO GENERATE MASKED BEAM PULSE
1130
CONTINUOUSLY TRANSLATE SAMPLE ALONG CURRENT COLUMN
1135
1140
DURING TRANSLATION OF SAMPLE, EFFECTUATE THE IRRADIATION OF SAMPLE WITH RADIATION BEAM PULSE HAVING MASKED INTENSITY PATTERN OR WITH SHAPED BEAM WHEN BEAM REACHED PREDETERMINED LOCATIONS WITH RESPECT TO SAMPLE
TRANSLATE SAMPLE SO THAT THE BEAM IS POINTED TO THE NEXT COLUMN FOR LATERAL SOLIDIFICATION PROCESSING
1155
1150
SHUT OFF RADIATION BEAM AND HARDWARE
YES
ANY MORE COLUMNS OF SAMPLE TO BE IRRADIATED FOR PROCESSING?
NO
1145
STOP

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 March 2003 (06.03.2003)

PCT

(10) International Publication Number
WO 03/018882 A1

(51) International Patent Classification[7]: C30B 13/00

(21) International Application Number: PCT/US02/27246

(22) International Filing Date: 27 August 2002 (27.08.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/315,181 27 August 2001 (27.08.2001) US

(71) Applicant (*for all designated States except US*): THE TRUSTEES OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK [US/US]; 116th Street and Broadway, New York, NY 10027 (US).

(72) Inventors; and
(75) Inventors/Applicants (*for US only*): IM, James, S. [US/US]; 520 W. 114th Street, Apt. 74, New York, NY 10027 (US). VAN DER WILT, Paul, Christiaan [NL/NL]; Oostavenstraat 2A, NL-2312 Leiden MB (NL).

(74) Agents: TANG, Henry et al.; Baker Botts L.L.P., 30 Rockefeller Plaza, New York, NY 10112-4498 (US).

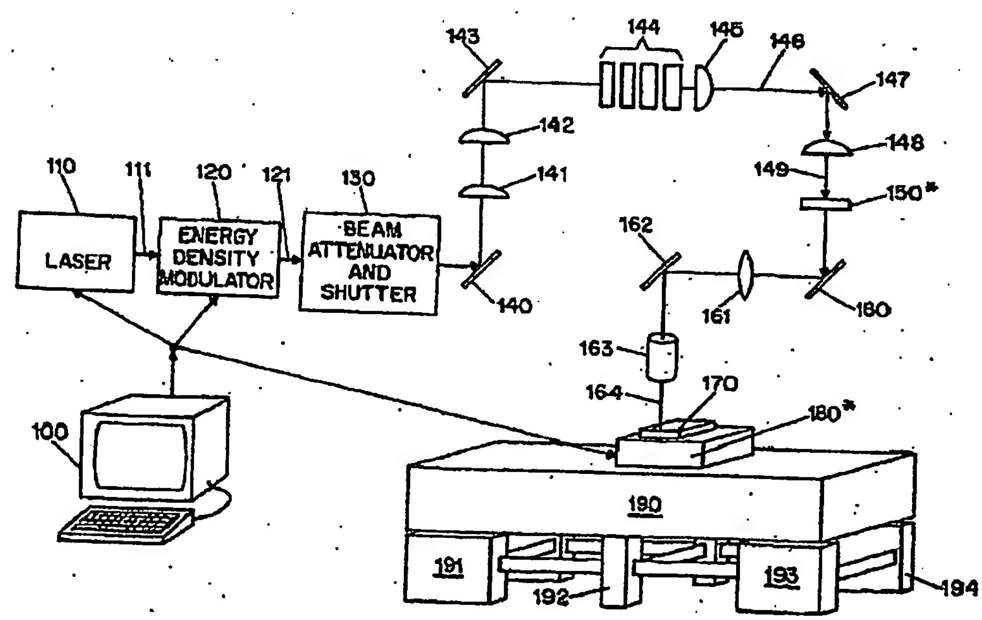
(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: IMPROVED POLYCRYSTALLINE TFT UNIFORMITY THROUGH MICROSTRUCTURE MIS-ALIGNMENT



(57) Abstract: Methods of making a polycrystalline silicon thin-film transistor having a uniform microstructure. One exemplary method requires receiving a polycrystalline silicon thin film having a grain structure which is periodic in at least a first direction, and placing at least portions (410, 420) of one or more thin-film transistors on the received film such that they are tilted relative to the periodic structure of the thin film.

WO 03/018882 A1

A METHOD TO INCREASE DEVICE-TO-DEVICE UNIFORMITY FOR POLYCRYSTALLINE THIN-FILM TRANSISTORS BY DELIBERATELY MIS-ALIGNING THE MICROSTRUCTURE RELATIVE TO THE CHANNEL REGION

SPECIFICATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based on United States provisional patent application serial no. 60/315,181, filed August 27, 2001, which is incorporated herein by reference for all purposes and from which priority is claimed.

BACKGROUND OF THE INVENTION

[0002] Technical Field. The present invention relates to semiconductor processing techniques, and more particularly, techniques for fabricating semiconductors suitable for use at thin-film transistor ("TFT") devices.

[0003] Background Art. Semiconductor films, such as silicon films, are known to be used for providing pixels for liquid crystal display devices and organic light emitting diode display devices. Such films are commonly processed via excimer laser annealing ("ELA") methods, where an amorphous silicon film is irradiated by an excimer laser to be crystallized.

[0004] Significant effort has gone into the refinement of "conventional" ELA (also known as line-beam ELA) processes in the attempt to improve the performance of the TFT devices placed on the processed semiconductor thin films. For example, U.S. Patent No. 5,766,989 issued to Maegawa et al., the entire disclosure of which is incorporated herein in its entirety by reference, describes the ELA methods for forming polycrystalline thin film and a method for fabricating a TFT. The '989 patent attempts to address the problem of non-uniformity of characteristics across the substrate, and provide certain options for apparently suppressing such non-uniformities.

[0005] However, the details of the beam-shaping approach used in conventional ELA methods make it extremely difficult to reduce the non-uniformities in the semiconductor films and to improve the performance characteristics of such films. For example, in a low-temperature polycrystalline silicon ("LTPS") process, when the size of the grains becomes

comparable to the dimensions of the channel region of the TFT, large device-to-device non-uniformity results. This is caused by the randomness of the microstructure, i.e., the random location of the grains and thus the grain boundaries. Such non-uniformity, especially when perpendicular to the current flow, can act as a current barrier. Further, when the transistor is in its off-state, carriers are generated at the grain boundary, which contribute to the off-current. This is especially the case when the grain boundary is in or close to the drain–channel junction.

[0006] Therefore, it has been realized that control over the microstructure is needed in order to ensure a uniform TFT process, both with respect to periodicity and location. Regarding the former, the film should be uniform, exhibiting periodicity in the location of the grains and thus the grain boundaries. Regarding the latter, the location of the grains and thus the grain boundaries should be controlled so that their contribution to the electrical characteristics is the same for every single device.

[0007] In an pulsed-laser, e.g., an excimer laser, irradiaton process to obtain LTPS films, control over the TFT microstructure may be obtained through the use lithography to induce such periodicity. The use of lithography also accounts for location control, since the accurate alignment procedure of the lithographic process is used. Unfortunately, the use of lithography requires at lease one extra processing step, which in turn increases complexity and thus costs.

[0008] Alternatively, control over the TFT microstructure may be obtained through the use of sequential lateral solidification ("SLS") techniques. For example, in U.S. Patent No. 6,322,625 issued to Im and U.S. patent application serial no. 09/390,537 (the "'537 application"), which is assigned to the common assignee of the present application, the entire disclosures of which are incorporated herein by reference, particularly advantageous apparatus and methods for growing large grained polycrystalline or single crystal silicon structures using energy-controllable laser pulses and small-scale translation of a silicon sample to implement sequential lateral solidification have been described. As described in these patent documents, at least portions of the semiconductor film on a substrate are irradiated with a suitable radiation pulse to completely melt such portions of the film throughout their thickness. In this manner, when the molten semiconductor material solidifies, a crystalline structure grows into the solidifying portions from selected areas of the semiconductor film which did not undergo a complete melting. Thereafter, the beam pulses irradiate slightly offset from the crystallized areas so that the grain structure extends into the molten areas from the crystallized areas.

[0009] Using the system shown in Fig. 1, an amorphous silicon thin film sample is processed into a single or polycrystalline silicon thin film by generating a plurality of excimer

laser pulses of a predetermined fluence, controllably modulating the fluence of the excimer laser pulses, homogenizing the modulated laser pulses in a predetermined plane, masking portions of the homogenized modulated laser pulses into patterned beamlets, irradiating an amorphous silicon thin film sample with the patterned beamlets to effect melting of portions thereof corresponding to the beamlets, and controllably translating the sample with respect to the patterned beamlets and with respect to the controlled modulation to thereby process the amorphous silicon thin film sample into a single or polycrystalline silicon thin film by sequential translation of the sample relative to the patterned beamlets and irradiation of the sample by patterned beamlets of varying fluence at corresponding sequential locations thereon.

[0010] While the system of Fig. 1 is highly advantageous in generating uniform, high quality polycrystalline silicon and single crystal silicon which exhibit periodicity and thereby solves a problem inherent with conventional ELC techniques, the technique does adequately not account for control over grain boundaries. For example, in the simplest form, SLS requires two pulses to crystallize the amorphous precursor into an LTPS film with partial periodicity, e.g., the 2-shot material shown schematically in Figure 2a. The periodicity is only in one direction, shown by long grain boundaries 210, 220, 230, 240, 250 that are parallel to each other and which also have a protrusion to them. However, the position of the short grain boundaries is not at all controlled. The spacing between the parallel grain boundaries can be increased, and this material is in general called n-shot material. Likewise, Figure 2b shows a so-called 4-shot material in which the grain boundaries are periodic in both directions. Again, the spacing between the grain boundaries can be increased, and is generally referred to as 2n-shot material.

[0011] While SLS techniques offer periodicity, such techniques do not offer accurate control of the location of grain boundaries. Referring to Figures 2c-d, the LTPS film produced includes a varying number of long grain boundaries perpendicular to the current flow, and the possibility of having a perpendicular grain boundary in or out of a TFT drain region. Both problems become more severe when grain size is increasing and/or when channel dimensions are decreasing, i.e., when the size of the grains becomes comparable to the dimensions of the channel region. While there has been a suggestion in United States Patent No. 6,177,301 to Jung to misalign TFT channel regions with respect to the grain growth direction, that suggestion is made without taking into account the underlying need to maintain uniformity in TFT microstructure. Accordingly, there exists a need for a TFT manufacturing technique that provides for control over both the periodicity of grain boundaries and the location of TFTs in order to provide for uniformity in TFT microstructure.

SUMMARY OF THE INVENTION

[0012] An object of the present invention is to provide a TFT manufacturing technique that provides for control over both the periodicity of grain boundaries and the location of TFTs in order to provide for uniformity in TFT microstructure.

[0013] Another object of the present invention is to provide a device having uniformity in TFT microstructure.

[0014] In order to meet these and other objects of the present invention which will become apparent with reference to further disclosure set forth below, the present invention provides methods of making a polycrystalline silicon thin-film transistor having a uniform microstructure. One exemplary method requires receiving a polycrystalline silicon thin film having a grain structure which is periodic in at least a first direction, and placing at least portions of one or more thin-film transistors on the received film such that they are tilted relative to the periodic structure of said thin film. The polycrystalline silicon thin film may be formed by a sequential lateral solidification process, e.g., a two shot sequential lateral solidification process.

[0015] Advantageously, the portions of said one or more thin-film transistors may be active channel regions having a width W. Where the periodic structure of the thin film is λ and m is a variable, the placing step involves placing active channel regions on the received film such that they are tilted at an angle θ relative to said periodic structure of said thin film, where $W \sin(\theta) = m \lambda$. The variable m is selected such that that the number of grain boundaries in any of the one or more thin-film transistors remains relatively controlled, and is preferably approximately equal to an integer.

[0016] The present invention also provides a device including a polycrystalline silicon thin-film transistor having a uniform microstructure. In an exemplary embodiment, the device includes polycrystalline silicon thin film having a grain structure which is periodic in at least a first direction, and at least portions of one or more thin-film transistors, placed on the thin film such that they are tilted relative to said periodic structure of the film.

[0017] The accompanying drawings, which are incorporated and constitute part of this disclosure, illustrate preferred embodiments of the invention and serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Fig. 1 is a functional diagram of a prior art system for performing semiconductor processing including sequential lateral solidification;

[0019] Figs. 2a-b are illustrative diagrams showing exemplary processed silicon samples using the prior art system of Fig. 1;

[0020] Figs. 2c-d are illustrative diagrams showing the prior art placement of active channel regions of TFTs on the exemplary processed silicon samples shown in Fig. 2a;

[0021] Figs 3a-b. are illustrative diagrams showing the placement of active channel region of TFTs on the exemplary processed silicon samples shown in Fig. 2a in accordance with the present invention;

[0022] Figs 4a-b. are illustrative diagrams showing the placement of active channel region of TFTs on the exemplary processed silicon samples shown in Fig. 2a in accordance with the present invention; and

[0023] Figs 5a-b. are illustrative diagrams showing the placement of active channel region of TFTs on the exemplary processed silicon samples shown in Fig. 2a in accordance with the present invention.

[0024] Throughout the Figs., the same reference numerals and characters, unless otherwise stated, are used to denote like features, elements, components or portions of the illustrated embodiments. Moreover, while the present invention will now be described in detail with reference to the Figs., it is done so in connection with the illustrative embodiments.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0025] Referring again to Figs. 2a-b, exemplary processed silicon thin films using the prior art SLS system of Fig. 1 are shown. In particular, Fig. 2a illustrates a sample processed by irradiating a region with a single excimer laser pulse, micro-translating the sample, and irradiating the region with a second excimer laser pulse. While the following exemplary description of the invention will be with respect to this so-called "2-shot" material as an example, those skilled in the art will appreciate that the present invention is more broadly applicable to silicon thin films that have been processed with n-shot and 2n-shot SLS techniques.

[0026] In accordance with the present invention, active channel regions of TFTs are deliberately tilted relative to the periodic microstructure of the processed thin film. Such tilting may be accomplished by tilting the placement of the channel region itself on the processed thin film, or alternatively, by fabricating a thin film during SLS processing which includes a tilted periodic grain structure. A combination of both alternatives may also be employed.

[0027] The precise methodology for placing TFTs on the processed thin film is not important to the present invention, and hence any known technique may be employed,. One exemplary technique is disclosed in U.S. Patent No. 5,766,989 to Maegawa et al., the contents of which are incorporated by reference herein.

[0028] When the active channel regions of TFTs are deliberately tilted relative to the periodic microstructure of the processed thin film., the spread in the number of perpendicular or long grain boundaries becomes less, leading to an increased device-to-device uniformity. In accordance with the present invention, the tilting angle (θ) should, however, not be too large, as not to increase the influence of the parallel, or short, grain boundaries. The ideal value of θ can be derived from equation (1), in which W is the width of the channel region, λ is the spacing between the perpendicular grain boundaries, and m is preferably close to an integer in value:

$$W * \sin(\theta) = m * \lambda, \tag{1}$$

[0029] In order to measure performance N of the TFT, equation (2) may be employed, where L is the length of the channel region, and n is a determined ratio:

$$L \cos(\theta) = n * \lambda, \tag{2}$$

[0030] In equation (2), a lower value of the ration n implies increased performance. L is often defined by the design rule of the process and is equal for all TFTs, and typically ranges from 3 to 6 µm. W, however, can be adjusted to match the requirements on the TFT properties, and typically ranges from 10 to 100s µm. The spacing λ between the perpendicular brain boundaries typically ranges from 2 to 10 µm , but smaller and larger values are possible.

[0031] Referring next to Figs. 3a-b, a first example of the present invention will be described. In this example, the ratio n =1, m =1, and θ = 10 degrees. As shown in Figs. 3a-b, all devices contain one perpendicular grain boundary, regardless of any translation of the TFT device, e.g., from the position shown in Fig 3a to that shown in Fig. 3b.

[0032] Referring next to Figs. 4a-b, a second example of the present invention will be described. In this example, the ratio n = 0.5, m = 1, and θ = 10 degrees. As shown in Figs. 4a-b, the channel region contains two portions, a first 410 in which one perpendicular grain boundary is present, and a second 420 in which no perpendicular grain boundary is present.

[0033] In latter portion 420, the device exhibits behavior as that of a TFT in fully directionally solidified material in which carriers are not hampered by grain boundaries. As shown in Figs. 4a-b, the relative contribution of each of these two parts is again invariable to any translation of the device, e.g., from the position shown in Fig 4a to that shown in Fig. 4b.

[0034] While the examples shown in Figs, 3-4 are considered to be the ideal scenarios, where m is an integer, small deviations from use of an integer value may be used in accordance with the present invention. However, the deviation from an integer value must be selected such that the number of grain boundaries in any given TFT remains relatively controlled.

[0035] Referring next to Figs. 5a-b, further examples of the present invention will be described. In Fig. 5a, the ratio $n = 2.1$, $m = 1$, and $\theta = 10$ degrees; in Fig. 5b, the ratio $n = 2.1$, $m = 0.5$, and $\theta = 5$ degrees. As shown in Figs. 5a-b, for the ideal value of θ, the number of grain boundaries is again invariable to any translation of the device. However, when θ deviates from this value, translations increasingly change the number of grain boundaries. When n equals, or is very close to, an integer the number of grain boundaries is essentially invariant for changes in θ. Of course it should exceed a certain value to assure that the fraction of perpendicular grain that is in the drain region is also invariant to translations.

[0036] The foregoing merely illustrates the principles of the invention. Various modifications and alterations to the described embodiments will be apparent to those skilled in the art in view of the teachings herein. It will thus be appreciated that those skilled in the art will be able to devise numerous systems and methods which, although not explicitly shown or described herein, embody the principles of the invention and are thus within the spirit and scope of the invention.

CLAIMS

1. A method of making a polycrystalline device including two or more thin-film transistors of substantially uniform microstructure, comprising the steps of:

(a) receiving a polycrystalline silicon thin film having a grain structure which is periodic in at least a first direction; and

(b) placing at least portions of two or more thin-film transistors on said received film tilted at an angle relative to said periodic structure of said thin film, such that that the number of long grain boundaries in any of said portions remains substantially uniform.

2. The method of claim 1, wherein said receiving step comprises the step of receiving a polycrystalline silicon thin film formed by a sequential lateral solidification process.

3. The method of claim 1, wherein said portions of said two or more thin-film transistors comprise active channel regions having a width W.

4. The method of claim 3, wherein said periodic structure of said thin film is λ, m is a variable, and said placing step comprises the step of placing said active channel regions on said received film such that said active channel regions are tilted at an angle θ relative to said periodic structure of said thin film, where $W \sin(\theta) = m \lambda$.

5. The method of claim 4, wherein m substantially equal to an integer.

6. The method of claim 4, wherein m is equal to an integer.

7. The method of claim 4, wherein m is equal to the integer 1.

8. A method of making a device including thin-film transistors, comprising the steps of:

(a) receiving a polycrystalline silicon thin film having a grain structure which is periodic in at least a first direction in an amount λ; and

(b) placing at least portions of one or more thin-film transistors having a width W on said received film tilted at an angle θ relative to said periodic structure λ of said thin film, such that $W \sin(\theta) = m \lambda$, where m is substantially equal to an integer.

9. The method of claim 8, wherein said receiving step comprises the step of receiving a polycrystalline silicon thin film formed by a sequential lateral solidification process.

10. The method of claim 8, wherein said portions of said one or more thin-film transistors comprise active channel regions having a width W.

11. The method of claim 10, wherein m is equal to an integer.

12. The method of claim 10, wherein m is equal to the integer 1.

13. A device including two or more polycrystalline silicon thin-film transistors of substantially uniform microstructure, comprising:

(a) a polycrystalline silicon thin film having a grain structure which is periodic in at least a first direction; and

(b) at least two or more thin-film transistor portions placed on said received film, each tilted at an angle relative to said periodic structure of said thin film, such that that the number of long grain boundaries in any of said portions remains substantially uniform.

14. The device of claim 13, wherein said polycrystalline silicon thin film comprises thin film formed by a sequential lateral solidification process.

15. The device of claim 13, wherein said portions of said two or more thin-film transistors comprise active channel regions having a width W.

16. The device of claim 13, wherein said periodic structure of said thin film is λ, m is a variable, and said active channel regions are tilted at an angle θ relative to said periodic structure of said thin film, where $W \sin(\theta) = m \lambda$.

17. The device of claim 16, wherein m is substantially equal to an integer.

18. The device of claim 16, wherein m is equal to an integer.

19. The device of claim 16, wherein m is equal to the integer 1.

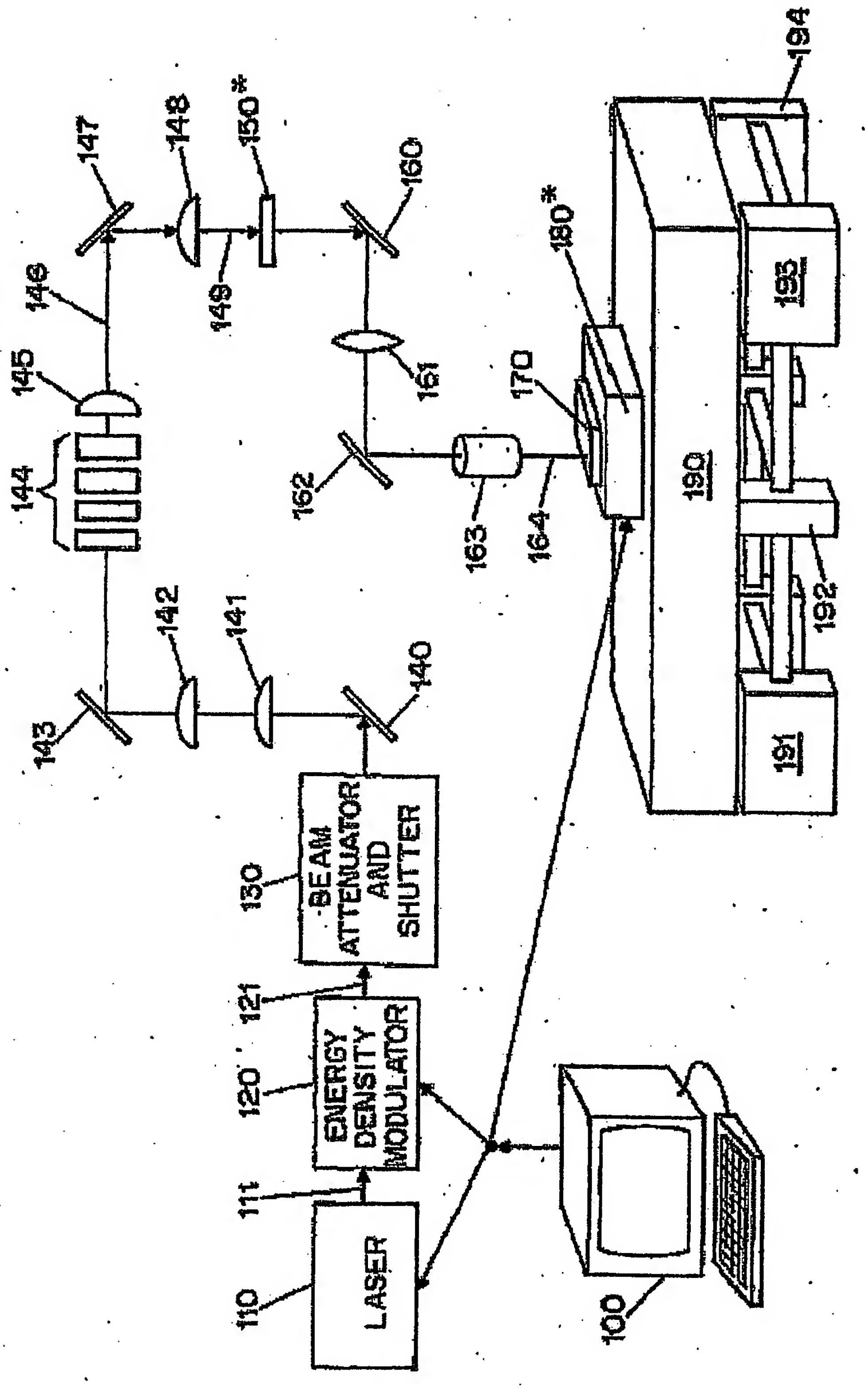


FIG. 1 (Prior Art)

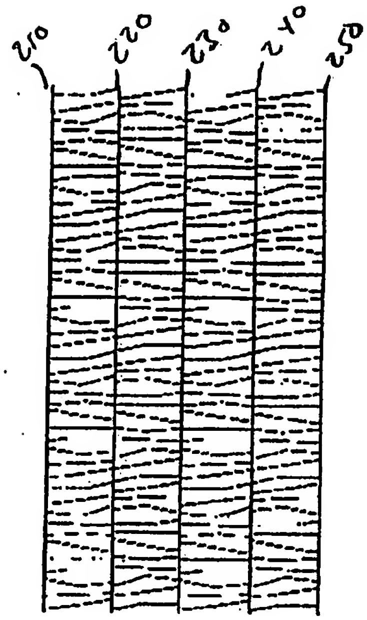


figure 2a

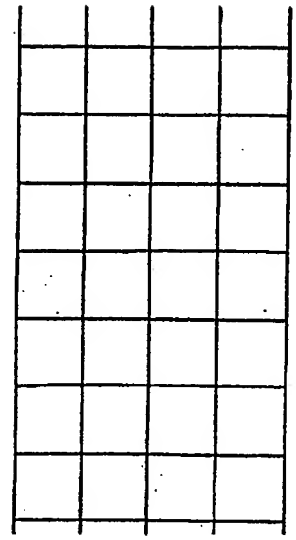


Figure 2b

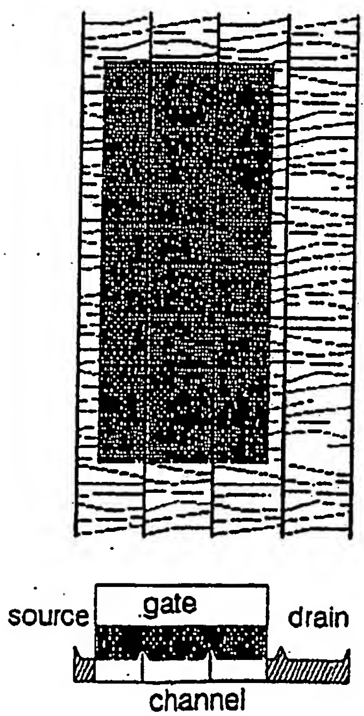


Figure 2c

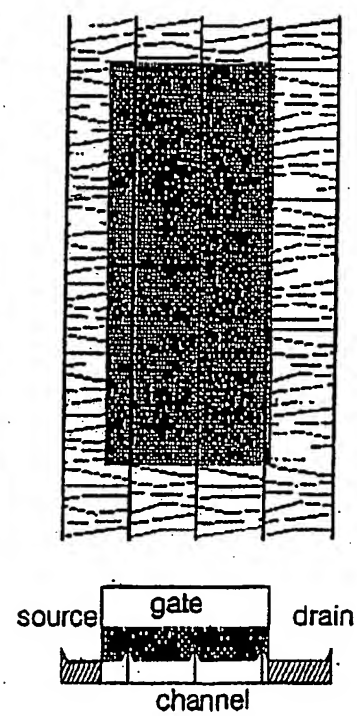


Figure 2d

Fig 3a

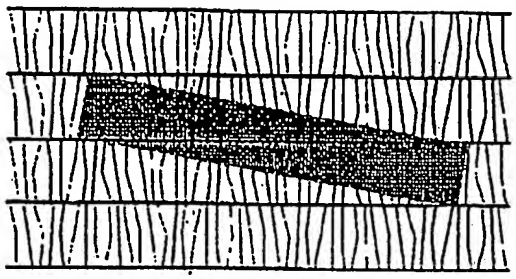


Fig 3b

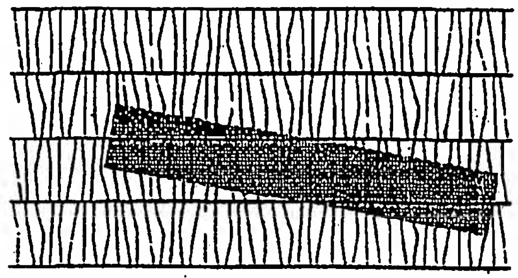


figure 3. n =1 and m = 1, θ = 10°

Fig 4a

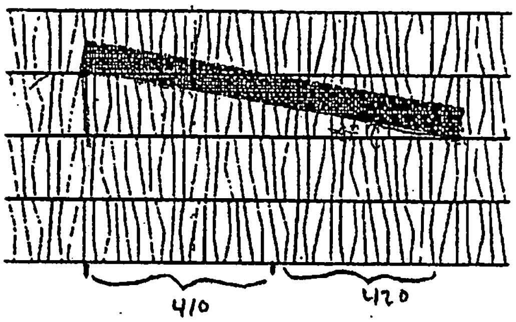


Fig 4b

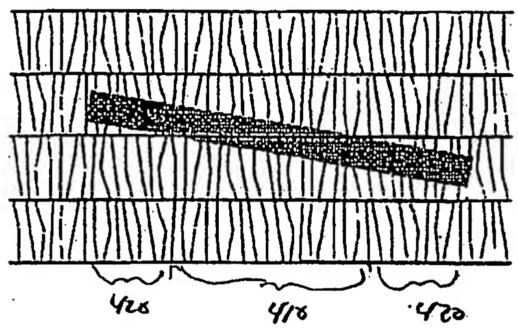


figure 4. n = 0.5, m = 1, θ = 10°

Fig 5a

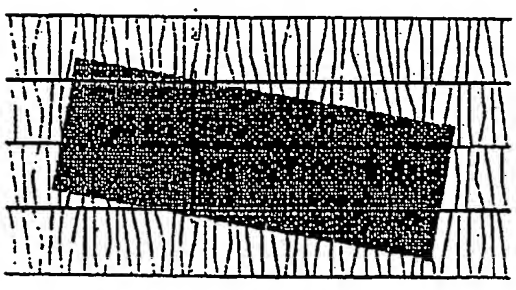


Fig 5b

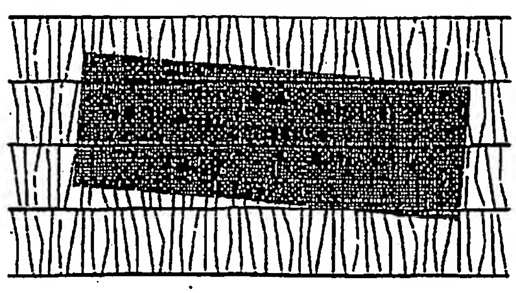


figure 5. left: n = 2.1, m = 1, θ = 10°, right: n = 2.1, m ~ 0.5, θ = 5°

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/27246

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : C30B 13/00
US CL : 117/43
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 117/37, 44, 45, 46, 54, 56, 73, 74, 904, 923; 438/149, 166, 479, 481, 486, 487, 488, 490, 779; 257/45, 75

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,P	US 6,322,625 B2 (IM) 27 November 2001 (27.11.2001), Figs. 9 and 10 plus description.	1-19
A	US 4,977,104 A (SAWADA et al) 11 December 1990 (11.12.1990), Fig. 8.	1-19
A	US 6,162,711 A (MA et al) 19 December 2000 (19.12.2000), col. 5, lines 39-47.	1-19
A	US 2001/0001745 A1 (IM et al.) 24 May 2001 (24.5.2001), Figs. 9 and 10, and descriptions.	1-19

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 November 2002 (13.11.2002)	11 DEC 2002
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Benjamin Utech Telephone No. (703) 308-0661

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
16 October 2003 (16.10.2003)

PCT

(10) International Publication Number
WO 03/084688 A2

(51) International Patent Classification⁷: B21C

(21) International Application Number: PCT/US03/09861

(22) International Filing Date: 1 April 2003 (01.04.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/369,186 1 April 2002 (01.04.2002) US

(71) Applicant (*for all designated States except US*): THE TRUSTEES OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK [US/US]; 116th Street and Broadway, New York, NY 10027 (US).

(72) Inventors; and
(75) Inventors/Applicants (*for US only*): IM, James, S. [US/US]; 520 West 114th Street, Apt. 74, New York, NY 10027 (US). CHOI, Jae, Beom [KR/US]; 145 East Central Blvd., 2nd Floor, Palisades Park, NJ 07650 (US).

(74) Agents: TANG, Henry et al.; Baker & Botts, LLP, 30 Rockefeller Plaza, New York, NY 10112-4498 (US).

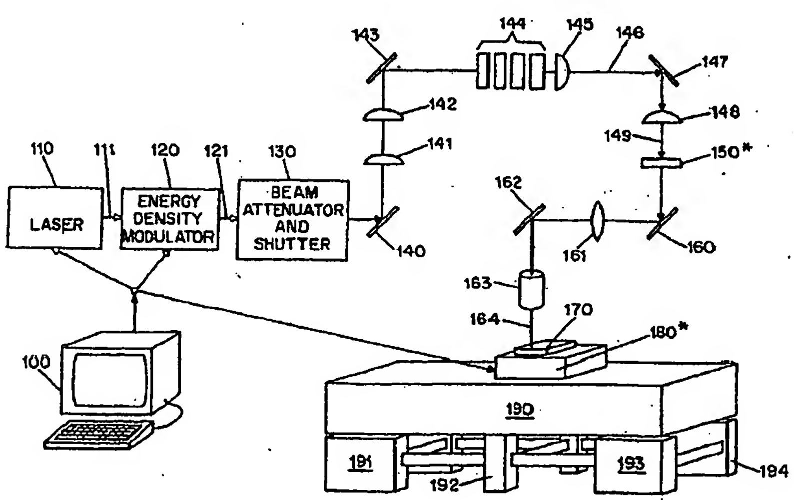
(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD AND SYSTEM FOR PROVIDING A THIN FILM WITH A CONTROLLED CRYSTAL ORIENTATION USING PULSED LASER INDUCED MELTING AND NUCLEATION-INITIATED CRYSTALLIZATION



(57) Abstract: Method and system for generating a metal thin film with a uniform crystalline orientation and a controlled crystalline microstructure are provided. For example, a metal layer is irradiated with a pulsed laser to completely melt the film throughout its entire thickness. The metal layer can then resolidify to form grains with a substantially uniform orientation. The resolidified metal layer can be irradiated with a sequential lateral solidification technique to modify the crystalline microstructure (*e.g.*, create larger grains, single-crystal regions, grain boundary controlled microstructures, etc.) The metal layer can be irradiated by patterning a beam using a mask which includes a first region capable of attenuating the pulsed laser and a second region allowing complete irradiation of sections of the thin film being impinged by the masked laser beam. An inverse dot-patterned mask can be used, the microstructure that may have substantially the same as the geometric pattern as that of the dots of the mask.

WO 03/084688 A2

Method and System for Providing a Thin Film with a Controlled Crystal Orientation Using Pulsed Laser Induced Melting and Nucleation-Initiated Crystallization

Cross-Reference to Related Application(s)

This application claims priority from United States Application Serial No. 60/369,186 filed April 1, 2002, the entire disclosure of which is incorporated herein by reference.

Notice of Government Rights

The U.S. Government may have certain rights in this invention pursuant to the terms of the Defense Advanced Research Project Agency award number N66001-98-1-8913.

Field of the Invention

The present invention relates to a system and process for producing a metal thin film having a uniform crystal orientation and controlled microstructure. In particular, the system and process of the present invention utilize a pulsed laser beam in conjunction with sequential lateral solidification ("SLS") techniques to produce, e.g., an aluminum thin film with, preferably, a (111) crystal orientation.

Background of the Invention

An inherent problem in the production of metallic thin films is minimizing the electro-migration that occurs in the metal interconnects. The electro-migration results in the transport of metal material of an interconnect line, and is caused when free electrons dislodge the atoms of the conductive material upon the current density increase that occurs due to smaller cross-sectional dimensions of the interconnect lines. The electro-migration occurs due to the transfer of momentum from the electrons flowing in a metal conductor when the conductor fails, because of a void or break in the conductor. This phenomenon is generally known as an "electron wind." The failure occurs most often along the grains of the conductive material since the atoms are not as firmly bound along the grains, and the grains provide efficient paths for the electron transport. These grains may extend in a direction which is parallel to the direction of the interconnect lines, i.e., along the direction of the current flow, which is considered to be particularly undesirable (i.e., such grain direction results in

an increased electro-migration). If vacancies or voids are formed in the conductive material, the void that is formed reduces the cross-sectional area in a region of the interconnect through which the current may flow, effectively raising the current density of that region of the interconnect even further. Therefore, the void may become so large that an open circuit or a break in the interconnect line results. Alternatively, the atoms of the conducting material that are dislodged may accumulate in a region of the interconnect so as to form a protrusion. If the protrusion becomes large enough, a contact with an adjacent interconnect may occur, thereby causing an undesired connection between the adjacent interconnect lines.

As the features of integrated semiconductor circuit chips are reduced, the cross-section of the metal interconnect lines on the integrated circuit chips are also reduced. This decrease in the cross-sectional dimensions increases the current density in the interconnect lines, which creates increased electro-migration in the metal interconnects. Moreover, the electro-migration would likely increase with a presence of a random orientation of the microstructure of the thin film. Since increasing the grain size to be larger than the metallization line width and preparing semiconductor films with a uniform orientation would reduce the propensity for electro-migration failure, there is a need for a system and method to control crystallization, and produce thin films with the substantially uniform orientation of the microstructure of the thin film.

Control over the thin film microstructure may be obtained through the use of sequential lateral solidification ("SLS") techniques. For example, U.S. Patent No. 6,322,625 (the "'625 application"), U.S. Patent Application Serial Nos. 60/239,194 (the "'194 application"), 09/390,535 (the "'535 application"), 09/390,537 (the "'537 application"), 60/253,256 (the "'256 application"), 09/526,585 (the "'585 application") and International Patent Application Nos. PCT/US01/31391 and PCT/US01/12799, the entire disclosures of which are hereby incorporated herein by reference, describe advantageous apparatus and methods for growing large grained polycrystalline or single crystal structures using energy-controllable laser pulses and small-scale translation of a sample to implement the SLS techniques. As described in these patent documents, at least portions of the semiconductor film on a substrate are irradiated with a suitable radiation pulse to completely or partially melt such portions of the film throughout their thickness. In this manner, when the molten semiconductor material solidifies, a crystalline structure grows into the solidifying portions from selected

areas of the semiconductor film which did not undergo a complete melting. Thereafter, the beam pulses irradiate slightly offset from the crystallized areas so that the grain structure extends into the molten areas from the crystallized areas. With the SLS techniques, and the systems described therein, crystallization may be controlled to modify the microstructure of the thin film (e.g., by creating larger grains, single-crystal regions, grain-boundary-location-controlled microstructures), and produce grains with a particular orientation.

Summary of the Invention

One of the objects of the present invention is to produce at least one section of a metal layer having a uniform crystal orientation and a controlled microstructure. In particular, the present invention may be used to produce an aluminum metal layer having a controlled crystal orientation of microstructures provided therein. For example, a pulsed laser beam may be utilized in conjunction with a sequential lateral solidification ("SLS") technique to produce a (111) crystal orientation of an aluminum thin film with.

In one exemplary embodiment of the present invention, a method and system are provided for processing a sample having a metal layer to generate a polycrystalline film with a controlled crystal orientation. In particular, at least one portion of the metal layer can be irradiated with a pulsed laser, so that the metal layer is completely melted throughout its entire thickness. Such portion of the metal layer is then resolidified via the crystalline growth, so that the grains of the metal layer have a substantially uniform orientation therein. In another embodiment of the present invention, the metal layer may be deposited on a substrate, which may be done by sputtering, evaporation or any conventional method. In yet another exemplary embodiment, the metal layer may be composed of aluminum or an aluminum alloy (e.g., an aluminum-copper alloy, an aluminum-silicon alloy, an aluminum-copper-silicon alloy etc.) In a further embodiment of the present invention the substantially uniform orientation may be a (111) orientation

In still another exemplary embodiment of the present invention, the metal layer can be irradiated without patterning (i.e., flood irradiate) to obtain grains with a uniform orientation. The metal layer is then irradiated using the SLS technique, as described in the above-identified patent applications. Certain masks and mask patterns can be used for the SLS techniques to generate various shapes of grain

boundaries for modifying the microstructure. This is done by, e.g., creating larger grains, single-crystal regions, grain-boundary-location-controlled microstructures, etc.

In a still further embodiment of the present invention, a mask used during the sequential solidification technique includes a first region capable of attenuating the pulsed laser and a second region which allows substantially the entire intensity of the corresponding portion of the pulsed laser to pass therethrough. The mask may be an inverse dot-patterned mask. The entire thin film can be completely melted throughout its entire thickness and the attenuation may be such that the region of the metal layer corresponding to the first region reaches a lower temperature than the melting temperature of the metal layer and lower than that the temperature of the section of the metal layer irradiated by the beam that is shaped by the second region. In yet another embodiment of the present invention, the dot patterns of the mask can be spaced closer than the super lateral growth distance which is based on the relevant process temperature. The inverse dot-patterned mask can include dots arranged in a geometric pattern such that the microstructure of the metal layer irradiated using such mask crystallizes in substantially the same geometric pattern as the arrangement of the dots of the inverse dot-patterned mask. The dots of the inverse dot-patterned mask may also be arranged to irradiate the metal layer microstructure in a manner to a hexagonal pattern or a square pattern therein.

Brief Description of the Drawings

For a better understanding of the present invention, together with other and further objects thereof, reference is made to the following description, taken in conjunction with the accompanying drawings, and its scope will be pointed out in the appending claims.

Figure 1 shows a block diagram of a system for performing a preferred embodiment of a lateral solidification process according to an exemplary embodiment of the present invention;

Figure 2 shows an illustration of a section of an exemplary aluminum thin film sample after pulsed laser irradiation to induce complete melting and subsequent solidification of a section of an aluminum sample;

Figure 3 shows an enlarged representation of a portion of the section illustrated in Figure 2;

Figure 4 shows inverse pole symbols representing the nucleated aluminum grains of the sample of Figure 3 illustrating that the nucleated aluminum grains have a (111) orientation;

Figure 5 shows an exemplary embodiment of an inverse dot-patterned mask with the dot patterns arranged in a hexagonal form, which may be used with the exemplary system and process according to the present invention;

Figure 6 shows an exemplary temperature profile of the melted aluminum thin film sample after irradiation of a portion thereof with the inverse dot-patterned mask of Figure 5;

Figure 7 shows an exemplary section of the sample after the Sequential lateral solidification ("SLS") is utilized using the inverse dot-patterned mask of Figure 5;

Figure 8 shows an enlarged illustration of approximately hexagonal portions of the sample shown in Figure 7;

Figure 9 shows inverse pole symbols representing nucleated aluminum grains of the sample of Figures 7 and 8 illustrating that the nucleated aluminum grains have a (111) orientation; and

Figure 10 shows a flow diagram of an exemplary embodiment of a method according to the present invention which can be implemented by the system of Figure 1.

Throughout the Figures, the same reference numerals and characters, unless otherwise stated, are used to denote like features, elements, components or portions of the illustrated embodiments. Moreover, while the present invention will now be described in detail with reference to the Figures, it is done so in connection with the illustrative embodiments.

Detailed Description

In one exemplary embodiment of the present invention, a uniform crystalline orientation of at least one section of a metal thin film may be obtained using the sequential lateral solidification process. Therefore, in order to fully understand the present invention, the sequential lateral solidification process is further described. As disclosed in aforementioned patent applications, the sequential lateral solidification ("SLS") process is a technique for producing large grained thin films through small-scale unidirectional translation of a sample between sequential pulses emitted by an excimer laser. As each pulse is absorbed by the sample, a small area of the sample is

caused to melt completely, and then resolidify laterally into a crystal region produced by the preceding pulses of a pulse set. It should be understood that various systems according to the present invention may be utilized to generate, nucleate, solidify and crystallize one or more areas on the thin film (e.g., composed of aluminum) which have uniform material therein, such that at least an active region of a thin-film transistor ("TFT") may be placed in such areas. The exemplary embodiments of the systems and processes of the present invention to generate such areas, as well as those of the resulting crystallized metal thin films, shall be described in further detail below. However, it should be understood that the present invention is in no way limited to the exemplary embodiments of the systems, processes and semiconductor thin films described herein.

Figure 1 shows a system that includes excimer laser 110, energy density modulator 120 to rapidly change the energy density of laser beam 111, beam attenuator and shutter 130, optics 140, 141, 142 and 143, beam homogenizer 144, lens system 145, 146, 148, a mask or masking system 150, lens system 161, 162, 163, incident laser pulse 164, thin metal film sample 170, sample translation stage 180, granite block 190, support system 191, 192, 193, 194, 195, 196, and managing computer 100. As described in further detail in the '535 application, a non-processed thin film sample 170 may be processed into a single or polycrystalline metal thin film by generating a plurality of excimer laser pulses of a predetermined fluence, controllably modulating the fluence of the excimer laser pulses, homogenizing the modulated laser pulses in a predetermined plane, masking portions of the homogenized modulated laser pulses into patterned beamlets, irradiating an amorphous silicon thin film sample with the patterned beamlets to effect melting of portions thereof corresponding to the beamlets, and controllably translating the sample with respect to the patterned beamlets and with respect to the controlled modulation to thereby process the amorphous thin film sample into a single or polycrystalline thin film by sequential translation of the sample relative to the patterned beamlets and irradiation of the sample by patterned beamlets of varying fluence at corresponding sequential locations thereon. The laser system may include a laser source, optics, mask, and projection system, which may be substantially the same as or similar to the equipment used for other SLS systems and processes.

In an exemplary embodiment of the present invention, the method and system may be used to generate metal thin films (e.g., aluminum film) with a uniform

crystalline orientation. The thin film may be composed of aluminum alloys such as, e.g., Al-Cu, Al-Si, Al-Cu-Si, etc. In such exemplary embodiment, the concentration of the impurities may preferably be less than 20%.

The aluminum thin film sample may be deposited on a substrate by various methods, such as sputtering, evaporation, etc. In one exemplary embodiment of the present invention, it is possible to use the polycrystalline aluminum films without the need to place it on a substrate. In one exemplary embodiment, at least one portion of the aluminum thin film layer is irradiated with a pulsed laser (e.g., an excimer laser) without patterning of the beam pulse (i.e. flood irradiation). The entire portion of the metal layer is completely melted, preferably throughout its entire thickness. The completely melted liquefied section of the aluminum thin film solidifies via nucleation and crystalline growth thus resulting in an aluminum thin film as shown in Figure 2. Figure 3 shows a representation of an enlarged portion of the resolidified section illustrated in Figure 2 indicating that the complete melting and solidification of the section(s) of the aluminum thin film results in grain boundaries 200 and grain shapes 202 that are relatively random.

According to another exemplary embodiment of the present invention, the resolidified (and possibly nucleated) grains of the aluminum layer provided as a substrate can have a substantially uniform orientation after irradiation and solidification. The nucleated aluminum grains likely have a uniform (111) orientation. Such exemplary orientation of the aluminum grains may preferably occur through the heterogeneous nucleation at an interface between liquid aluminum and the substrate. For example, the (111) planes of the aluminum grains likely have the lowest surface energy, which reduces the activation energy for the heterogeneous nucleation. Thus, the (111) orientation of the aluminum grains is thermodynamically preferred according to the present invention. Figure 4 shows inverse pole symbols representing an exemplary portion of the resolidified section of the aluminum thin film of Figure 2 illustrating that the crystallized aluminum grains have various orientations, and in particular, a (111) orientation. In an exemplary embodiment of the system and process according to the present invention, it is possible to obtain the (111)-oriented polycrystalline aluminum films by positioning the sample 170 in a predetermined manner and subjecting the thin film to the SLS processing. This can be done after the thin film is subject to flood irradiation.

In another exemplary embodiment of the present invention, it is possible to initially irradiate a portion of the aluminum thin film sample without patterning (i.e., by flood irradiating), so as to allow the irradiated portions of thin film to solidify, so as to obtain grains having a (111) orientation, and then irradiate such previously-irradiated portion of the metal layer using the SLS process, as described in the above-identified patent applications and patents. Depending on the masks and their mask patterns (the examples of which are described and shown in the above-identified applications and patents), it is possible to generate various shapes of grain boundaries so as to modify the metal microstructure and the orientation of the grains thereof (e.g., by creating larger grains, single-crystal regions, grain-boundary-location-controlled microstructures, etc.).

The mask 150 may include a first region capable of attenuating the pulsed laser and a second region that allows the associated portions of complete pulsed laser to irradiate therethrough. For example, an inverse dot-patterned mask may be used in which the dots are arranged in a geometric pattern such that the microstructure of the metal layer crystallizes substantially corresponds to the geometric shape of the arrangement of the dots of the mask pattern. In a further embodiment of the present invention, similarly to the conventional SLS techniques which utilize dot-patterned masks, the dot patterns on such mask should be spaced closer to one another than the super lateral growth distance corresponding to the relevant process temperature. As described in the applications and patents identified herein above, the dot regions of the inverse dot patterned mask may be arranged to form a metal layer with a hexagonal microstructure as shown in Figure 5. In particular, the exemplary mask of Figure 5 includes a first region 500 that attenuates the beam intensity and a second region 502 that allows the beam to pass therethrough to reach and irradiate the aluminum thin film. It is preferable for the energy density of the beam to be large enough to completely melt the intended sections of the aluminum thin film, including the regions masked by the dots 500. Since the dots 500 are opaque, and the beam is significantly attenuated in those regions, the aluminum thin film area positioned to be irradiated by the dot regions (although completely melted) would likely not reach as high of a temperature as that of the areas outside the dot regions (which are also completely melted) as is shown in Figure 6. In particular, the temperature 501 in the attenuated region o f the aluminum thin film should be lower than the melting temperature of the film so that at least some of (111) nucleated grains that are formed

remain as solids (e.g., via a previous irradiation such as the flood irradiation) to seed the molten metal around those solid regions into the (111) oriented grains.

As the film cools, the section of the aluminum thin film irradiated by the section of the laser beam masked the dot regions nucleates, thus, providing the (111) oriented seeds that grow laterally into the non-masked areas in accordance with the principles of SLS techniques described in the above-identified U.S. and International patent applications and patents. In particular the dot-patterned SLS techniques described therein. As described in these patent documents, the microstructure that is obtained depends on the geometry of the dot regions of the mask 150. Therefore, as shown in Figures 7 and 8, the use of the exemplary inverse dot-patterned mask of Figure 5 to mask the laser beam and irradiate the aluminum thin film results in crystallized aluminum film with a hexagonal microstructure. Figure 8 shows an enlarged representation of a portion of the section provided in Figure 7 further illustrating the locations and shapes of the grain boundaries 800, 802, respectively. Figure 9 shows inverse pole symbols representing the portion of the section provided in Figure 8 that illustrate that the crystallized aluminum grains have substantially a (111) orientation. In a further exemplary embodiment of the present invention, the dot regions of the inverse dot patterned mask may be arranged so as to generate the sections of the metal thin film with square microstructure therein.

Referring to Figure 10, exemplary steps executed by computer 100 of Figure 1 to control the irradiation and grain orientation of the metal thin film is described. The various electronics of the system shown in Figure 1 are initialized by the computer to initiate the process in step 1000. A thin metal (aluminum) film sample 170 is then loaded onto the sample translation stage in step 1005. It should be noted that such loading may be either manual or robotically implemented under the control of the computer 100.

Next, the sample translation stage 180 is moved into an initial position in step 1010, which may include an alignment with respect to reference features on the sample 170. The various optical components of the system are focused in step 1015 if necessary. The laser is then stabilized in step 1020 to a desired energy level and repetition rate, as needed to fully melt the metal thin film sample 170 in accordance with the particular processing to be carried out. If necessary, the attenuation of the laser pulses is finely adjusted (step 1025).

Next, the sample 170 is positioned to point the beam to impinge on the first section of sample in step 1030. The beam 149 is masked with the appropriate mask pattern of the mask 150 (step 1035). It is also possible to not mask the beam prior to its impingement of the sample 170. After the beam 149 is masked to become a masked beam pulse 164, the masked beam pulse 164 irradiates at least one section of the metal (aluminum) thin film sample 170 to produce grains that have a particular (e.g., - 111) orientation in step 1040. Then, in step 1045, it is determined whether all intended areas of the thin metal film sample 170 have been irradiated in a predetermined manner. If not, the sample 170 is then translated in the X and/or Y directions in step 1050 for a distance which is less than the super lateral grown distance of the metal thin film using the SLS and/or non-SLS techniques. After processing all of the desired sections of the metal thin film sample 170, the beam and hardware are shut off in step 1055 and the process is completed in step 1060. If processing of additional samples is desired or steps 1005 – 1050 may be repeated for each such sample.

In addition, it is also possible to obtain the (111) oriented grains using the SLS techniques described above and without the flood irraditions being effectuated on the aluminum thin film prior to such SLS processing. In particulars, the desired sections of the aluminum thin film 170 are irradiated using the one of the patterned masks described above (e.g., the dot-patterned mask, the hexagonal-shaped mask, the rectangular shaped mask, etc.) and the SLS techniques in order to nucleate center areas corresponding to the such shapes (which allow some or all of the irradiation of the beam pulse to pass therethrough). The resolidified desired regions of the aluminum thin film 170 result in the (111) oriented grains, which are also grain boundary controlled grains. Accordingly, it is not necessary to subject the aluminum thin film 170 to flood irradiation prior to it being irradiated using the SLS processing technique.

The foregoing merely illustrates the principles of the invention. Various modifications and alterations to the described embodiments will be apparent to those skilled in the art in view of the teachings herein. For example, while the above embodiment has been described with respect to at least partial lateral solidification and crystallization of the semiconductor thin film, it may apply to other materials processing techniques, such as micro-machining, photo-ablation, and micro-patterning techniques, including those described in the above-identified patent documents. The

various mask patterns and intensity beam patterns described in the above-referenced patent application may also be utilized with the process and system of the present invention. It will thus be appreciated that those skilled in the art will be able to devise numerous systems and methods which, although not explicitly shown or described herein, embody the principles of the invention and are thus within the spirit and scope of the present invention.

Claims

1. A method for processing a sample having a metal thin film provided thereon to generate a polycrystalline film with a substantially uniform orientation, comprising the steps of:

(a) irradiating at least one portion of the metal thin film with a pulsed laser to completely melt the at least one portion throughout its entire thickness; and

(b) allowing the melted metal thin film to re-solidify after the at least one portion is melted, wherein the grains of the at least one resolidified portion of the metal thin film have the substantially uniform orientation.

2. The method according to claim 1, wherein the metal thin film is deposited on a substrate.

3. The method according to claim 2, wherein the metal thin film is deposited on a substrate by at least one of a sputtering procedure, an evaporation procedure and a further thin film deposition procedure.

4. The method according to claim 1, wherein the metal thin film is composed of aluminum.

5. The method according to claim 1, wherein the metal thin film is composed of an aluminum alloy, the aluminum alloy including at least one of an aluminum-copper alloy, an aluminum-silicon alloy and an aluminum-copper-silicon alloy.

6. The method according to claim 1, wherein the substantially uniform orientation is a (111) orientation.

7. The method according to claim 1, further comprising the step of:

(c) irradiating the at least one portion of the metal thin film with the laser pulse based on a sequential lateral solidification technique.

8. The method according to claim 7, wherein the laser pulse irradiating the at least one portion is patterned using a mask to modify a shape of the laser pulse.

9. The method according to claim 8, wherein the mask is comprised of a first region capable of attenuating the pulsed laser and a second region allowing a significant section of the laser beam impacting the second region to pass therethrough.

10. The method according to claim 9, wherein the mask is an inverse dot-patterned mask, and wherein the second region includes opaque array patterns which include at least one of dot-shaped areas, hexagonal-shaped areas and rectangular-shaped areas.

11. The method according to claim 10, wherein each portion of the metal thin film is completely melted throughout its entire thickness, and wherein an attenuation of the laser beam produced by the first region impinges associated section of the thin film to reach a temperature that is lower than a melting temperature of the metal thin film and lower than a temperature as further sections of the thin film corresponding with the areas irradiated by the second region.

12. The method according to claim 11, wherein dot patterns of the mask are spaced closer than a super lateral growth distance corresponding to a resolidification process temperature of the metal thin film.

13. The method according to claim 10, wherein the inverse dot-patterned mask is comprised of dots has a geometric pattern such that upon the irradiation of the metal thin film, a microstructure of the metal thin film solidifies and crystallizes in substantially the same geometric pattern as the pattern of the inverse dot-patterned mask.

14. The method according to claim 13, wherein the dots of the inverse dot-patterned mask are arranged in a pattern such that upon the irradiation of the metal thin film with the masked laser beam, a microstructure of the metal thin film is formed having one of a hexagonal pattern, a rectangular pattern and a square pattern.

15. The method according to claim 7, wherein, in step (a), a width of the at least one irradiated portion is greater than a super-lateral growth width of the metal thin film.

16. The method according to claim 1, wherein step (a) is performed using a sequential lateral solidification technique, and wherein, upon the execution of step (a), in step (b), grain-boundary location controlled grains are formed in the at least one portion of the metal thin film.

17. A system for producing at least one section of a polycrystalline metal film with a substantially uniform orientation, comprising:

a logic arrangement which is operable to:

(a) irradiate at least one portion of the at least one portion of the metal thin film to completely melt the at least one portion of the metal thin film throughout its entire thickness, and

(b) allow the at least one portion of the melted metal thin film to re-solidify after the at least one is melted, wherein the grains of the at least one portion have the substantially uniform orientation upon the re-solidification.

18. The system according to claim 17, wherein the metal thin film is deposited on a substrate.

19. The system according to claim 18, wherein the metal thin film is deposited on a substrate by at least one of a sputtering procedure, an evaporation procedure and a further thin film deposition procedure.

20. The system according to claim 17, wherein the metal thin film is composed of aluminum.

21. The system according to claim 17, wherein the metal thin film is composed of an aluminum alloy, the aluminum alloy including at least one of an aluminum-copper alloy, an aluminum-silicon alloy and an aluminum-copper-silicon alloy.

22. The method according to claim 17, wherein the substantially uniform orientation is a (111) orientation.

23. The system according to claim 17, where the logic arrangement is further operable to irradiate the at least one portion of the thin film sample with a sequential lateral solidification technique.

24. The system according to claim 23, wherein the laser pulse irradiating the at least one portion is patterned using a mask to modify a shape of the laser pulse.

25. The system according to claim 24, wherein the mask is comprised of a first region capable of attenuating the pulsed laser and a second region allowing a significant section of the laser beam impacting the second region to pass therethrough.

26. The system according to claim 25, wherein the mask is an inverse dot-patterned mask, and wherein the second region includes opaque array patterns which include at least one of dot-shaped areas, hexagonal-shaped areas and rectangular-shaped areas.

27. The system according to claim 26, wherein each portion of the metal thin film is completely melted throughout its entire thickness, and wherein an attenuation of the laser beam produced by the first region impinges associated section of the thin film to reach a temperature that is lower than a melting temperature of the metal thin film and lower than a temperature as further sections of the thin film corresponding with the areas irradiated by the second region.

28. The system according to claim 27, wherein dot patterns of the mask are spaced closer than a super lateral growth distance corresponding to a resolidification process temperature of the metal thin film.

29. The system according to claim 28, wherein the inverse dot-patterned mask is comprised of dots has a geometric pattern such that upon the irradiation of the metal thin film, a microstructure of the metal thin film solidifies and

crystallizes in substantially the same geometric pattern as the pattern of the inverse dot-patterned mask.

30. The system according to claim 29, wherein the dots of the inverse dot-patterned mask are arranged in a pattern such that upon the irradiation of the metal thin film with the masked laser beam, a microstructure of the metal thin film is formed having one of a hexagonal pattern, a rectangular pattern and a square pattern.

31. The system according to claim 17, wherein the logic arrangement irradiates the at least one portion of metal using a sequential lateral solidification technique, and wherein, upon the completion of step (b), grain-boundary location controlled grains are formed in the at least one portion of the metal thin film.

32. A polycrystalline metal film, comprising:

at least one portion which is irradiated to be completely melted throughout its entire thickness, wherein the at least one portion is re-solidified after being melted, and wherein the at least one portion include grains which have a substantially uniform orientation upon the re-solidification of the at least one portion.

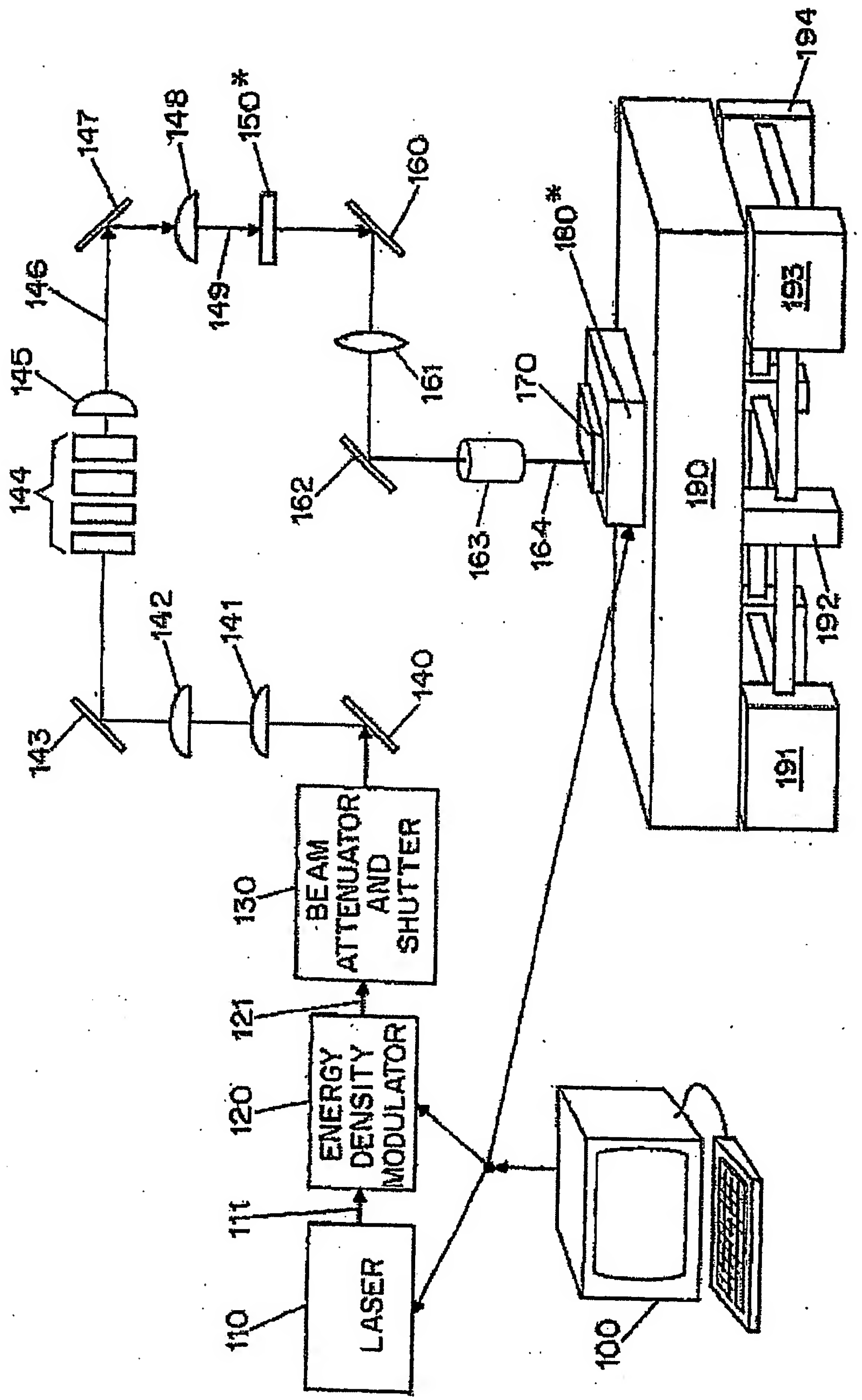

LASER
ENERGY DENSITY MODULATOR
BEAM ATTENUATOR AND SHUTTER
110
111
120
121
130
140
141
142
143
144
145
146
147
148
149
150*
160
161
162
163
164
170
180*
190
191
192
193
194
100

FIGURE 1

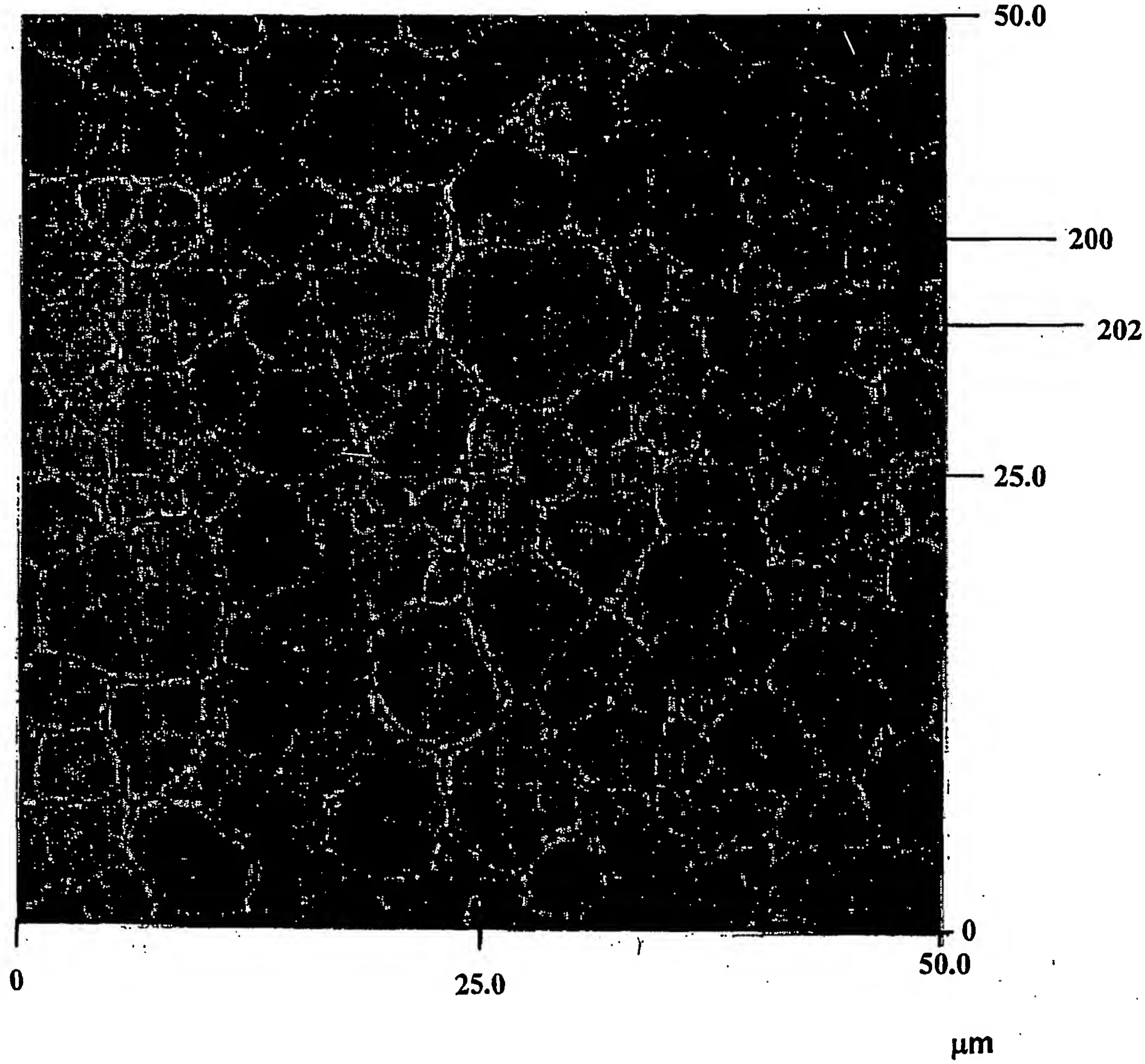


FIGURE 2

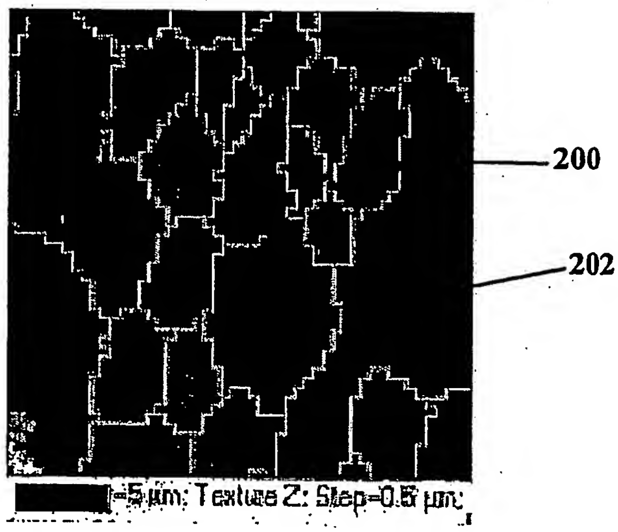


FIGURE 3

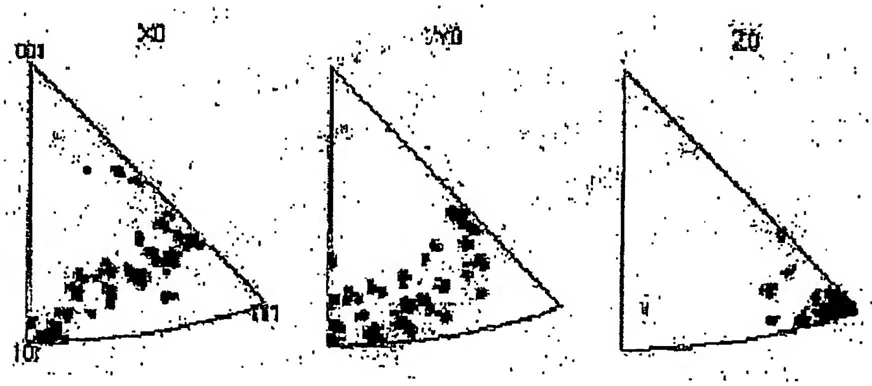


FIGURE 4

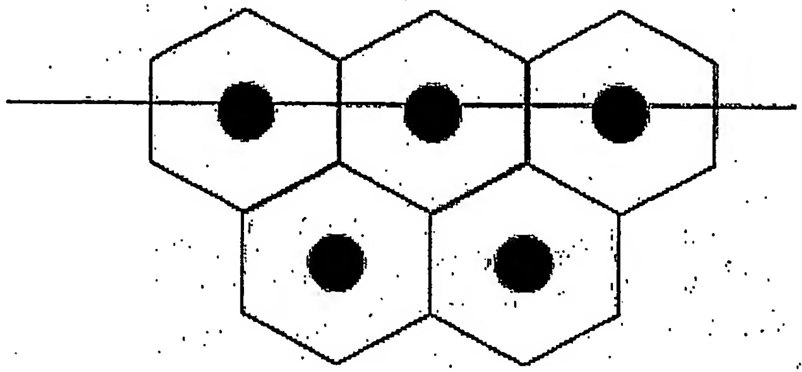


FIGURE 5

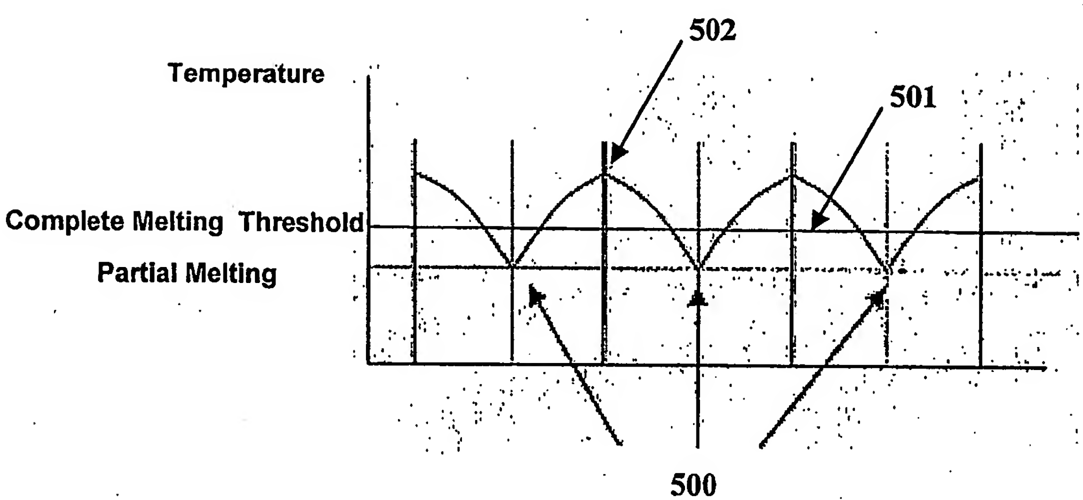


FIGURE 6

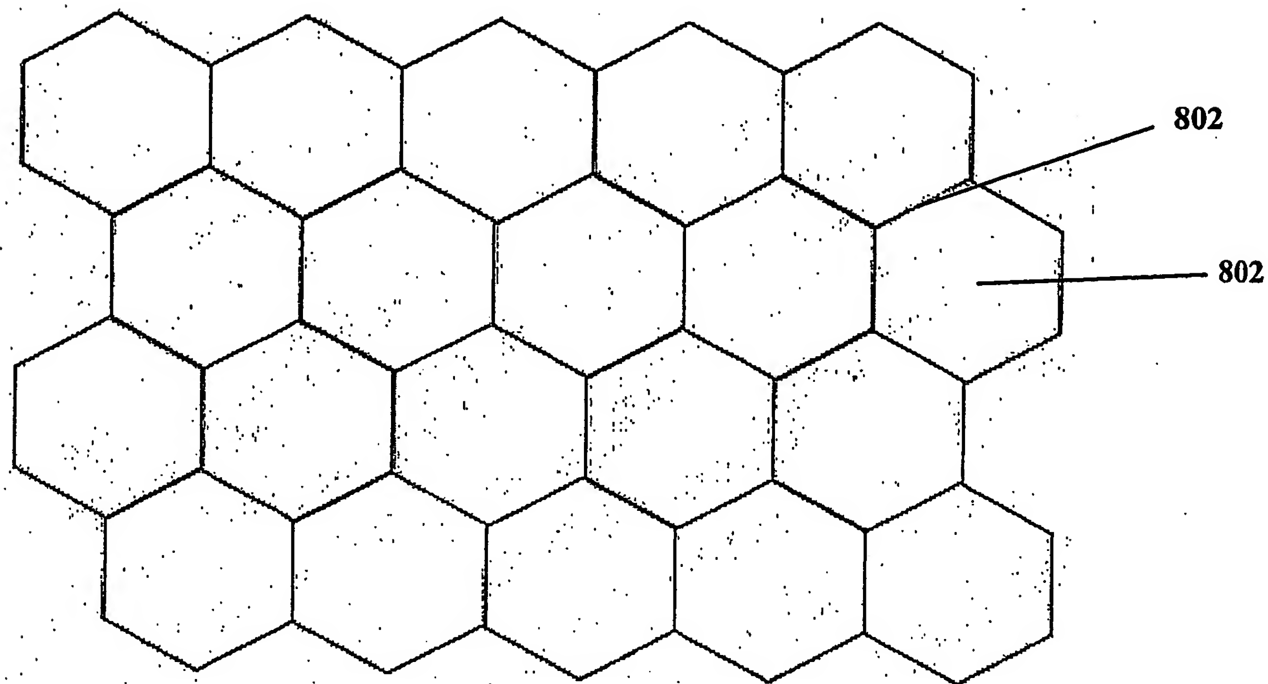


FIGURE 7

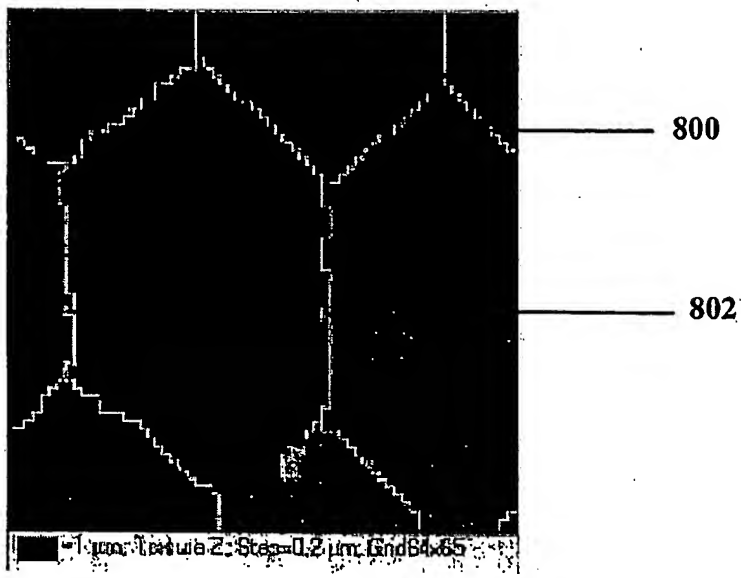


FIGURE 8

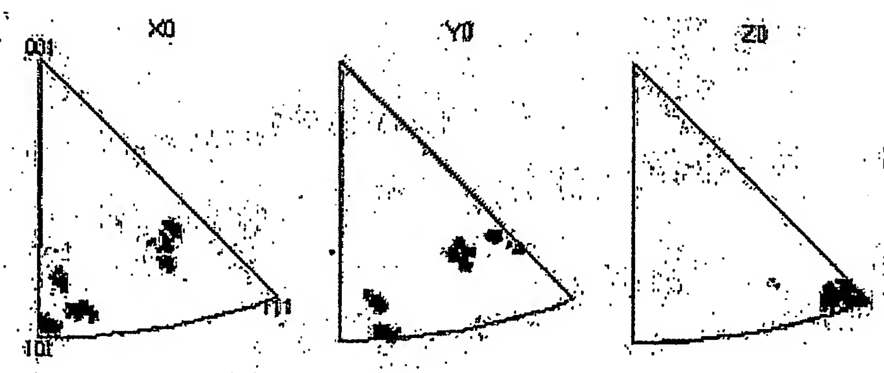
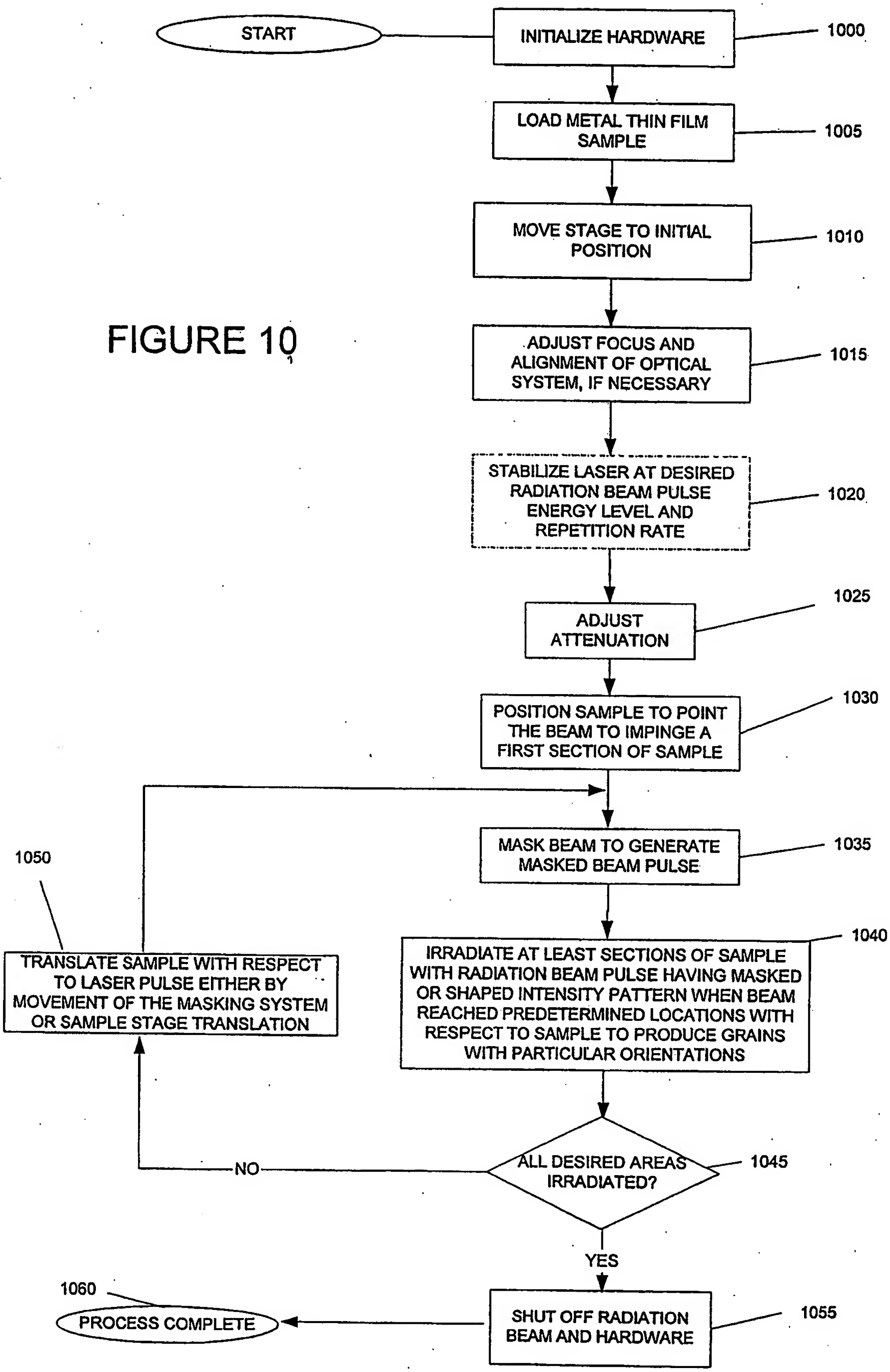


FIGURE 9

FIGURE 10


START
INITIALIZE HARDWARE
1000
LOAD METAL THIN FILM SAMPLE
1005
MOVE STAGE TO INITIAL POSITION
1010
ADJUST FOCUS AND ALIGNMENT OF OPTICAL SYSTEM, IF NECESSARY
1015
STABILIZE LASER AT DESIRED RADIATION BEAM PULSE ENERGY LEVEL AND REPETITION RATE
1020
ADJUST ATTENUATION
1025
POSITION SAMPLE TO POINT THE BEAM TO IMPINGE A FIRST SECTION OF SAMPLE
1030
MASK BEAM TO GENERATE MASKED BEAM PULSE
1035
IRRADIATE AT LEAST SECTIONS OF SAMPLE WITH RADIATION BEAM PULSE HAVING MASKED OR SHAPED INTENSITY PATTERN WHEN BEAM REACHED PREDETERMINED LOCATIONS WITH RESPECT TO SAMPLE TO PRODUCE GRAINS WITH PARTICULAR ORIENTATIONS
1040
ALL DESIRED AREAS IRRADIATED?
1045
NO
1050
TRANSLATE SAMPLE WITH RESPECT TO LASER PULSE EITHER BY MOVEMENT OF THE MASKING SYSTEM OR SAMPLE STAGE TRANSLATION
YES
SHUT OFF RADIATION BEAM AND HARDWARE
1055
PROCESS COMPLETE
1060

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
31 October 2002 (31.10.2002)

PCT

(10) International Publication Number
WO 02/086955 A1

(51) International Patent Classification[7]: H01L 21/28, 27/115, 29/788

(21) International Application Number: PCT/IB02/01320

(22) International Filing Date: 11 April 2002 (11.04.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
01201459.3 23 April 2001 (23.04.2001) EP

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventor: DORMANS, Guido, J., M.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: DUIJVESTIJN, Adrianus, J.; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

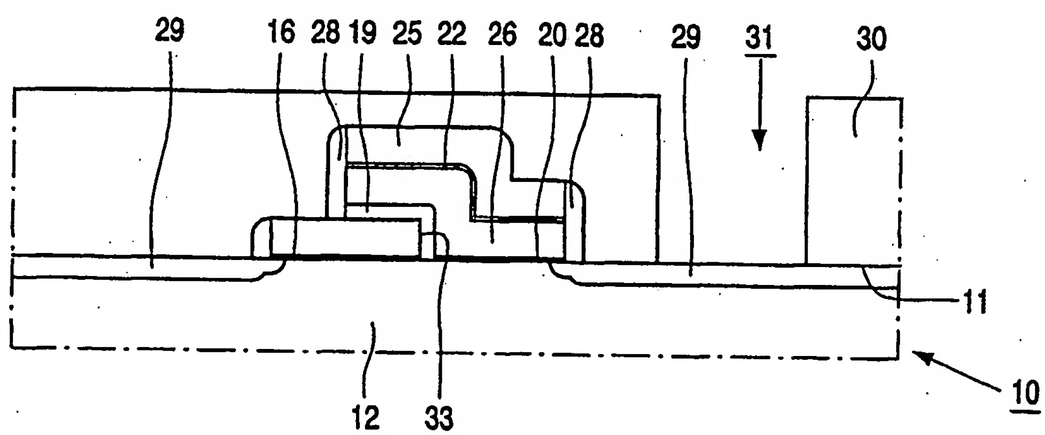
(81) Designated States (*national*): JP, KR.

(84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SAME



(57) Abstract: The invention relates to a semiconductor device comprising a semiconductor body (10) which is provided with an active semiconductor region (12) which borders on a surface (11) of said semiconductor body, which active semiconductor region is provided with a non-volatile memory cell comprising a source zone and a drain zone (29), a select gate (18), and a stacked gate structure (32) comprising a floating gate (26) and a control gate (25). The stacked gate extends above the select gate and covers a side wall (33) of said select gate, which side wall extends at least substantially perpendicularly to the surface of the semiconductor body. The stacked gate structure is insulated from the select gate by a layer of an insulating material (19, 35) that is applied to the select gate. The select gate and the floating gate, viewed along the surface of the semiconductor body, are situated at a distance from each other, which distance is determined by the thickness of the layer of insulating material applied to the select gate's side wall (33) which extends at least substantially perpendicularly to the surface of the semiconductor body, which thickness enables a continuous channel to be formed between the source zone and the drain zone.

WO 02/086955 A1

Semiconductor device and method of manufacturing same

The invention relates to a semiconductor device comprising a semiconductor body including an active semiconductor region which borders on a surface of said semiconductor body and which is provided with a non-volatile memory cell comprising a source region, a drain region, a select gate, and a stacked gate structure comprising a floating gate and a control gate, which stacked gate structure projects beyond the select gate and covers the wall of the select gate that extends at least substantially transversely to the surface, said stacked gate structure being insulated from the select gate by a layer of an insulating material. The invention also relates to a method of manufacturing such a device.

In this semiconductor device, the stacked gate structure of a memory transistor overlaps the select gate of a select transistor. By virtue thereof, the memory cell can be formed on a comparatively small part of the surface of the semiconductor body, while the stacked gate structure occupies a comparatively large surface area. A comparatively large stacked gate structure has the advantage that a comparatively large capacitive coupling is possible between the control gate and the floating gate, as a result of which the memory cell can be read using low voltages.

US 5,550,073 discloses a semiconductor device of the type mentioned in the opening paragraph, wherein, viewed along the surface, between the select gate of the select transistor and the floating gate of the memory transistor, there is formed, in the active region, a connection region which borders on the surface and is of opposite conductivity type to the active region. During reading such a memory cell, this connection region interconnects inversion regions that are formed, in the active region, below the select gate and below the floating gate. As the connection region is present between the inversion regions, the electric resistance between the inversion regions is minimal. As a result, during reading at a low voltage, there is a comparatively high, readily detectable current flow. A drawback of the connection region is, however, that it occupies a comparatively large surface area, as a result of which the memory cell is comparatively large.

It is an object of the invention to provide a semiconductor device comprising a memory cell which can be formed on a smaller part of the surface than the memory cell of the known semiconductor device described hereinabove.

To achieve this, the semiconductor device mentioned in the opening paragraph is characterized in that the select gate and the floating gate, viewed along the surface, are situated at a distance from each other that is determined by the thickness of the layer of insulating material applied to the wall of the select gate, said wall extending substantially transversely to the surface, and said thickness enabling a continuous channel to be formed between the source region and the drain region. Surprisingly, it has been found that the thickness of the layer of insulating material against the select gate wall extending at least substantially transversely to the surface, which thickness determines the distance between the select gate and the floating gate, can be chosen to be such that a connection region as used in the known memory cell described hereinabove can be dispensed with. By virtue thereof a substantial gain in space is achieved. Despite the absence of this connection region, it has been found that the inversion regions, which are formed during reading of the memory cell below the select gate and below the floating gate in the active semiconductor region, blend so well with each other that a negligibly small series resistance is present between said inversion regions, resulting in a continuous channel between the source region and the drain region. At a read voltage between 0.5 and 1 volt, a read current ranging between 30 and 50 μA is generated which can be readily detected in practice. In this respect, it is advantageous if the thickness of the layer of insulating material against the select gate wall extending at least substantially transversely to the surface is smaller than 70 nm. Preferably, this thickness is smaller than 50 nm and larger than 30 nm. The distance between the select gate and the floating gate preferably is not below 30 nm to avoid excessive parasitic coupling between the select gate and the floating gate. As a result of such parasitic coupling, writing data in and erasing data from the memory cell would be less effective. At an equal voltage on the control gate, the voltage difference between the floating gate and the underlying active semiconductor region would be smaller. As a result, writing and erasing data would take longer. To compensate this, the memory would have to be operated at higher write and erase voltages, which is undesirable.

In order to further reduce said parasitic coupling, the layer of insulating material is provided on the select gate in a thickness that is preferably larger than the thickness of the layer of insulating material against the select gate wall extending at least

substantially transversely to the surface. By virtue thereof, parasitic coupling is reduced while the distance between the select gate and the floating gate can be maintained at a value that enables a continuous channel to be formed. In practice, said parasitic coupling is negligibly small if the layer of insulating material on top of the select gate has a thickness above 100 nm.

The invention also relates to a method of manufacturing a semiconductor device comprising a non-volatile memory cell, wherein

- a semiconductor body is provided, at a surface, with an active semiconductor region;
- a select gate is provided, which select gate is insulated from the active semiconductor region;
- the select gate is provided with a layer of an insulating material;
- a stacked gate structure comprising a floating gate and a control gate is provided, which stacked gate structure extends above the select gate and covers the select gate wall extending at least substantially transversely to the surface, which stacked gate structure is insulated from the select gate by means of the layer of insulating material and insulated from the active semiconductor region by means of a gate dielectric;
- the active semiconductor region is provided with a source region and a drain region, the select gate and the stacked gate structure being used as a mask.

Such a method is disclosed in the above-mentioned US 5,550,073, wherein, after the formation of the select gate, first the connection region is formed. Subsequently, the stacked gate structure is formed. To form the connection region, a 10 to 30 nm thick layer of silicon nitride is deposited, after the manufacture of the select gate, in a layer of heavily doped polycrystalline silicon. Next, the parts of the silicon nitride layer extending transversely to the surface are provided with spacers of silicon oxide. After etching away the silicon nitride, the spacers of silicon oxide remain at a distance of 10 to 30 nm from the select gate. While masking the select gate and said spacers, between which two 10 to 30 nm wide gaps are present, phosphor ions are implanted. After removal of the spacers and the underlying silicon nitride, an oxidation treatment is carried out, wherein a layer of silicon oxide is formed on the select gate, and an approximately 6 to 12 nm thick layer of tunnel oxide is formed on the surface next to the select gate. During this oxidation treatment, which is carried out at a high temperature, the phosphor ions diffuse in the silicon body and the connection region is formed. On the select gate of heavily doped polycrystalline silicon, the oxidation rate, using customary oxidation processes to form gate and tunnel oxides, is

substantially twice the rate that can be achieved when use is made of less heavily doped monocrystalline silicon, and a 12 to 24 nm thick silicon oxide layer will be formed. In practice, the phosphor ions will diffuse approximately 200 nm below the select gate and below the spacers, resulting in an approximately 500 nm wide connection region.

The semiconductor device in accordance with the invention can be manufactured much more readily because the process steps that are necessary to form the connection region are avoided. The method of manufacturing the device in accordance with the invention is characterized in that the layer of insulating material is applied to the select gate wall extending substantially transversely to the surface in a thickness which, viewed along the surface, determines the distance between the select gate and the floating gate and enables a continuous channel to be formed between the source region and the drain region.

For the gate dielectric, which insulates the stacked gate structure from the active semiconductor region, use can be made of various materials. Advantageously, however, use is made of silicon oxide for the gate dielectric, which gate dielectric is hereinafter referred to as tunnel oxide. A desirable thickness for the tunnel oxide lies in the range between 8 and 10 nm. To form a layer having a thickness in the range between 30 and 70 nm on the wall of the select gate, and to form a layer having a thickness between 8 and 10 nm on the surface of the semiconductor body, in this case a silicon body, use can be made, for example, of a customary oxidation process to form a 60 nm thick layer on the select gate. As a result, an approximately 30 nm thick layer is formed on the surface. By means of an etching treatment, during which the select gate is covered by a mask, the thickness of the tunnel oxide formed can be reduced to the desired value. A simpler solution is obtained if the silicon body is subjected to an oxidation treatment wherein said silicon body is heated to a temperature in the range between 600 and 800 °C in a gas mixture of a non-oxidizing carrier gas and water vapor. It has been found that, under such conditions, the rate at which a layer of silicon oxide grows on heavily doped non-crystalline silicon is six times the growth rate that is achieved on lightly doped monocrystalline silicon. Thus, when a 8 to 10 nm thick layer of tunnel oxide is formed, a 50 to 60 nm thick layer of silicon oxide forms on the select gate.

As noted hereinabove, advantageously, the thickness of the layer of insulating material on top of the select gate is larger than the thickness of said layer of insulating material covering the select gate wall extending at least substantially transversely to the surface. This can be readily achieved by providing a stack of a conductive layer and an insulating layer, and patterning this stack so as to form the select gate in the conductive layer.

Preferably, the insulating layer, which is provided on the conductive layer, is applied in a thickness above 100 nm.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

In the drawings:

Fig. 1 shows an electrical circuit diagram of an EEPROM memory comprising an array of memory cells arranged in rows and columns, as formed in the semiconductor device in accordance with the invention,

Fig. 2 through Fig. 10 are diagrammatic, cross-sectional plan views of several stages in the manufacture of a first example of the semiconductor device in accordance with the invention, which is manufactured by means of the method in accordance with the invention,

Fig. 11 through Fig. 16 are diagrammatic cross-sectional views of several stages in the manufacture of a second example of the semiconductor device in accordance with the invention, which is manufactured by means of the method in accordance with the invention.

Fig. 1 shows an electrical circuit diagram of an EEPROM memory comprising an array of memory cells M_{ij} arranged in rows and columns, where i represents the number in the row and j represents the number in the column. Each memory cell comprises a memory transistor T1 having a floating gate 1 and a control gate 2 and, arranged in series therewith, a select transistor T2 with a select gate 3. The control gates 2 of a number of memory transistors T1, for example eight or more, are interconnected per column by lines CGj, the select gates 3 of the select transistors T2 are interconnected per column by lines SGj. Furthermore, the memory transistors T1 are interconnected per row by bit lines BL_i, and the transistors T2 are interconnected by a source line SO that is shared by a number of memory cells.

The EEPROM memory in accordance with the invention, which will be described in greater detail hereinafter, can be operated in various ways. Data can be written in the memory cells and erased from said memory cells by Fowler-Nordheim tunneling, or, alternatively, data can be written by injection of "hot electrons" and erased by Fowler-

Nordheim tunneling. The following Tables show the voltages that can be applied to said lines in order to write data in one of the memory cells, in this case memory cell M_{11}, erase data from a column of memory cells, in this case memory cells M_{1j}, and read the content of one memory cell, in this case M_{11}.

In the first case:

	CG_1	SG_1	BL_1	$CG_{2..j..}$	$SG_{2..j..}$	$BL_{2...i..}$	SO
Writing	+12V	0V	0V	0V	0V	+6V	Open
Erasing	-12V	0V	0V	0V	0V	0V	Open
Reading	+1V	+3V	+1V	+1V	0V	0V	0V

In the second case:

	CG_1	SG_1	BL_1	$CG_{2..j..}$	$SG_{2..j..}$	$BL_{2...i..}$	SO
Writing	+10V	+1,5V	+5V	0V	0V	0V	0V
Erasing	-12V	0V	0V	0V	0V	0V	Open
Reading	+1V	+3V	+1V	+1V	0V	0V	0V

It is to be noted that the memory transistor T1 has a threshold voltage of approximately +2 V during writing, and of approximately –2 V during erasing.

Figs. 2 through 10 are diagrammatic, cross-sectional plan views of a few stages in the manufacture of a first example of the semiconductor device in accordance with the invention. Said Figures show, in a plan view, the manufacture of two juxtaposed memory cells and, in a cross-sectional view, the manufacture of the left memory cell.

As shown in Fig. 2, in a semiconductor body 10, for example a silicon body, active strip-shaped semiconductor regions 12 are formed at the location of the memory cells to be formed, which active strip-shaped semiconductor regions border on a surface 11 of the semiconductor body 10 and are bounded by field oxide regions 13. Said field oxide regions 13 also bound strip-shaped semiconductor regions 14 extending transversely to the strip-shaped active regions 12. The strip-shaped regions 14 are interconnected, outside the plane of the drawing, and form the above-mentioned common source line SO. In Fig. 2, the part of the surface 11 that is occupied by two memory cells is indicated by means of dot-dash lines 15. In this example, use is made of a customary, heavily doped silicon body which is provided with an epitaxially grown top layer which is comparatively lightly doped with approximately

10^{15} atoms per cc. In the top layer, the semiconductor regions 12 and 14 are formed. For the sake of simplicity, only this top layer is shown in the drawings of the silicon body 10.

As shown in Fig. 6, after the formation of the semiconductor regions 12 and 14, the surface 11 of the silicon body 10 is provided with a silicon oxide layer 16, in a customary manner by thermal oxidation of silicon bordering on the surface 11, which silicon oxide layer has a thickness between 5 and 10 nm, as a result of which the layer can suitably be used as a gate oxide of the select transistors T2. As shown in Fig. 3, on this layer of silicon oxide 16, a first system of mutually parallel strips 17 is subsequently formed in a first conductive layer, for example an approximately 150 nm thick layer of non-crystalline silicon, which is deposited on the layer of silicon oxide 16. The layer of non-crystalline silicon may be a layer of polycrystalline silicon or, alternatively, a layer of amorphous silicon. During the manufacture of the semiconductor device, where the semiconductor body is generally subjected several times to a treatment at a high temperature, said layer of amorphous silicon may convert to a layer of polycrystalline silicon. To form the strips, the layer of non-crystalline silicon is heavily n-type doped. As shown in Fig. 3, the strips 17 form, at the location of the active regions 12, the select gates 18 of the select transistors T2. Furthermore, the strips interconnect the select gates 18 of the select transistors T2 arranged in a column, and thereby form the lines SG.

After the formation of the strips of non-crystalline silicon 17, an implantation of boron ions is carried out, while masking the strips, using a dose of 10^{12} atoms per cm^2 to set the threshold voltage of the memory transistor T1 to be formed next to the select transistor T2. Subsequently, the parts of the silicon oxide layer 16 that are situated next to the strips 17 are removed and, as shown in Fig. 4, the select gate 18 is provided with a layer of an insulating material 19, in which process also a 8 to 10 nm thick silicon oxide layer 20 is formed on the surface 11 of the semiconductor body, next to the select gate 18, so that the layer can suitably be used as a tunnel oxide for the memory transistor.

Subsequently, a second conductive layer, for example a layer of n-type doped non-crystalline silicon, is deposited. As shown in Figs. 5 and 6, strips 21 are formed in said layer, which extend in the direction of the active regions 12 and transversely to the strips 17 formed in the first layer of non-crystalline silicon. Next, as shown in Fig. 7, a layer of an intermediate dielectric 22 is deposited on the structure thus formed, which intermediate dielectric is composed, in this case, of an approximately 6 nm thick layer of silicon oxide, an approximately 6 nm thick layer of silicon nitride and an approximately 6 nm thick layer of silicon oxide, which are successively deposited. A third conductive layer 23, for example a

layer of n-type doped non-crystalline silicon, is deposited on the layer of an intermediate dielectric 22.

In the third layer of non-crystalline silicon 23, strips 24 are formed, as shown in Fig. 10. The parts of the strips situated above the active regions 12 form the control gates 25 of the memory transistors T1. The control gates 25 of memory transistors arranged in columns are interconnected by the strips of non-crystalline silicon, so that said strips 24 form the lines CG of the memory.

While masking these strips 24, as shown in Fig. 8, also the layer of intermediate dielectric 22, the underlying strips 21 formed in the second layer of non-crystalline silicon and the silicon oxide layers 19 and 20 are etched in accordance with a pattern. The remaining parts of the strips 21 formed in the second layer of non-crystalline silicon form the floating gates 26 of the memory transistors T1. Control gate 25 and floating gate 26 are separated from each other by the layer of intermediate dielectric.

Subsequently, a customary source-drain-extension implantation with 10^{13} arsenic atoms per cm^2 is carried out, after which the source-drain-extension regions 27 are formed, as shown in Fig. 8, by means of a thermal treatment. After the silicon oxide spacers 28 are formed in a customary manner on the edges of the exposed edges of the strips 17 and 24, the source-drain regions 29 are formed by an implantation of 10^{15} arsenic ions per cm^2 and a subsequent thermal treatment.

Finally, as shown in Figs. 9 and 10, a layer of silicon oxide 30 is deposited and contact windows 31 are formed therein. The layer of silicon oxide 30 is provided with aluminum conductor tracks, not shown in said drawings, which make contact, in the contact holes 31, with the drain regions 29 of the memory transistors T1. These strips form the bit lines BL of the memory.

In this manner, as shown in Figs. 9 and 10, a semiconductor device is formed comprising a semiconductor body 10, in this example a silicon body, including an active semiconductor region 12, which is arranged so as to border on a surface 11 of said semiconductor body, which semiconductor region is provided with an EEPROM memory comprising an array of memory cells ME arranged in rows and columns, and including a select transistor T2 having a select gate 18 of, in this example, noncrystalline-doped silicon, which is situated on a gate oxide layer 16 formed on the surface 11, and also including a memory transistor T1 having a stacked gate structure 32 with a floating gate 26 of, in this example, noncrystalline-doped silicon, a layer of intermediate dielectric 22 and a control gate 25 of, in this example, noncrystalline-doped silicon, which stacked gate structure (?) is

situated on a tunnel oxide layer 20 formed on the surface 11 next to the select gate 18 and extends so as to be situated on top of the select gate 18 and covers the wall 33 thereof which extends at least substantially transversely to the surface, the stacked gate structure 32 being insulated from the select gate 18 by a layer of an insulating material 19.

The select gate 18 and the floating gate 26 are situated, viewed along the surface 11, at a distance from each other that is determined by the thickness of the layer of insulating material 19 which is present on the wall 33 of the select gate 18 and over which the stacked gate structure 32 extends. This thickness, which is such as to enable a continuous channel to be formed between the source region and the drain region, is preferably smaller than 70 nm, and preferably ranges between 30 and 50 nm. As a result, the inversion regions below the select gate 18 and below the floating gate 26, which inversion regions are formed during reading the memory cell, will merge so well that for reading the memory cell low voltages are sufficient. At such a small distance between the select gate and the floating gate, a negligibly small series resistance remains between said inversion regions. At a read voltage between 0.5 and 1 volt, the read current ranges between 30 and 50 μA, which can be readily detected in practice.

In order to reduce parasitic coupling between the select gate and the floating gate, the thickness of the layer of insulating material on top of the select gate preferably is larger than the thickness of said layer on the select gate wall that extends at least substantially transversely to the surface. As a result, parasitic coupling is reduced while the distance between the select gate and the floating gate can be maintained at a value enabling a continuous channel to be formed between the source region and the drain region. In practice, parasitic coupling is negligible if the layer of an insulating material on top of the select gate has a thickness above 100 nm, as in the case of the manufacture of the second example to be described of the semiconductor device in accordance with the invention.

In the manufacture of the first example, a semiconductor body 10, for example a silicon body, is provided with an active semiconductor region 12 bordering on a surface 11 of said semiconductor body, and, subsequently, with an array of memory cells ME arranged in rows and columns, including a select transistor T2 with a select gate 18 which is formed in a first conductive layer, for example a layer of non-crystalline silicon, which is deposited on a layer of gate oxide 16 formed on the surface 11, and including a memory transistor T1, which is arranged in series therewith, having a stacked gate structure 32 with a floating gate 26, intermediate dielectric 22 and control gate 25, which is formed in a second conductive layer 21, for example a layer of non-crystalline silicon, a layer of the intermediate dielectric

22 and a third conductive layer 23, for example a layer of non-crystalline silicon, which are successively deposited on the select gate 18 and on a juxtaposed tunnel oxide layer 20 formed on the surface 11. The gate structure 32 formed extends above the select gate 18 and covers the side wall 33 thereof which is directed transversely to the surface. The select gate 18 is provided with a layer of an insulating material 19 as a result of which the stacked gate structure 32 is insulated from the select gate 18.

Immediately after the formation of the select gate 18, as shown in Fig. 4, the tunnel oxide layer 20 is formed on the surface next to the select gate 18, and the side wall 33 of the select gate 18 is provided with a layer of silicon oxide 19 in a thickness enabling a continuous channel to be formed between the source region and the drain region, said thickness advantageously being below 70 nm, and preferably ranging between 30 and 50 nm. For the tunnel oxide layer 20, a desirable thickness ranges between 8 and 10 nm. In order to provide the wall 33 of the select gate 18 with a layer having a thickness between 30 and 70 nm and provide the surface with a layer having a thickness between 8 and 10 nm, for example, a layer having a thickness of 60 nm can be formed on the select gate using a customary oxidation process. As a result, an approximately 30 nm thick layer is formed on the surface. By means of an etch treatment, during which the select gate is covered with a mask, the thickness of the tunnel oxide formed can then be reduced to the desired value. A simpler solution is obtained if the silicon body is subjected to an oxidation treatment wherein the silicon body is heated to a temperature in the range between 600 and 800 °C in a gas mixture of a non-oxidizing gas, such as nitrogen, and water vapor. It has been found that, under such conditions, a silicon oxide layer grows on heavily doped non-crystalline silicon at a rate that is six times the rate of growth on lightly doped monocrystalline silicon. And, during the formation of an 8 to 10 nm thick tunnel oxide layer, a 50 to 60 nm thick silicon oxide layer forms on the select gate.

The memory with the memory cells ME described hereinabove can be manufactured on a very small part of the surface 11. The parts of the surface 11, indicated by means of dot-dash lines 15 in Figs. 2, 6 and 10, which comprise two memory cells, have dimensions of 600 by 800 nm per memory cell when use is made of a "0.18 μm process" (a technology enabling minimum details of 0.18 μm to be realized).

Figs. 11 through 16 are diagrammatic, cross-sectional views of a few stages in the manufacture of a second example of the semiconductor device in accordance with the invention. In these Figures, where possible, the same reference numerals are used as in the preceding Figures.

In this example, prior to the formation of the strips 17 in the first conductive layer, which is for example a layer of a non-crystalline silicon, this first conductive layer is covered with an insulating layer, for example a layer of silicon oxide, after which the strips 17 are formed in the first conductive layer, during which treatment the insulating layer, which is provided on the first conductive layer, is provided with a pattern. In this manner, the select gate 18 shown in Fig. 11 is formed, which is provided with an insulating top layer 35. This top layer 35, of course, also extends over the strips 17.

Subsequently, as shown in Fig. 12, after the removal of the part of the silicon oxide layer 16 that is situated next to the select gate, and after the above-mentioned implantation of boron ions, the above-mentioned oxidation treatment is carried out, wherein the side wall 33 of the select gate 18 is provided with an approximately 40 nm thick layer of silicon oxide 19 and the surface is provided with an approximately 8 nm thick tunnel oxide layer 20.

As shown in Fig. 13, after the formation of the insulating layers 19 and 20, the strips 21 are formed, just like in the first example, in the second conductive layer, for example a layer of non-crystalline silicon, after which, as shown in Fig. 14, the layer of intermediate dielectric 22 and the third conductive layer 23, for example a layer of non-crystalline silicon, are deposited. Next, the stacked gate structure 32 is formed comprising the floating gate 26 and the control gate 25. After the formation of the source and drain extension regions 27, the spacers 28 are formed, after which the source and drain regions 29 are formed and the whole is covered with the silicon oxide layer 30 wherein the contact windows 31 are etched.

The silicon oxide layer 35 on top of the select gate 18 can be readily provided in a thickness exceeding that of the silicon oxide layer 19 provided on the wall 33 of the select gate 18. Preferably, the layer 35 has a thickness above 100 nm. As a result, parasitic coupling between the select gate 18 and the floating gate 26 is negligibly small.

CLAIMS:

1. A semiconductor device comprising a semiconductor body (10) including an active semiconductor region (12) which borders on a surface (11) of said semiconductor body and which is provided with a non-volatile memory cell comprising a source region and a drain region (29), a select gate (18), and a stacked gate structure (32) comprising a floating gate (26) and a control gate (25), which stacked gate structure projects beyond the select gate and covers the wall (33) of the select gate that extends at least substantially transversely to the surface, said stacked gate structure being insulated from the select gate by a layer of an insulating material (19, 35), characterized in that the select gate and the floating gate, viewed along the surface, are situated at a distance from each other that is determined by the thickness of the layer of insulating material applied to the wall of the select gate, said wall extending substantially transversely to the surface, and said thickness enabling a continuous channel to be formed between the source region and the drain region.

2. A semiconductor device as claimed in claim 1, characterized in that the thickness of the layer of insulating material against the select gate wall extending at least substantially transversely to the surface is below 70 nm.

3. A semiconductor device as claimed in claim 1 or 2, characterized in that the thickness of the layer of insulating material against the select gate wall extending at least substantially transversely to the surface lies in the range between 30 and 50 nm.

4. A semiconductor device as claimed in any one of the preceding claims, characterized in that the select gate, viewed along the surface, is provided on the side of the stacked gate structure facing the source region.

5. A semiconductor device as claimed in any one of the preceding claims, characterized in that the layer of insulating material on top of the select gate has a larger thickness than the layer of insulating material against the select gate wall extending at least substantially transversely to the surface.

6. A semiconductor device as claimed in claim 5, characterized in that the layer of insulating material on top of the select gate has a thickness above 100 nm.

7. A method of manufacturing a semiconductor device comprising a non-volatile memory cell, wherein

- a semiconductor body (10) is provided, at a surface (11), with an active semiconductor region (12);
- a select gate (18) is provided, which select gate is insulated from the active semiconductor region;
- the select gate is provided with a layer of an insulating material (19, 35);
- a stacked gate structure (32) comprising a floating gate (26) and a control gate (25) is provided, which stacked gate structure extends above the select gate and covers the select gate wall (33) extending at least substantially transversely to the surface, which stacked gate structure is insulated from the select gate by means of the layer of insulating material and insulated from the active semiconductor region by means of a gate dielectric (20);
- the active semiconductor region is provided with a source region and a drain region (29), the select gate and the stacked gate structure being used as a mask;

characterized in that

- the layer of insulating material is applied to the select gate wall extending at least substantially transversely to the surface in a thickness which, viewed along the surface, determines the distance between the select gate and the floating gate and enables a continuous channel to be formed between the source region and the drain region.

8. A method as claimed in claim 7, characterized in that the layer of insulating material is applied to the select gate wall extending at least substantially transversely to the surface in a thickness below 70 nm.

9. A method as claimed in claim 7 or 8, characterized in that the layer of insulating material is applied to the select gate wall extending at least substantially transversely to the surface in a thickness ranging between 30 and 50 nm.

10. A method as claimed in any one of the claims 7 through 9, characterized in that prior to the provision of the stacked gate structure, the semiconductor body is subjected

to a thermal oxidation treatment, in the course of which the select gate is provided with the layer of insulating material and the active semiconductor region is provided with the gate dielectric in order to insulate the stacked gate structure from the active semiconductor region.

11. A method as claimed in any one of the claims 7 through 10, characterized in that the select gate is formed by providing a stack of a conductive layer provided with an insulating layer, which stack is patterned so as to form the select gate in the conductive layer.

12. A method as claimed in claim 11, characterized in that the insulating layer, which is applied to the conductive layer, is provided in a thickness above 100 nm.

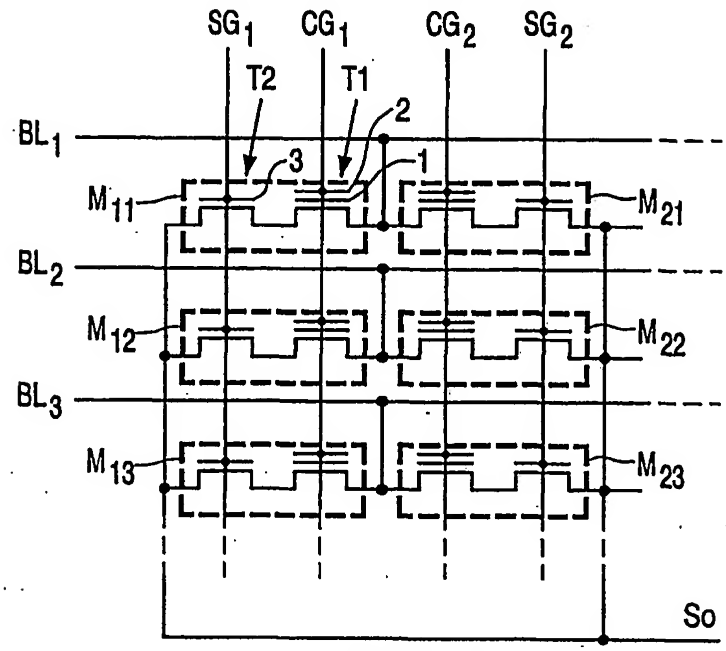


FIG. 1

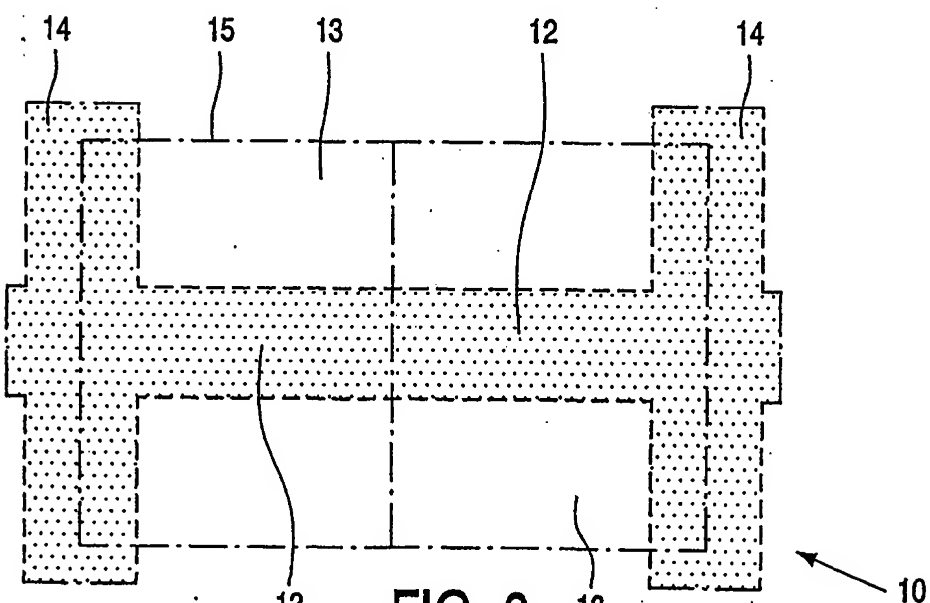


FIG. 2

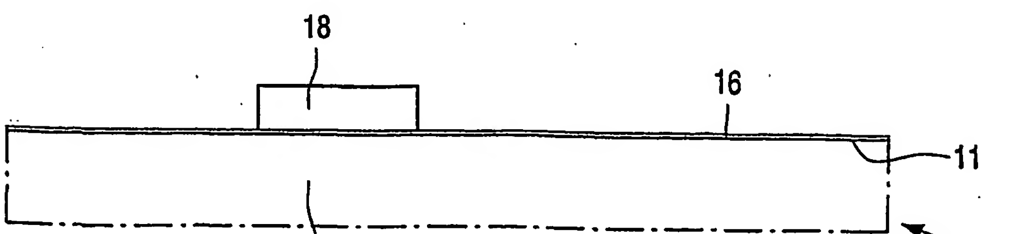


FIG. 3

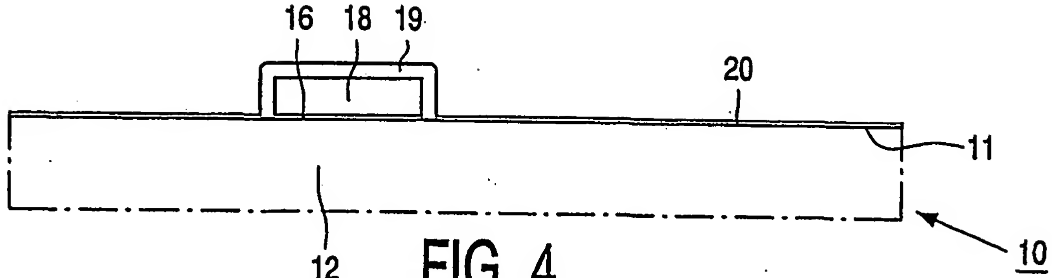


FIG. 4

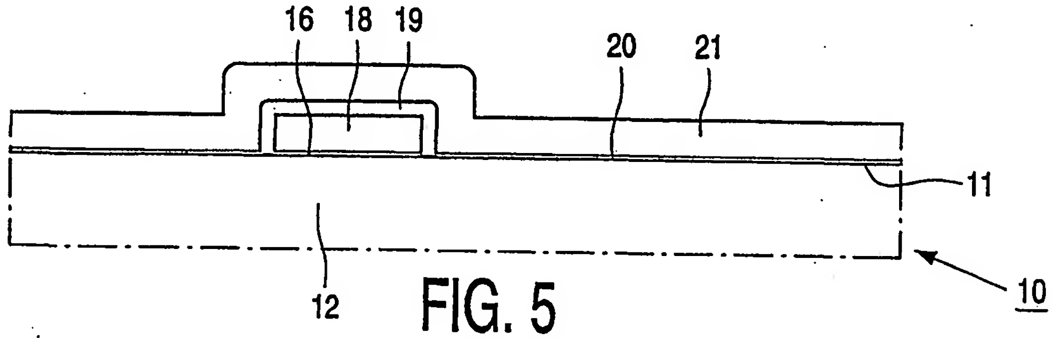


FIG. 5

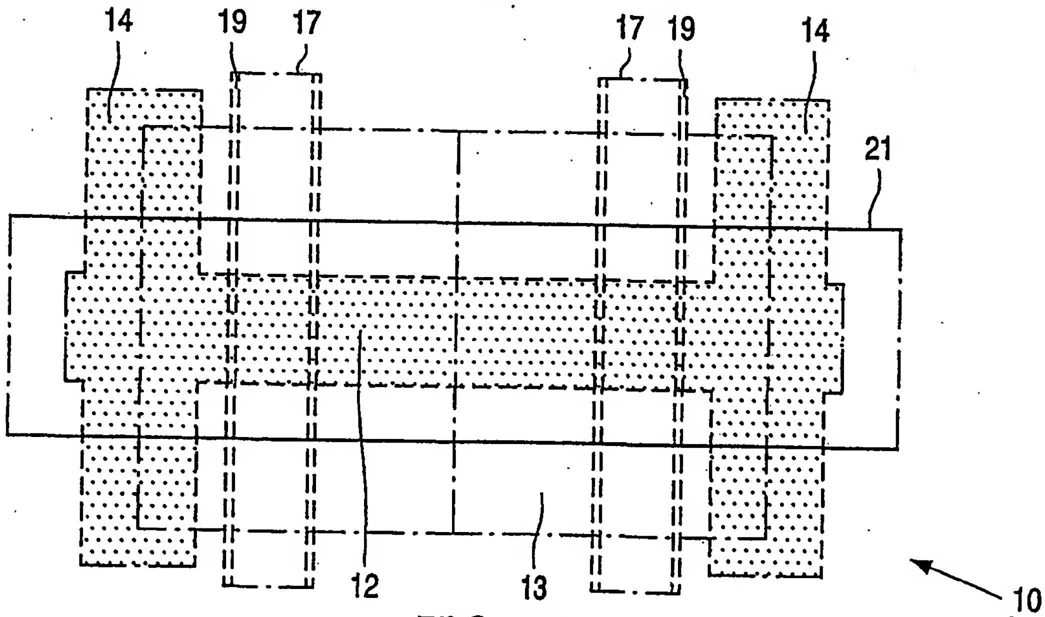


FIG. 6

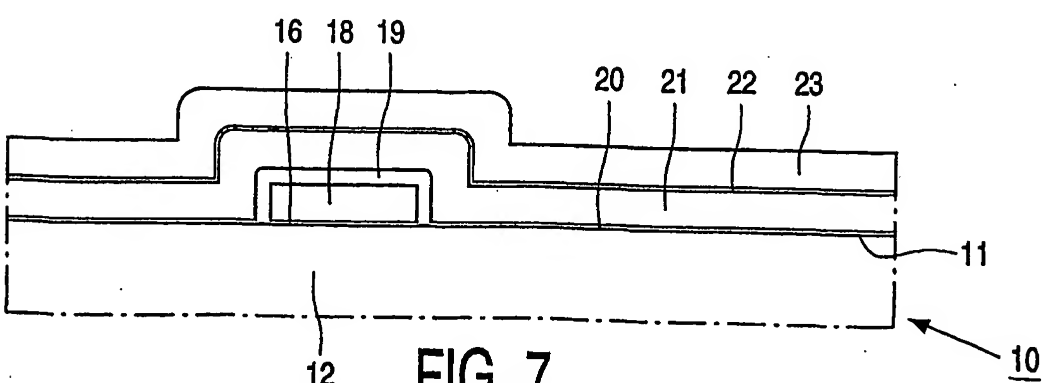


FIG. 7

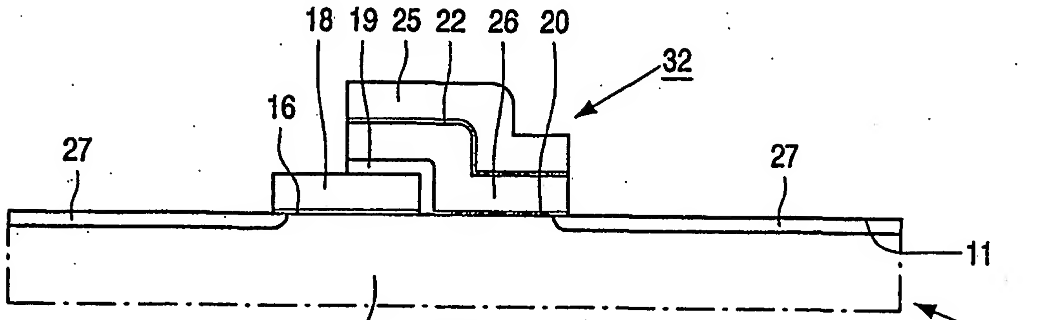


FIG. 8

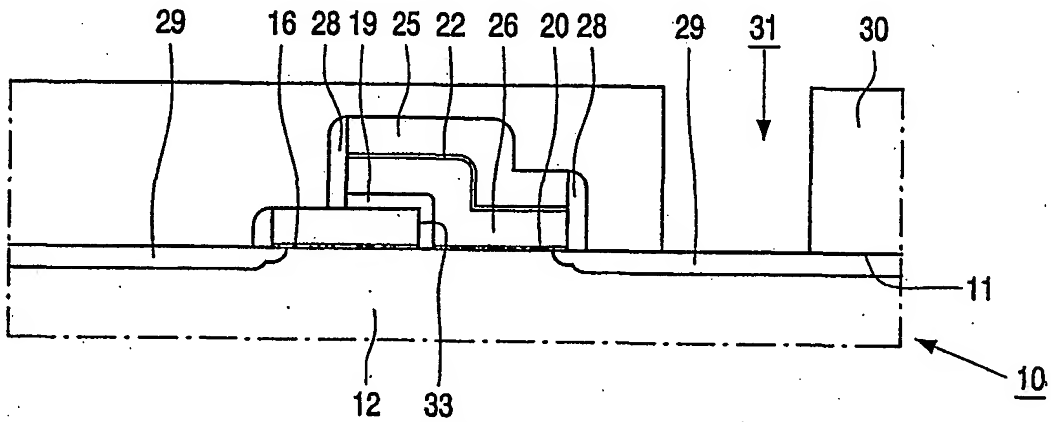


FIG. 9

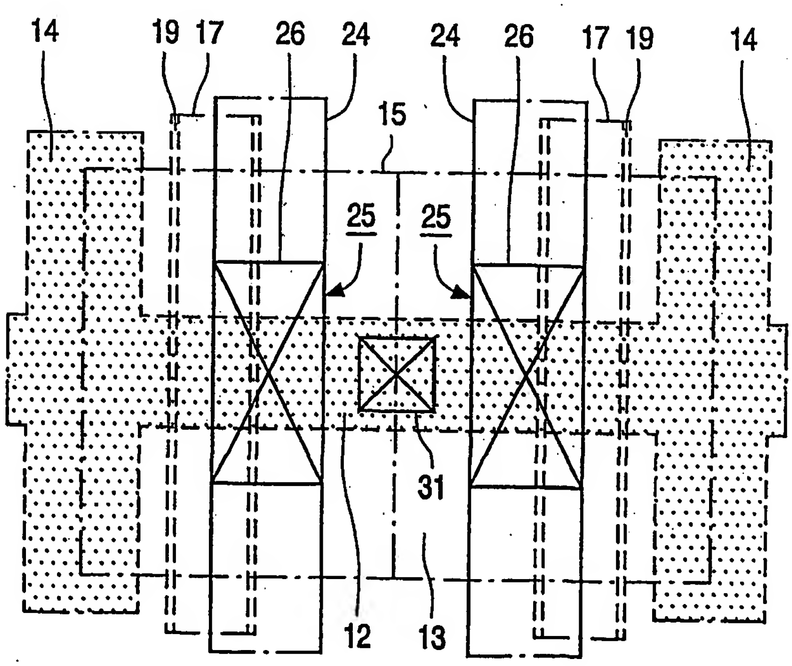


FIG. 10

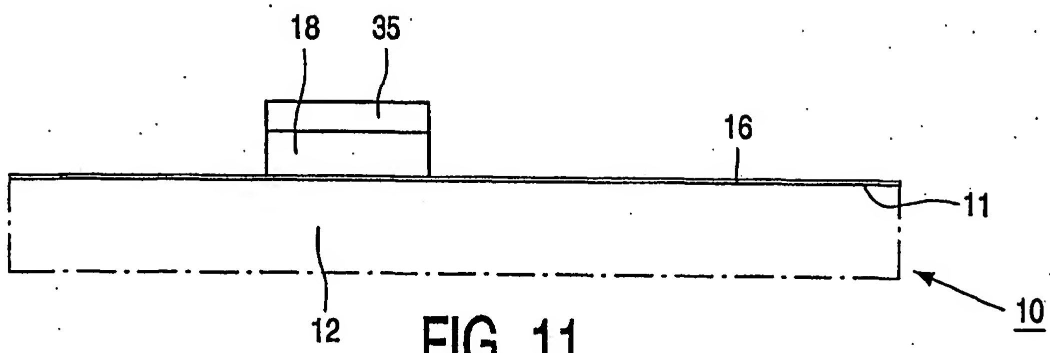


FIG. 11

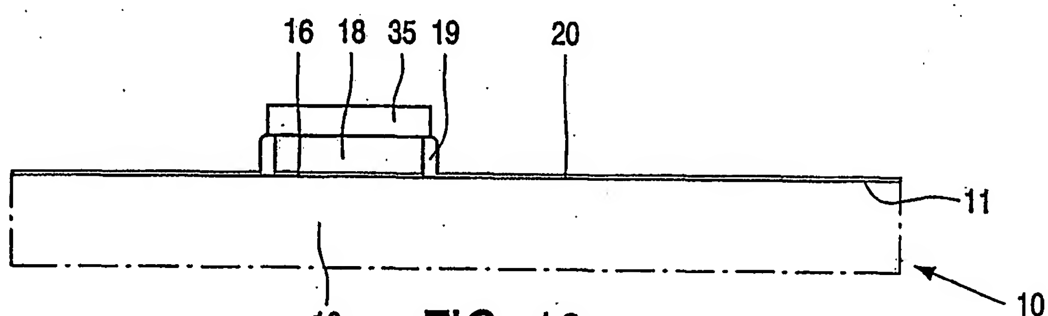


FIG. 12

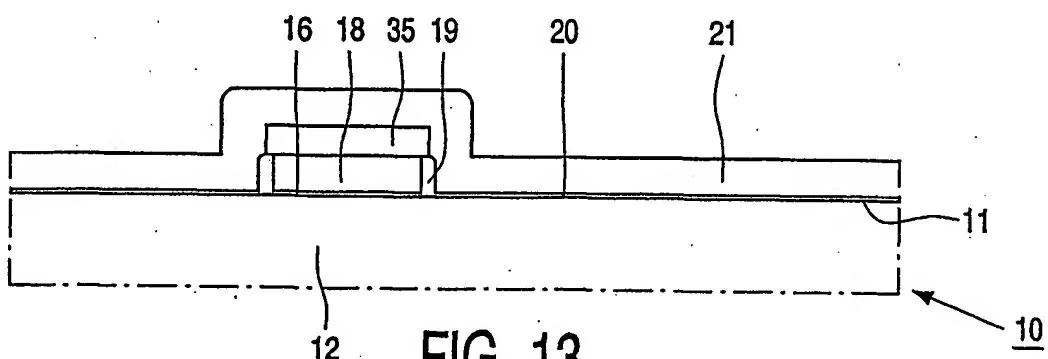


FIG. 13

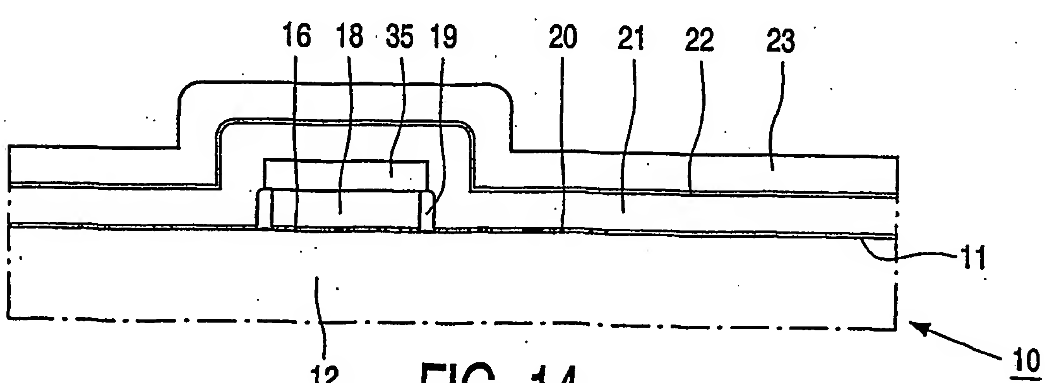


FIG. 14

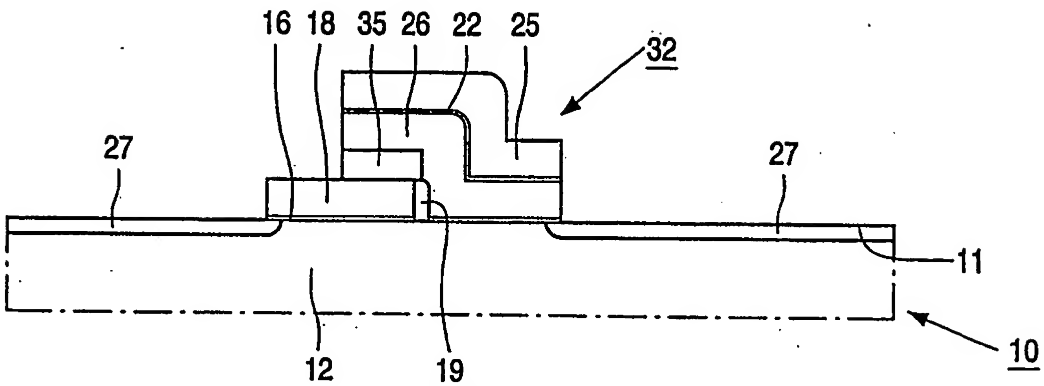

16
18
35
26
22
25
32
27
27
11
12
19
10

FIG. 15

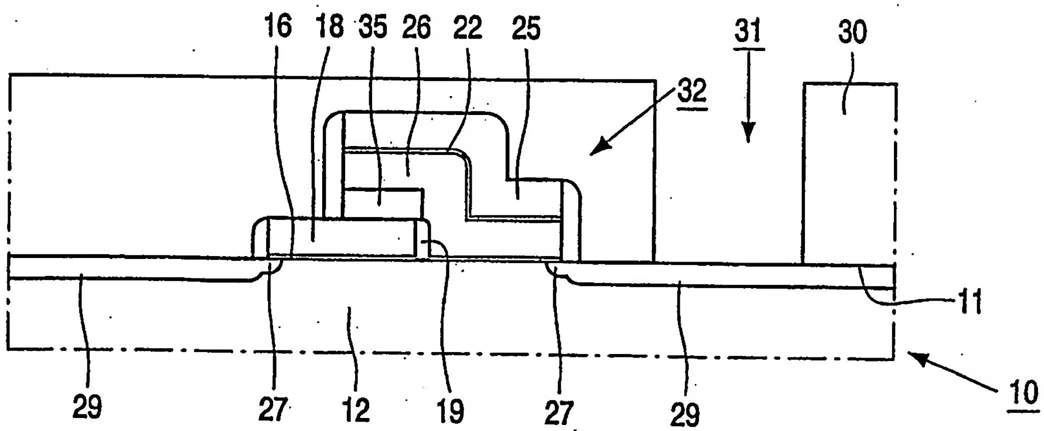

16
18
35
26
22
25
31
30
32
11
29
27
12
19
27
29
10

FIG. 16

INTERNATIONAL SEARCH REPORT

Int nal Application No
PCT/IB 02/01320

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/28 H01L27/115 H01L29/788

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 668 757 A (JENG CHING-SHI) 16 September 1997 (1997-09-16)	1-3,5-12
A	the whole document	4

X	US 5 793 079 A (MIHNEA ANDREI ET AL) 11 August 1998 (1998-08-11) the whole document	1-12

X	US 6 040 216 A (SUNG KUO-TUNG) 21 March 2000 (2000-03-21)	1-3,5-12
A	the whole document	4

X	PATENT ABSTRACTS OF JAPAN vol. 016, no. 230 (E-1208), 27 May 1992 (1992-05-27) -& JP 04 044365 A (MITSUBISHI ELECTRIC CORP), 14 February 1992 (1992-02-14)	1,5
A	abstract	2-4,6,7

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 July 2002	13/08/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Albrecht, C

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 550 073 A (HONG GARY) 27 August 1996 (1996-08-27) cited in the application column 2, line 20 -column 3, line 33; figures 2A-2I ----	1-12

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/IB 02/01320

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5668757	A	16-09-1997	US	6057575 A	02-05-2000
			US	5912843 A	15-06-1999
			US	5856943 A	05-01-1999
US 5793079	A	11-08-1998	NONE		
US 6040216	A	21-03-2000	NONE		
JP 04044365	A	14-02-1992	NONE		
US 5550073	A	27-08-1996	NONE		

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
31 October 2002 (31.10.2002)

PCT

(10) International Publication Number
WO 02/086954 A1

(51) International Patent Classification[7]: H01L 21/268

(21) International Application Number: PCT/US01/12799

(22) International Filing Date: 19 April 2001 (19.04.2001)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicants *(for all designated States except US)*: **THE TRUSTEE OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK** [US/US]; 116th Street and Broadway, New York, NY 10112 (US). **NVIK CORPORATION** [US/US]; 6 Skyline Drive, Hawthorne, NY 10532 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **SPOSILI, Robert, S.** [US/US]; Apartment 1C, 190 Claremont Avenue, New York, NY 10027 (US). **IM, James, S.** [US/US]; Apartment #74, 520 West 114th Street, New York, NY 10025 (US).

(74) Agents: **TANG, Henry et al.**; Baker Botts LLP, 30 Rockefeller Plaza, New York, NY 10112 (US).

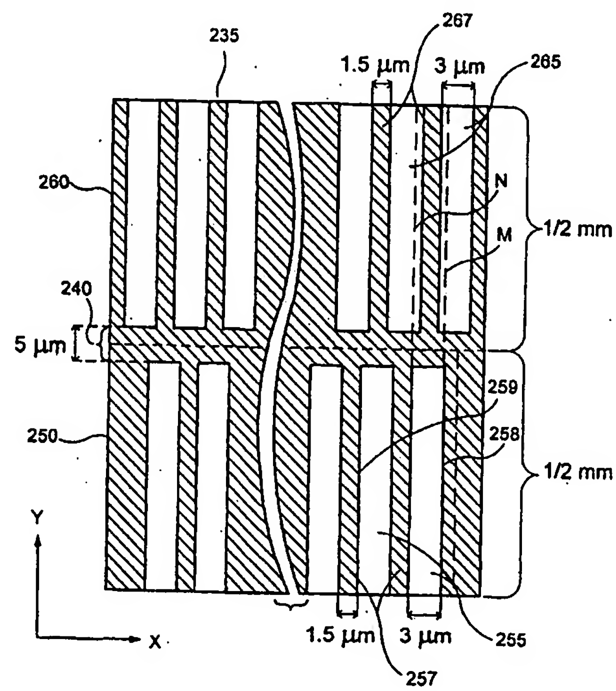
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) Title: METHOD AND SYSTEM FOR PROVIDING A SINGLE-SCAN, CONTINUOUS MOTION SEQUENTIAL LATERAL SOLIDIFICATION



(57) Abstract: A method and system for processing a silicon thin film sample on a substrate. The substrate has a surface portion that does not seed crystal growth in the silicon thin film. The film sample has a first edge and a second edge. An irradiation beam generator is controlled to emit successive irradiation beam pulses at a predetermined repetition rate. Each of the irradiation beam pulses is masked to define a first plurality of beamlets and a second plurality of beamlets, the first and second plurality of beamlets of each of the irradiation pulses being provided for impringing the film sample and having an intensity which is sufficient to melt irradiated portions of the film sample throughout their entire thickness. The film sample is continuously scanned at a constant predetermined speed, so that a successive impingement of the first and second beamlets of the irradiation pulses occurs in a scanning direction of the film sample between the first edge and the second edge. During the continuous scanning of the film sample, a plurality of first areas of the film sample are successively irradiated using the first beamlets of the irradiation beam pulses so that the first areas are melted throughout their thickness and leaving irradiated regions between respective adjacent ones of the first areas. Also during the continuous scanning, each one of the first areas irradiated using the first beamlets of each of the irradiation pulses is allowed to resolidify and crystallize. During resolidification and crystallization of the first areas, a plurality of second areas of the film sample are successively irradiated using the second beamlets of the irradiation beam pulses so that the second areas are melted throughout their thickness. Each of the second areas partially overlaps a respective pair of the resolidified

WO 02/086954 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

METHOD FOR SINGLE-SCAN, CONTINUOUS MOTION SEQUENTIAL LATERAL SOLIDIFICATION

SPECIFICATION

FIELD OF THE INVENTION

The present invention relates to a method and system for processing a thin-film semiconductor material, and more particularly to forming large-grained, grain-shaped and grain-boundary-location controlled semiconductor thin films from amorphous or polycrystalline thin films on a substrate using laser irradiation and a continuous motion of the substrate having the semiconductor film being irradiated.

BACKGROUND INFORMATION

In the field of semiconductor processing, there have been several attempts to use lasers to convert thin amorphous silicon films into polycrystalline films. For example, in James Im et al., "Crystalline Si Films for Integrated Active-Matrix Liquid-Crystal Displays," 11 MRS Bulletin 39 (1996), an overview of conventional excimer laser annealing technology is described. In such conventional system, an excimer laser beam is shaped into a beam having an elongated cross-section which is typically up to 30 cm long and 500 micrometers or greater in width. The shaped beam is stepped over a sample of amorphous silicon (i.e., by translating the sample) to facilitate melting thereof and to effectuate the formation of grain-shape and grain boundary-controlled polycrystalline silicon upon the re-solidification of the sample.

The use of conventional laser annealing technology to generate polycrystalline silicon is problematic for several reasons. First, the polycrystalline silicon generated in the process is typically small grained, of a random micro structure (i.e., poor control of grain shapes and grain boundary locations), and having a nonuniform grain size, therefore resulting in poor and nonuniform devices and accordingly, low manufacturing yield. Second, in order to obtain acceptable quality grain-shape and grain-boundary-location controlled polycrystalline thin films, the manufacturing throughput

for producing such thin films must be kept low. Also, the process generally requires a controlled atmosphere and preheating of the amorphous silicon sample, which leads to a reduction in throughput rates. Accordingly, there exists a need in the field for a method and system for growing amorphous or polycrystalline thin semiconductor films to produce higher quality thin polycrystalline or single crystalline semiconductor silicon films at greater throughput rates. There likewise exists a need for manufacturing techniques which generate larger and more uniformly microstructured polycrystalline silicon thin films to be used in the fabrication of higher quality devices, such as thin film transistor arrays for liquid crystal panel displays.

SUMMARY OF THE INVENTION

An object of the present invention is to provide techniques for producing large-grained and grain-shape and grain-boundary, location controlled polycrystalline thin film semiconductors using a sequential lateral solidification ("SLS") process, and to generate such silicon thin films in an accelerated manner. Another object of the present invention is to effectuate such accelerated sequential lateral solidification of the polycrystalline thin film semiconductors provided on a simple and continuous motion translation of the semiconductor film, without the necessity of "microtranslating" the thin film, and re-irradiating the previously irradiated region in the direction which is the same as the direction of the initial irradiation of the thin film while the sample is being continuously translated.

At least some of these objects are accomplished with a method and system for processing a semiconductor thin film sample on a substrate. The substrate has a surface portion that does not seed crystal growth in the silicon thin film. The film sample has a first edge and a second edge. An irradiation beam generator is controlled to emit successive irradiation beam pulses at a predetermined repetition rate. Each of the irradiation beam pulses is masked to define a first plurality of beamlets and a second plurality of beamlets, the first and second plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to melt irradiated portions of the film sample throughout their entire thickness. The film sample is continuously scanned, at a constant predetermined speed, so that a

successive impingement of the first and second beamlets of the irradiation beam pulses occurs in a scanning direction on the film sample between the first edge and the second edge. During the continuous scanning of the film sample, a plurality of first areas of the film sample are successively irradiated using the first beamlets of the irradiation beam pulses so that the first areas are melted throughout their thickness and leaving unirradiated regions between respective adjacent ones of the first areas. Also during the continuous scanning, each one of the first areas irradiated using the first beamlets of each of the irradiation beam pulses is allowed to re-solidify and crystalize. During resolidification and crystallization of the first areas, a plurality of second areas of the film sample are successively irradiated using the second beamlets of the irradiation beam pulses so that the second areas are melted throughout their thickness. Each of the second areas partially overlaps a respective pair of the re-solidified and crystalized first areas and the respective unirradiated region therebetween.

In another embodiment of the present invention, during the successive irradiation of the second areas by the second beamlets, third areas of the film sample are successively irradiated by the first beamlets to completely melt the third areas throughout their thickness, each of the third areas partially overlapping a respective one of the re-solidified and crystalized first areas and leaving further unirradiated regions between respective adjacent ones of the third areas. One of the first areas and one of the third areas may lie on a first line which is parallel to the scanning direction, and one of the second areas may lie of a second line which is parallel to the scanning direction. The first line preferably extends at an offset from the second line. Upon the successive irradiation of the third areas by the first beamlets, each one of the second areas irradiated by the first beamlets of each of the irradiation beam pulses can be allowed to re-solidify and crystalize.

According to another embodiment of the present invention, when the film sample is continuously scanned, each one of the third areas irradiated by the first beamlets of each of the irradiation beam pulses is allowed to re-solidify and crystalize. After the irradiation of the second and third areas, a plurality of fourth areas of the film sample are successively irradiated by the second beamlets of the irradiation beam pulses so that the fourth areas are melted throughout their thickness, wherein each one of the

fourth areas partially overlaps a respective pair of the re-solidified and crystalized third areas and the respective further unirradiated region therebetween.

In yet another embodiment of the present invention, the first edge is located on a side of the film sample which is opposite from a side of the film sample on which the second edge is located. In addition, the first and second impingements along the film sample is continued until the first impingement by the first set of patterned beamlets of the film sample and the second impingement by the second set of patterned beamlets of the film sample passes the second edge of the film sample. Thereafter, the film sample can be positioned so that the first and second sets of patterned beamlets impinge on at a first location outside of boundaries of the film sample with respect to the film sample, and then the film sample may be translated so that impingement of the first and second sets of patterned beamlets moves from the first location to a second location, the second location being outside of the boundaries of the film sample. Finally, the film sample can be maintained so that the patterned beamlets impinge on the second location until any vibration of the film sample is damped out. With this embodiment, a completed portion of the film sample having a predetermined width has preferably been irradiated and re-solidified, the film sample having a controlled crystalline grain growth in the entire completed portion.

In still another embodiment, the particular direction extends along a first path, the film sample is translated along a second path which is perpendicular to the first path. The successive impingement by the first and second beamlets of the irradiation beam pulses the film sample may pass the second edge of the film sample. After, the successive irradiation of the first and second areas, the film sample is positioned so that the first and second beamlets of the irradiation beam pulses impinge on at a first location outside of boundaries of the film sample with respect to the film sample. Thereafter, the film sample can be positioned so that the successive impingement of the first and second beamlets with respect to the film sample moves from the first location to a second location, the second location being outside of the boundaries of the film sample. A completed portion of the film sample having a predetermined width which has been irradiated, melted throughout its entire thickness and re-solidified can be defined, with the film sample having a controlled crystalline grain growth in the entire completed

portion. The particular direction may extend along a first path, and the film sample may be translated along a second path, the first axis being perpendicular to the first path. The second location can be provided at the distance from the first location approximately equal to the predetermined width.

According to another embodiment of the present invention, the film sample can be continuously scanned, at the constant predetermined speed, so that the successive impingement of the first and second beamlets of the irradiation beam pulses occurs in a further direction on the film sample between the second edge and the first edge, the further direction being opposite to the scanning direction. At that time, a plurality of fifth areas of the film sample can be successively irradiated with the second beamlets of the irradiation beam pulses so that the fifth areas are melted throughout their thickness and leaving additional unirradiated regions between respective adjacent ones of the fifth areas. Also, each one of the fifth areas irradiated by the second beamlets of each of the irradiation beam pulses can be allowed to re-solidify and crystalize. Furthermore, a plurality of sixth areas of the film sample can be successively irradiated by the first beamlets of the irradiation beam pulses so that the sixth areas are melted throughout their thickness, with each one of the sixth areas partially overlapping a respective pair of the re-solidified and crystalized fifth areas and the respective unirradiated region therebetween.

In still another embodiment, portions of the irradiation beam pulses can be masked to emit successive partial intensity irradiation pulse which have a reduced intensity so that when the successive partial intensity irradiation pulses irradiate a particular region of the film sample, the particular region is melted for less than the entire thickness of the film sample. Then, each of the re-solidified and crystalized second areas can be successively irradiated by the respective one of the successive partial intensity irradiation pulses.

In a further embodiment of the present invention, a method and system for processing a semiconductor thin film sample on a substrate is provided. The substrate has a surface portion that does not seed crystal growth in the semiconductor thin film. The film sample has a first edge and a second edge. An irradiation beam generator is controlled to emit successive irradiation beam pulses at a predetermined repetition rate.

Each of the irradiation beam pulses is masked to define a first plurality of beamlets and a second plurality of beamlets, the first and second plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to melt irradiated portions of the film sample throughout their entire thickness. The film sample is continuously scanned, at a constant predetermined speed, so that a successive impingement of the first and second beamlets of the irradiation beam pulses occurs in a scanning direction on the film sample between the first edge and the second edge. During the continuous scanning of the film sample, a plurality of first areas of the film sample are successively irradiated using the first beamlets of the irradiation beam pulses so that the first areas are melted throughout their thickness and leaving unirradiated regions adjacent to the first areas. Each of the first areas has a first border with a first width, the border extending along a first line which is perpendicular to the scanning direction. Also during the continuous scanning, each one of the first areas irradiated using the first beamlets of each of the irradiation beam pulses is allowed to re-solidify and crystalize. Following the resolidification and crystallization of the first areas, a plurality of second areas of the film sample are successively irradiated using the second beamlets of the irradiation beam pulses so that the second areas are melted throughout their thickness. A first region of each one of the second areas completely overlaps at least one of the re-solidified and crystalized first areas, and a second region of the respective one of the second areas overlaps the respective unirradiated region provided adjacent to the re-solidified and crystalized first area. The first region has a second border with a second width which is greater than half of the first width, the second border extending along a second line which is parallel to and offset from the first line.

BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments of the present invention will now be described in further detail with reference to the accompanying drawings in which:

Figure 1 shows a diagram of an exemplary embodiment of a system for performing a single-scan, continuous motion sequential lateral solidification ("SLS")

according to the present invention which does not require a microtranslation of a sample for an effective large grain growth in a silicon thin film;

Figure 2 shows an enlarged view of an exemplary embodiment of the sample conceptually subdivided and having the silicon thin film thereon;

Figure 3 shows an enlarged illustration of an intensity pattern of an irradiation beam pulse as defined by a first exemplary embodiment of a mask utilized by the system and method of the present invention which facilitates the single-scan, continuous motion SLS as it impinges the silicon thin film on a substrate;

Figure 4 shows an exemplary irradiation path of beam pulses impinging the sample, as the sample is translated by the system of Figure 1, using a first exemplary embodiment of the method according to the present invention which provides the single-scan, continuous motion SLS;

Figures 5A-5G show the radiation beam pulse intensity pattern and portions of grain structures on an exemplary first conceptual column of the sample having the silicon thin film thereon at various sequential stages of the SLS processing according to the first exemplary embodiment of the method of the present invention illustrated in Figure 4, in which the intensity pattern of the irradiation beam pulse of Figure 3 is used to irradiate a first conceptual column of the sample;

Figures 6A and 6B show the radiation beam pulse intensity pattern and portions of the grain structures on an exemplary second conceptual column of the sample having the silicon thin film thereon at two sequential stages of SLS processing according to the first exemplary embodiment of the method of the present invention illustrated in Figure 4, which is performed along a second conceptual column of the sample, after the silicon thin film of the entire first conceptual column of the sample illustrated in Figures 5A-5G is completely melted, re-solidified and crystalized;

Figure 7 shows an illustrative diagram of the crystallized silicon film of the sample after the silicon thin film in all conceptual columns of the sample is completely melted, re-solidified and crystalized;

Figure 8 shows an enlarged illustration of a second exemplary embodiment of an intensity pattern of the irradiation beam pulse as defined by a further mask utilized by the system and method of the present invention as it impinges the

silicon thin film on the substrate, which promotes a growth of larger grains in the silicon thin film;

Figure 9 shows the radiation beam pulse intensity pattern and the grain structure of a portion of an exemplary first conceptual column of the sample having the silicon thin film thereon at an exemplary stage of the SLS processing according to a second exemplary embodiment of the method of the present invention which utilizes the mask illustrated in Figure 8 for growing longer grains in the silicon thin film;

Figure 10 shows an illustrative diagram of a further progression of the SLS processing of Figure 9 for the silicon thin film of the sample after the beam pulses complete the irradiation of a particular portion of the first conceptual column of the sample, which then crystallizes;

Figure 11 shows an enlarged illustration of a third exemplary embodiment of an intensity pattern of the irradiation beam pulse as defined by another mask utilized by the system and method of the present invention as it impinges the silicon thin film of the sample, which includes a single lower-energy portion provided adjacent to one section of slit-shaped beamlets of the irradiation beam pulse;

Figure 12 shows an enlarged illustration a fourth exemplary embodiment of an intensity pattern of the irradiation beam pulse as defined by yet another mask utilized by the system and method of the present invention as it impinges the silicon thin film of the sample, which includes two lower-energy portions, each provided opposite to one another and adjacent to a respective different section of slit-shaped beamlets of the irradiation beam pulse;

Figures 13A-13D show the radiation beam pulse intensity pattern and the grain structure of a portion of an exemplary conceptual first column of the silicon thin film provided on the sample at various sequential stages of SLS processing according to a third exemplary embodiment of the method of the present invention, which uses the technique of the first embodiment of the method illustrated in Figures 5A-5G, after the sample is rotated 90° in a clock-wise direction;

Figure 14 shows an illustrative diagram of the crystallized silicon film of the sample after the silicon thin film in all conceptual columns of the rotated sample have

been completely melted, re-solidified and crystalized using the technique illustrated in Figures 13A-13D; and

Figure 15 shows a flow diagram illustrating the steps implemented by the system of Figure 1 and the method illustrated in Figures 5A-5G and 6A-6B according to one exemplary embodiment of the present invention.

DETAILED DESCRIPTION

Certain systems and methods for providing a continuous motion SLS are described in U.S. Patent Application Serial No. 09/526,585 (the " '585 application"), the entire disclosure of which is incorporated herein by reference. The '585 application explicitly describes and illustrates the details of these systems and methods, and their utilization of microtranslations of a sample, which has an amorphous silicon thin film provided thereon being irradiated by irradiation beam pulses to promote the sequential lateral solidification on the thin film. Similar to the system described in the '585 application, an exemplary embodiment of a system for carrying out the continuous motion SLS processing of amorphous silicon thin films according to the present invention is illustrated in Figure 1. The exemplary system includes a Lambda Physik model LPX-315I XeCl pulsed excimer laser 110 emitting an irradiation beam (e.g., a laser beam), a controllable beam energy density modulator 120 for modifying the energy density of the laser beam, a MicroLas two plate variable attenuator 130, beam steering mirrors 140, 143, 147, 160 and 162, beam expanding and collimating lenses 141 and 142, a beam homogenizer 144, a condenser lens 145, a field lens 148, a projection mask 150 which may be mounted in a translating stage (not shown), a 4×-6× eye piece 161, a controllable shutter 152, a multi-element objective lens 163 for focusing an incident radiation beam pulse 164 onto a sample 40 having a silicon thin film 52 to be SLS processed mounted on a sample translation stage 180, a granite block optical bench 190 supported on a vibration isolation and self-leveling system 191, 192, 193 and 194, and a computer 106 (e.g., a general purpose computer executing a program or a special-purpose computer) coupled to control the pulsed excimer laser 110, the beam energy density modulator 120, the variable attenuator 130, the shutter 152 and the sample translation stage 180.

The sample translation stage 180 is controlled by the computer 106 to effectuate translations of the sample 40 in the planar X-Y directions and the Z direction. In this manner, the computer 106 controls the relative position of the sample 40 with respect to the irradiation beam pulse 164. The repetition and the energy density of the irradiation beam pulse 164 are also controlled by the computer 106. It should be understood by those skilled in the art that instead of the pulsed excimer laser 110, the irradiation beam pulse can be generated by another known source of short energy pulses suitable for melting a semiconductor (or silicon) thin film 52 in the manner described herein below. Such known source can be a pulsed solid state laser, a chopped continuous wave laser, a pulsed electron beam and a pulsed ion beam, etc. with appropriate modifications to the radiation beam path from the source 110 to the sample 40. While the computer 106, in the exemplary embodiment of the system shown in Figure 1, controls translations of the sample 40 for carrying out the single-scan, continuous motion SLS processing of the silicon thin film 52 according to the present invention, the computer 106 may also be adapted to control the translations of the mask 150 and/or the excimer laser 110 mounted in an appropriate mask/laser beam translation stage (not shown for the simplicity of the depiction) to shift the intensity pattern of the irradiation beam pulses 164, with respect to the silicon thin film 52, along a controlled beam path. Another possible way to shift the intensity pattern of the irradiation beam pulse is to have the computer 106 control a beam steering mirror. The exemplary system of Figure 1 may be used to carry out the single-scan, continuous motion SLS processing of the silicon thin film 52 on the sample 40 in the manner described below in further detail.

As described in further detail in the '585 application, an amorphous silicon thin film sample is processed into a single or polycrystalline silicon thin film by generating a plurality of excimer laser pulses of a predetermined fluence, controllably modulating the fluence of the excimer laser pulses, homogenizing the intensity profile of the laser pulse plane, masking each homogenized laser pulses to define beamlets, irradiating the amorphous silicon thin film sample with the beamlets to effect melting of portions thereof that were irradiated by the beamlets, and controllably and continuously translating the sample with respect to the patterned beamlets. The output of the beamlets, as provided in the '585 application, is controllably modulated to thereby process the

amorphous silicon thin film provided on the sample into a single or grain-shape, grain-boundary-location controlled polycrystalline silicon thin film by the continuous motion sequential translation of the sample relative to the beamlets, and the irradiation of the sample by the beamlets of masked irradiation pulses of varying fluence at corresponding sequential locations thereon. One of the advantageous improvements of system and method according to the present invention is that there is a significant saving of processing time to irradiate and promote the SLS on the silicon thin film of the sample by completing the irradiation of a section of the sample 40 without the requirement of any microtranslation of the sample to be performed (i.e., the microtranslations as described in the '585 application).

Figure 2 shows an enlarged view of an exemplary embodiment of the sample 40 having the amorphous silicon thin film 52 thereon. This exemplary sample 40, as shown in Figure 2, is sized 40cm in the Y-direction by 30cm in the X-direction. The sample 40 is conceptually subdivided into a number of columns (e.g., a first column 210, a second column 220, etc.). The location/size of each column is stored in a storage device of the computer 106, and utilized by the computer 106 for later controlling the translation of the sample 40. Each of the columns 210, 220, etc. is dimensioned, e.g., 2cm in the X-direction by 40cm in the Y-direction. Thus, if the sample 40 is sized 30cm in the X-direction, the sample 40 may be conceptually subdivided into fifteen (15) columns. Within the constraints of the system discussed below, the sample 40 may be subdivided into columns having different dimensions (e.g., 1cm by 40cm columns, 3cm by 40cm columns, 4cm by 40cm columns, etc.). When the sample 40 is conceptually subdivided into columns, at least a small portion of each column extending for the entire length of the column should be overlapped by the neighboring column(s), i.e., an overlapped portion 230, so as to avoid a possibility of having any unirradiated areas of the silicon thin film 52. The overlapped portions 230 are preferably provided between all neighboring columns. For example, the overlapped area may have a width of 1μm. It should be understood that other widths of the overlapped portions are possible, such as 2μm, and are within the scope of the present invention.

Figure 3 shows an enlarged illustration of a first exemplary embodiment of an intensity pattern 235 of the masked irradiation beam pulse 164 which is defined by

the mask 150 as it impinges the silicon thin film 52 provided on the sample 40. The intensity pattern 235 is produced by placing the mask 150, which has a particular pattern of the transparent and opaque regions, in the path of the homogenized irradiation beam 149, and the resultant beamlets exiting the mask 150 are focused by the objective lens 163 to produce the masked irradiation beam pulse 164 having the desired intensity pattern 235. Using such intensity pattern 235, the system and method of the present invention can effectuate the single-scan, continuous motion SLS of the silicon thin film 52. The first exemplary intensity profile 235 shown in this drawing includes two beamlet sections 250, 260, with the slit-shaped beamlets in each section being separated from one another in a predetermined manner. The location of the slit-shaped beamlets 255 of the first section 250 are provided at an offset in the X-direction with respect to the location of the slit-shaped beamlets 265 of the second section 260. A detailed discussion of the exemplary intensity pattern 235 shown in Figure 3 is provided below.

As described above, the intensity pattern 235 includes two sections, i.e., a first beamlet section 250 and a second beamlet section 260. The first beamlet section 250 has first slit-shaped beamlets 255, each having a width of approximately 3μm in the X-direction and a length of approximately ½mm in the Y-direction. The first slit-shaped beamlets 255 are equidistantly spaced from one another by first shadow regions 257 (i.e., the first slit-shaped beamlets 255 are spaced apart from one another by these first shadow regions 257). The first shadow regions 257 may have a width of, e.g., 1½μm.

As shown in Figure 3, the second beamlet section 260 is located substantially adjacent to the first beamlet section 250 in the Y-direction, and has second slit-shaped beamlets 265. The second beamlet section 260 includes second shadow regions 267 separating the second slit-shaped beamlets 265 from one another. The second slit-shaped beamlets 265 and the second shadow regions 267 are separated from the first slit-shaped beamlets 255 and the first shadow regions 257 by an intervening shadow region 240. The dimensions of the second slit-shaped beamlets 265 and the second shadow regions 267 are substantially similar to those of the first slit-shaped beamlets 255 and the first shadow regions 257, respectively. It is preferable for an edge 258 of each one of the first slit-shaped beamlets 255, which extends in the Y-direction, to coincide with a line M which extends into the area of a respective one second slit-

shaped beamlet 265, and for the other edge 259 of each first slit-shaped beamlet 255 to coincide with a line N which extends into the area of the second slit-shaped beamlets 265 adjacent to the one of the second slit-shaped beamlets having the line M extending therethrough. The first beamlet section 250 is separated from the second beamlet section 260 by an intervening shadow region 240 having a width of 5μm. It should be noted that the masked irradiation beam pulse 164 does not project any beam energy into the shadow regions 257, 267, 240, while providing the full laser pulse intensity of the beamlets onto the silicon thin film 52.

Therefore, the dimension of the intensity pattern 235 in the Y-direction should be approximately 1.005 mm after adding the length of the first slit-shaped beamlets 255 (½mm) and those of the second slit-shaped beamlets 265 (½mm), plus 5μm to account for the intervening shadow region 240. The dimension of the intensity pattern 235 in the X-direction should be equal to the width of the conceptual columns 210, 220. Therefore, the approximate dimension of the exemplary intensity pattern 235 shown in Figure 3 is 2cm in the X-direction by approximately 1.005 mm in the Y-direction. In addition, the cross-section of the homogenized irradiation beam 149 should be at least large enough to cover the portion of the mask 150 that defines the intensity pattern 235. The array of beamlets 151 exiting the mask 150 and then focused by the objective lens 163 results in the masked irradiation beam pulse 164 having dimensions in the X-direction that substantially matches the width of each of the conceptual columns 210, 220 of the sample 40. It is preferable for the width the cross-sections of the masked irradiation beam pulse 164 (and thus of the intensity pattern 235) in the X-direction to be slightly greater than the width of each of the conceptual columns 210, 220. The advantages of such dimensions will be understood from the further description of the first embodiment of the method according to the present invention as discussed in greater detail below.

It should be understood that the width of the first and second slit-shaped beamlets 255, 265 may depend on a number of factors, e.g., the energy density of the incident laser pulse, the duration of the incident irradiation beam pulse, the thickness of the silicon thin film 52 provided on the sample 40, the temperature and thermal conductivity of the substrate, etc. While it is desirable from the standpoint of processing

efficiency to utilize the slit-shaped beamlets 255, 265 which have a larger width in the X-direction so as to cover a greater width of the sample 40, it is important to select the width of the first and second slit-shaped beamlets 255, 265 such that when portions of the silicon thin film 52 provided on the sample 40 are irradiated thereby and are completely melted throughout their thickness, no nucleation occurs within such melted portions when they re-solidify and crystalize. In particular, if the width of the slit-shaped beamlets 255, 265 is too large, certain areas within the fully-melted portions may re-solidify before the controlled lateral grain growth reaches these areas. If this occurs, the control of the grain growth in the irradiated areas will be compromised.

Other dimension and shapes of the first slit-shaped beamlets 255, the first shadow regions 257, the second slit-shaped beamlets 265, the second shadow regions 267 and/or the shadow region 240 are contemplated, and are within the scope of the present invention. For example, if the extension or length of each of the first and second slit-shaped beamlets 255, 265 is approximately 1mm (i.e., instead of ½mm), the dimension of the intensity pattern 235 of the masked irradiation beam pulse 164 in the Y-direction would be 2mm.

One of the important aspects of the intensity pattern 235 according to the present invention is that if the sample 40 is translated such that portions of the silicon thin film areas previously irradiated by the first beamlet section 250 (as well as re-solidified and crystalized) are irradiated by the second beamlet section 260, each of the slit-shaped second beamlets partially overlap a respective pair of regions previously irradiated by the first slit-shaped beamlets 255 of the first beamlet section 250, as well as overlapping the unirradiated region (i.e., the region overlapped by a respective shadow region 257) therebetween. This is because when the sample 40 is translated in the Y-direction by the sample translation stage 180, the second slit-shaped beamlets 265 of the masked irradiation beam pulse 164 should completely melt a portion of the silicon thin 52 film which was previously melted (by the first slit-shaped beamlets 255 of the masked irradiation beam pulse 164), cooled, re-solidified and crystallized. Such preferable technique according to the present invention promotes the lateral, controlled grain growth in the cooling regions of the silicon thin film 52 to extend such grain growth from the area that was completely melted by the first slit-shaped beamlets 255, cooled and re-

solidified (and not later re-melted) into the area that was previously solidified and re-melted, and to further extend lateral crystal into the newly melted area (that is adjacent to the originally-melted area). The details of this technique and method according to the preferred embodiment of the present invention is described in further detail below.

For the exemplary sample 40 shown in Figure 2 and described above, and for the purposes of the foregoing, the intensity pattern 235 of the masked irradiation beam pulse 164 may be defined as 2cm in the X-direction by ½cm in the Y-direction (e.g., a rectangular shape). However, as described above, the intensity pattern 235 of the masked irradiation beam pulse 164 is not limited to any particular shape or size. Indeed, other shapes and/or sizes of the intensity pattern 235 may be used, as would be apparent to those having ordinary skill in the art based on the teachings provided herein (e.g., square shape, circle, etc.). It should be understood that if a different the intensity pattern of the masked irradiation beam pulse 164 is desired, the mask 150, and possibly of the homogenized irradiation beam 149 would have to be modified to define the intensity pattern 235 after focusing by the objective lens 163.

The cross-section of the masked irradiated beam pulse 164 (i.e., the beam pulse area (B_A)) can be determined as follows:

$$B_A \approx \frac{E_{PULSE} \times K_{OPTICS}}{ED_{PROCESS}} \tag{1}$$

where E_{PULSE} is the energy per pulse of the laser or pulsed irradiation beam, K_{OPTICS} is the fraction of the irradiation beam energy passing through the optics of the system, and $ED_{PROCESS}$ is the energy density of the process (e.g., 500 mJ/cm^2 for 500Å silicon thin film and 30 nseconds pulse duration). It is preferably to determine $ED_{PROCESS}$ experimentally.

Referring now to Figures 4, 5A-5G and 6A-6B to describe the details of the first exemplary embodiment of the method according to the present invention, Figure 4 shows an exemplary irradiation path of beam pulses impinging portions of the silicon thin film 52 provided on the sample 40 as the sample 40 is translated under the control of the computer 106 by the sample translation stage 180 of Figure 1. In this drawing, a first exemplary embodiment of a method which effectuates the single-scan, continuous motion SLS according to the present invention, is utilized. Figures 5A-5G show the

intensity pattern of the radiation beam pulse 164 and the grain structure on an exemplary first conceptual column 210 of a silicon thin film on the sample 40 at various sequential stages of continuous motion SLS processing according to the first exemplary embodiment of the method of the present invention, which is discussed below with reference to Figure 4. In this part of the method, the masked radiation beam pulses164 have an intensity pattern defined by the mask 150 to provide the intensity pattern 235 which is illustrated in Figure 3. Figures 6A-6B show the masked radiation beam pulse intensity pattern and portions of the grain structures in an exemplary second conceptual column 220 of the sample 40 having the silicon thin film 52 thereon at two sequential stages of SLS processing according to the first exemplary embodiment of the method of the present invention illustrated in Figure 4. This part of the method is performed after the silicon thin film 52 of the entire conceptual first column 210 of the sample 40 illustrated in Figures 5A-5G is completely melted, cooled, re-solidified and crystalized.

Turning first to Figure 4, the sample 40 is placed on the sample translation stage 180, which is controlled by the computer 106. The sample 40 is placed such that the fixed position masked irradiation beam pulse 164 (having the intensity pattern 235 defined by the mask 150) impinges on a location 300 away from the sample 40. Thereafter, the sample 40 is translated in the Y-direction, and gains momentum to reach a predetermined velocity before the masked irradiation beam pulse 164 reaches and impinges an edge 45 of the sample 40 at a location 310. This is shown in Figure 4 as a path 305 which illustrates the path of the masked irradiation beam pulse 164 as the sample 40 is translated in the Y-direction. By controlling the motion of the sample 40 in the X and Y directions, the computer 106 controls the relative position of the sample 40 with respect to the masked irradiation beam pulse 164 which irradiates the silicon thin film 52 provided on the sample 40. The pulse duration, the pulse repetition rate and the energy of each pulse of the masked irradiation beam pulse 164 are also controlled by the computer 106.

In the first embodiment of the present invention as illustrated in Figure 4, the sample 40 is translated with respect to the stationary irradiation beam pulse 164 in order to sequentially irradiated successive portions of the silicon thin film 52 along predefined paths of irradiation to obtain a lateral growth of large grains having controlled

grain size and shape, and controlled grain boundary location and orientation in the silicon thin film 52. In particular, as the sample 40 is translated in the Y-direction, the stationary irradiation beam pulse 164 impinges and melts successive portions of the entire first column 210 along a path 315, starting from the location 310 until the radiation beam pulse 164 reaches a bottom edge 47 (opposite and parallel to the edge 45) at a location 320. The masked irradiated beam pulses 164 are only limited to the intensity pattern 235 defined by the mask 150 so long as each beamlet of the intensity pattern 235 of each masked irradiation beam pulse 164 has sufficient energy to melt a region of the silicon thin film 52 which it irradiates throughout its entire thickness, and each melted region of the silicon thin film 52 is sufficiently dimensioned to allow the lateral growth of grains in the melted region without nucleation inside the melted regions.

To reiterate, the paths of the irradiation of the silicon thin film 52 are shown in Figure 4 in the frame of reference of the translating sample 40 so that the stationary irradiation beam pulse 164 (shown in Figure 1) is depicted as traversing the stationary sample 40.

As shown in Figure 4, the computer 106 causes the radiation beam pulse 164 to be emitted and the sample 40 to be positioned such that the masked irradiated beam pulse 164 impinges a first location 300 in the frame of reference of the sample 40. The sample 40 is then accelerated in the +Y direction under the control of the computer 106 to reach a predetermined velocity with respect to the stationary irradiation beam pulse 164, which traces a first path 305 not on the sample 40. It is noted again that the path 305 is not the result of movement of the masked irradiated beam pulse 164, which is stationary, but represents the movement of the sample 40 relative to the stationary irradiation beam pulse 164.

When the upper edge 45 of the sample 40 reaches the position of impingement by the radiation beam pulse 164 at the location 310, the sample 40 is translating at the predetermined velocity with respect to the stationary irradiation beam pulse 164. The predetermined velocity V can be defined according to the following equation:

$$V = f \times \frac{W_B}{2} \qquad (2)$$

where f is the frequency (pulse repetition rate) of the stationary irradiation beam pulse 164 and W_B is the dimension of the masked irradiation beam pulse 164 in the Y-direction. As discussed above, the dimension of the masked irradiated beam pulse 164 in the Y-direction may be 2cm. The frequency f of the stationary irradiation beam pulse 164 may have a repetition pulse rate between 100 hertz and 500 hertz (preferably 250 hertz). In this embodiment of the present invention, the predetermined velocity is, for example, 250 cm/sec. It is also possible to utilize other frequency ranges depending on the configuration and the type of the excimer laser 110 being used. Thereafter, the sample 40 is continuously translated in the +Y direction at the predetermined velocity while the masked irradiated beam pulses 164 irradiates successive portions of the silicon thin film 52 provided on the sample 40 at a predetermined pulsed repetition rate along a second irradiation path 315, which traverses the length of the sample 40 in the −Y direction.

Figures 5A-5G illustrate the sequential steps of the irradiation (i.e., by the radiation beam pulse 164) and the re-solidification of the first column 210 of the silicon thin film 52 provided on the sample 40 as the sample 40 is translated in the +Y direction so that the successive portion of the silicon thin film 52 in the first column 210 of the sample 40 are irradiated along the second irradiation path 315.

In particular, Figure 5A shows the irradiation and complete melting of first areas 410 of the silicon thin film 52 in the first conceptual column 210 adjacent to the top edge 45 of the sample 40 where the sample 40 is overlapped only by the first beamlet section 250 of the intensity pattern 235 of the stationary radiation beam pulse 164, and the first slit-shaped beamlets 255 irradiates and completely melts the silicon thin film 52 in areas 410 of the sample. Regions 415 of the silicon thin film 52 on the sample 40 are not irradiated and melted as a result of being overlapped by the first shadow regions 257 of the intensity pattern 235 of the masked irradiated beam pulse 164.

As the sample 40 is translated past the location 310 (illustrated in Figure 4), the masked irradiated beam pulse 164 provides emit the first slit-shaped beamlets 255 of the intensity profile 235 (or a first masked radiation beam pulse) and irradiates each of the first areas 410 of the silicon thin film 52 on the first conceptual column 210. In this manner, the silicon thin film portions provided in the first areas 410 are melted

throughout the entire thickness thereof. It should be noted that each of the regions 415 of the first column 210 of the sample 40, overlapped by a respective one of the first shadow regions 257 of the intensity profile 235 remains unmelted.

Turning now to Figure 5B, before the irradiation by a second irradiation beam pulse, in accordance with the predetermined pulse repetition rate, each of the areas 410 of the silicon thin film 52 in the first conceptual column 210 of the sample 40 that were melted by the first radiation beam pulse cools, re-solidifies and crystalizes to form two columns of grains 420, 425 grown towards one another from the respective adjoining unmelted regions 415.

During re-solidification and crystallization of the melted first areas 410, the unmelted regions 415 bordering the melted first areas 410 seed the lateral growth of grains in respective adjoining melted first areas 410. The two columns 420, 425 abut one another along a respective one of a plurality of grain abutment boundaries 430 after the abutting grains have grown by a characteristic growth distance of approximately 1.5μm. Both columns of grains 420, 425 in each one of the re-solidification first areas 410 have a respective central portion in which grain boundaries form large angles (e.g., approximately 90°) with respect to the irradiation path 315.

While the cooling, re-solidification and crystallization of the melted areas 410 is taking place, the sample 40 is being continuously translated with respect to the stationary irradiation beam pulse 164 along the irradiation path 315 in the Y-direction. This is because when another area of the silicon thin film 52 on the first column 210 is irradiated by the second radiation beam pulse, the second beamlets 265 of the intensity pattern 235 of the stationary irradiation beam pulse 164 impinges the respective portion of the silicon thin film 52 so as to only partially overlap the respective adjacent pairs of the re-solidified and crystalized areas 410 and the unirradiated regions therebetween. For example, the timing for the emission of the second radiation beam pulse is controlled such that the distance of the translation of the sample 40 is less than the length of the first slit-shaped beamlets 255 (e.g., ½mm).

Turning to Figure 5C, the silicon thin film 52 in the first conceptual column 210 of the sample 40 is irradiated using both the first and second beamlet sections 250, 260 of the intensity profile 235. When the sample 40 reaches the position

on the first column 210 at which the first slit-shaped beamlets 255 of the intensity profile 235 would overlap certain portions of the re-solidified areas 410, the computer106 controls the excimer laser 110 to generate another irradiation beam pulse through the mask 150 (i.e., the second radiation beam pulse) to irradiate particular areas of portions of the silicon thin film 52 in the first conceptual column 210. The computer 106 times the pulses and controls the translation of the sample 40 so that the second radiation beam pulse irradiates the appropriate areas of the silicon thin film 52 as discussed below.

As shown in Figure 5C, the second radiation laser pulse is generated so that the first slit-shaped beamlets 255 irradiate and completely melt second areas 435 of the silicon thin film 52 in the first conceptual column 210, and the second slit-shaped beamlets 265 completely melt third areas 445 of the silicon thin film 52 in the first conceptual column 210. The second areas 435 preferably extend along the same scanning path in the first column 210 as the first areas 410 that are shown in Figure 5B. However, the second areas 435 are provided at an offset, the distance of which is slightly less than then length of the first areas 410 (i.e., ½mm) in the negative Y-direction. As shown in Figure 5C, overlapped areas 440 are provided between the first areas 410 and the second areas 435 which are small sections of the first areas 410 that were re-solidified, but again completely melted by the first slit-shaped beamlets 255 of the intensity profile 255. The computer 106 controls the timing of the pulses and the translation of the sample 40 to allow for the existence of such overlapped areas 440 so as to avoid the possibility of having unirradiated areas on the silicon thin film 52. The width of the overlapped areas 440 can be, e.g., $1\mu m$. Other width of the overlapped areas 440 may also be used (e.g., $0.5\mu m$, $1.5\mu m$, $2\mu m$, etc.)

The third areas 445 preferably extend along a line Q (in the Y-direction) which is parallel to the centerline P, along which the first areas 410 and the second areas 435 extend, and offset therefrom by approximately $0.75\mu m$. In addition, the bottom edge 436 of each of the second areas 435 is offset with respect to the Y-direction by $505\mu m$ from the bottom edge 446 of the respective third area 445. The top edge 437 of each of the second areas 435 is offset in the Y-direction by $5\mu m$ from the bottom edge 446 of the respective third area 445. Because of such configuration of the second areas 435 and the third areas 445, the third areas 445 overlap certain portions 450 of the re-solidified first

areas 410 melted by the first masked irradiation beam pulse. Therefore, the silicon thin film 52 in these portions 450, which were overlapped by the third areas 445, are again completely melted throughout its thickness along with the previously unmelted regions.

Figure 5D shows the cooling, re-solidification, grain growth and crystallization of the completely melted silicon thin film 52 provided in the second and third areas 435, 445, the overlapped areas 440 and the portion 450, and the previous melted regions. With reference to the second areas 435, each of these areas 410 re-solidifies and crystalizes to form two columns of grains 460, 465 that are seeded and grown towards one another from the adjoining unmelted regions 455. The two columns 460, 465 abut one another along a respective one of a plurality of grain abutment boundaries 468 after the abutting grains have grown by a characteristic growth distance of approximately 1.5μm. Both columns 460, 465 in each of the second re-solidification areas 435 have a respective central portion in which grain boundaries form large angles (e.g., approximately 90°) with respect to the second irradiation path 315.

In the melted third areas 445 that adjoin respective non-overlapped portions of the first areas 410, which have been previously irradiated and re-solidified, the grains in such non-overlapped portions of the first areas 410 seed grain growth in the adjoining region of the third areas 445 until grains growing in the opposite directions in the third areas 445 abut one another at a grain abutment boundaries 470. In this manner, the grains of the first areas 410 of grains 420, 425 of silicon thin film 52 in the first areas are extended into the third areas 445 so as to increase the lengths of the grains.

Similarly to the discussion above with reference to Figure 5B, while re-solidification of the second and third melted areas 435, 445 is taking place, the sample 40 is being continuously translated with respect to the stationary irradiation beam pulse 164 along the second irradiation path 315. In particular, the sample 40 is translated so that another area of the silicon thin film 52 is irradiated by a third radiation beam pulse having the intensity pattern 235 shown in Figure 3, and the sample 40 is translated so as to only partially overlap certain regions of the re-solidified second and third areas 435, 445 by the third irradiation beam pulse. The timing of the generation of the third irradiation beam pulse is controlled in the similar manner as the control of the generation of the second pulse described above.

Turning to Figure 5E, the third radiation laser pulse is generated so that the first slit-shaped beamlets 255 irradiate and completely melt fourth areas 475 of the silicon thin film 52 in the first column 210, and the second slit-shaped beamlets 265 completely melt fifth areas 485 of the silicon thin film 52 in the first column 210. The fourth areas 475 preferably extend in the same direction as the first areas 410 which are illustrated in Figure 5B. Similarly to the second areas 435 of Figure 5C, the fourth areas 475 are provided at a distance from the second areas 435 in the negative Y-direction which is slightly less than the length of the second areas 435 (i.e., slightly less than ½mm). Overlapped areas 490 provided between the second areas 435 and the fourth areas 475, and overlapped areas 495 provided between the third areas 445 and the fifth areas 485 are small sections of the first and second areas, respectively, which were re-solidified but again completely melted by the first and second slit-shaped beamlets 255, 265 of the further intensity profile 405 of the masked irradiated beam pulse 164, respectively. The computer 106 controls the timing of the pulses and the translation of the sample 40 to allow for the creation of such overlapped areas 490, 495 in order to avoid the possibility of having unirradiated areas on the silicon thin film 52. The width of the overlapped areas 490, 495 is similar to that of the overlapped areas 440.

The positional relationship between the fourth and fifth areas 475, 485 is substantially the same as the positional relationship between the second and third areas 435, 445, the details of which are described above. Due to such configuration, the fifth areas 485 overlap certain portions 497 of the third re-solidified areas 445. Therefore, the silicon thin film 52 in these portions 497 (which were overlapped by the fifth areas 485) is again completely melted.

Figure 5F shows the re-solidification and grain growth in the previously completely melted fourth and fifth areas 475, 485 and the overlapped areas 490, 497. The description of the re-solidification and lateral growth provided above with reference to Figure 5D is equally applicable herein. In particular, as the fourth areas 475 are re-solidified, and the controlled grain lateral growth occurs therein that is seeded from their edges, two columns of grain formations 500, 505 are formed, thus effectively extending the columns 460, 465, respectively. With respect to the fifth areas 485, two columns of grain formations 510, 515 are also formed in a similar manner. Thus, the controlled

lateral grain growth of the silicon thin film 52 is further extended along the first column 210 to include the previously and completely melted silicon thin film 52 provided in the fourth and fifth areas 475, 485.

As the sample 40 is continuously translated and the first column 210 of the silicon thin film 52 is irradiated by the masked irradiated beam pulse 164 along the second path 315, further areas of the silicon thin film 52 on the first column 210 are melted consistent with the melting configuration of the areas 435, 445 and the areas 475, 485, and the controlled sequential lateral solidification and grain growth in all such further areas of the first column 210 is effectuated. Thus, all portions of the silicon thin film 52 in the entire first conceptual column 210 of the sample 40 between the top edge 45 and the bottom edge 47 of the sample 40 are subjected to the continuous motion SLS. Since all areas in the first column 210 have been irradiated and subjected to the SLS, there is no need to further re-irradiate any portion of the silicon thin film 52 provided therein. In particular, the end product of such continuous motion SLS for the first column 210 is illustrated in Figure 5G, which shows that when the cooling and re-solidification of all melted areas 410, 435, 445, 475, 485, etc. is completed, a re-solidification region 520 is formed having contiguous columns 510 of relatively long grains, along with grain boundaries oriented generally along the X-direction. This is an improvement over the prior SLS methods which require microtranslations of the sample 40 to be performed while each respective column of such sample is irradiated using the radiation beam pulse. Such microtranslations require the continuous translation of the sample to be slowed to a stop, the sampled to be microtranslated, then to increase the speed of the translation of the sample via the sample translation stage to reach a predetermined velocity, and to continue with the translation of the sample while irradiating the particular column of the silicon thin film.

Turning back to Figure 4, when the sample 40 is translated so that the fixed position of impingement of the masked irradiated beam pulse 164 reaches a bottom edge 47 of the sample 40 at a location 320 with respect to the position of the sample 40, the translation of the sample 40 is slowed along a third path 325 until the sample 40 comes to a full stop when the fixed position of impingement of the radiation beam pulse 164 is at a location 330 with respect to the position of the sample 40. In the present

embodiment, the predetermined pulse repetition rate is, for example, 250-300 pulses/sec (which is preferable for the excimer laser 110 used herein) and each pulse provides a beamlet intensity of approximately 500 mJ/cm^2 with a pulse duration of approximately 30 nseconds.

After the stationary irradiation beam pulse 164 in the frame of reference of the translating sample 40 has come to a stop at the location 330, the sample 40 translated in the X direction under the control of the computer 106 so that the pulsed irradiation beam pulse 164 traces a fourth path 335 until the masked irradiation beam pulse 164 impinges the sample 40 at a location 340. The sample 40 is then accelerated in the -Y direction so that the pulsed irradiation beam traverses a fifth path 345 such that the sample 40 reaches the predetermined velocity of translation by the time the bottom edge 47 of the sample 40 reaches a position 347 of impingement of the masked irradiated beam pulse 164. Thereafter, the sample 40 is continuously translated at the predetermined velocity in the – Y direction for the entire length of a sixth irradiation path 350, while the masked irradiation beam pulse 164 sequentially irradiates the metal layer 52 on second column 220 of the sample 40 at the predetermined pulsed repetition rate.

Referring to Figure 6A, there is shown a portion 540 of the silicon thin film 52 in the second conceptual column 220 immediately above the lower edge 47 of the sample 40, after the translation of the sample 40, so that it is impinged by the masked irradiated beam pulse 164 along the sixth path 250. The portion 540 of the silicon thin film 52 in the second column 220 is first irradiated using the second slit-shaped beamlets 265, and areas 550 of the portion 540 are completely melted throughout their entire thickness. This is because the portion of the intensity profile of the masked irradiated beam pulse 164 which irradiates and completely melts the areas 550 using the second beamlet section 260 having the second slit-shaped beamlets 265 provided in the configuration that was described above. At this point in the process, the first slit-shaped beamlets 255 do not irradiate the second column 220 of the sample 40 because they are irradiated outside the boundaries of the sample 40 (i.e., below the bottom edge 47). It should be noted that a small strip 550 of a particular area 550, which is adjacent to the re-solidification region 520 of the first conceptual column 210, slightly overlaps a small portion 555 of the re-solidification region 520 along the length of such area 550 (e.g., for

½mm). Prior to the irradiation by the second slit-shaped beamlets 265, when the masked irradiated beam pulse 164 impinges the sample 40 along the sixth path 350, this small portion 555 is subjected to the irradiation and SLS in the first column 210 of the sample. The small portion 555 corresponds to a initial section of the overlapping portion 230 shown in Figure 4. The irradiated and melted silicon thin film 52 of the areas 550 are separated by the shadow areas 560. As described above, the reason that these areas 560 were not irradiated is because the first shadow regions 267 of the intensity pattern 235 of the masked irradiated beam pulse 164did not irradiate and melt the areas 560.

The silicon thin film 52 provided in the areas 550 cool and re-solidify to effect lateral grain growth therein starting from their respective edges. In particular, each area 550 has two abutting columns of grains 570, 575 (shown in Figure 6B) which extend along the entire length of the respective area 550. As described above with respect to the SLS of the first column 210, the grain growth is initiated from and seeded from the shadow areas 560 toward a center of the respective areas 550. With respect to the particular area 550 which has the small overlapping area 555, the grains of neighboring completed portion 565 seed and laterally grow into that particular area 550.

Turning to Figure 6B as the areas 550 cool and re-solidify, the sample 40 is continuously translated in the negative Y-direction at the predetermined velocity along the sixth path 350, and another portion of the silicon thin film 52 in the second conceptual column 220 is irradiated. Since the masked irradiated beam pulse 164 impinges the silicon thin film 52 along the sixth path 350 while the sample 40 is translated by the computer 106 as described above, the second slit-shaped beamlets 265 irradiate and completely melt the silicon thin film 52 in areas 580. As discussed above with reference to Figures 5C and 6A, each of the areas 580 has a small area 582 which overlaps a portion of the previously irradiated and re-solidified respective area 550. In addition and as described above with reference to Figure 6A, the particular area 580 bordering the re-solidification region 520 has a small area 583 which overlaps and melts a portion 584 thereof. In addition, the first slit-shaped beamlet 255 irradiate and completely melt the silicon thin film 52 in the areas 585. A small area 583 corresponds to a portion of the overlapping portion 230 shown in Figure 4 which is subsequent to the small area 555 illustrated in Figure 6A.

As further shown in Figure 6B, the areas 585 are provided at a distance from the areas 580 (in the negative Y-direction) slightly greater than the entire length of the areas 580. The configuration of the areas 580, 585 with respect to one another is substantially similar to the configuration of the areas 435, 445 described above and shown in Figure 5C. Thereafter, the areas 580, 585 cool and re-solidify in a substantially the same manner described above with reference to in Figure 5C, only that the SLS for the silicon thin film 52 provided in the second column 220 of the sample if effectuated from the bottom edge 47 of the sample 40, instead of from the top edge 45 as provided for the first column 210.

Again turning back to Figure 4, when the sample 40 is translated in the -Y direction so that the fixed position of impingement of the masked irradiated beam pulse 164 reaches the top edge 45 of the sample 40, the translation of the sample 40 is slowed along a seventh path 355 until the sample 40 comes to a full stop when the fixed position of impingement of the radiation beam pulse 164 on the sample 40 is at a location 360 with respect to the sample 40. After the stationary irradiation beam pulse 164 in the frame of reference of the translating sample 40 has come to a stop at the fourth location 360 (i.e., the translation of the sample 40 is stopped), the sample 40 is translated in the negative X-direction under the control of the computer 106 so that the masked irradiated beam pulse 164 traces an eighth path 365 until the masked irradiated beam pulse 164 impinges a location 370 outside the boundaries of the sample 40. The sample 40 is then accelerated in the Y-direction so that the masked irradiated beam pulse 164 traverses another path which is substantially parallel to the second irradiation path 315 (i.e., the sample 40 is again translated in the Y-direction). This procedure continues until the silicon thin film 52 provided in all conceptual columns of the sample 40 are irradiated, and the SLS is successfully effectuated therein.

As described above, each such translation of the sample 40 and the irradiation thereof is performed for every conceptual column of the sample 40. Thus, if the sample 40 is conceptually subdivided into 15 columns, the sample 40 is continuously translated in the Y-direction or the negative Y-direction 15 times. The results of the single-step, continuous motion SLS according to the present invention is shown in Figure 7. This drawing illustrates the end product of the sample 40 whose every area of the

silicon thin film 52 extending along the entire periphery of the sample 40 is irradiated to promote the controlled SLS and grain growth thereon.

It is preferable to use a high aspect homogenized irradiation beam, i.e., having a wide and thin intensity profile in the direction of the translation of the sample 40. In particular, when such intensity is utilized, it takes less steps to irradiate all columns of the sample 40. There are also timing advantages to the utilization of the above-described embodiment of the method according to the present invention. Generally, the total process time $T_{PROCESS}$ to irradiate and process the silicon thin film 52 provided on the entire sample 40 is calculated as follows:

$$T_{PROCESS} = T_{CRYSTALIZATION} + T_{WASTED} \tag{3}$$

where:

$$T_{CRYSTALIZATION} = \frac{\frac{A_{TOTAL}}{A_{BEAM}} \times n}{f_{LASER}}, \tag{4}$$

A_{TOTAL} is the total area of the sample 40 (e.g., 40cm x 30cm = 1200cm^2), A_{BEAM} is a beam area (e.g., 2cm x 1mm = 20mm^2), and n is a number of shots fired at a particular point (e.g., for a two shot process illustrated in Figures 5A-5G and 6A-6B, n=2). In the present embodiment, the crystallization time for each column is approximately 1 second. Therefore, the total time of crystallization for the sample having 15 columns is 15 second. Next, the wasted time should be evaluated. For example,

$$T_{WASTED} = n_{STEP} \times T_{STEP}, \tag{5}$$

where n_{STEP} is the number of times the sample is stepped to the next column (e.g., for 15 columns, the sample is stepped 14 times), and T_{STEP} is the time required for each such stepping (e.g., 0.3 seconds). Thus, T_{WASTED} is 14 x 0.3 seconds = 4.2 seconds for the sample 40. To compare this result with the time wasted for the method and system described in the '585 application, while the crystallization time of each column of the sample 40 is the same for the system and method of the present invention and that of the '585 application (due to a reduction of the sample velocity in the present invention by half as compared to the velocity of the sample described in the '585 application), the

wasted time of the system and method of the '585 application is higher than that of the system and method of the present invention. This is because the system and method of the present invention does not require the sample 40 to be microtranslated (as described in the '585 application) when the masked irradiated beam pulse 164 is impinging a location outside of the periphery of the sample 40. Therefore, according to the present invention, the microtranslation time is not at issue because the sample 40 is not microtranslated. Thus, if the sample of '585 application is subjected to one microtranslation per column thereof, the time wasted not crystalizing the silicon thin film on the sample is 14 columns x 0.3 seconds = 4.2 second for microtranslations and 4.2 seconds for regular translations of the entire sample. Thus, the time savings to crystalize each sample using the system and method of the present invention is reduced by, e.g., 4.2 seconds as compared to the system and method of the '585 application.

Figure 8 shows an enlarged illustration of a second exemplary embodiment of an intensity pattern of the irradiated beam pulse as defined by a further mask 150 utilized by the system and method of the present invention as it impinges the silicon thin film on the substrate, which promotes a larger grain growth on the silicon thin film. This exemplary intensity pattern 600 includes slit-shaped beamlets 601, 603, 605, 607, 609, 611, 613, 615, 617, 619, etc. provided in a stepped manner. The width of the slit-shaped beamlets 601, 603, 605, 607, 609, 611, 613, 615, 617, 619 along the X-direction can be the same as that of the first slit-shaped beamlets 255 of the intensity pattern 235 (e.g., 3μm), and the length of these slit-shaped beamlets can be, e.g., 0.2 μm. Other sizes and shapes of the slit-shaped beamlets 601, 603, 605, 607, 609, 611, 613, 615, 617, 619, etc. are conceivable, and are within the scope of the present invention.

In particular, the slit-shaped beamlet 601 is provided in a top-rightmost corner of the intensity pattern 600 The slit-shaped beamlet 603 is provided at an offset, in the -X direction, from the slit-shaped beamlet 601. In particular, a top edge 630 of the slit-shaped beamlet 603 extends slightly above a line A on which the center 602 of the slit-shaped beamlet 601 extends. Similarly, the slit-shaped beamlet 605 is provided at an offset (in the -X direction) from the slit-shaped beamlet 603 so that a top edge 631 of the slit-shaped beamlet 605 extends slightly above a line B on which the center 604 of the slit-shaped beamlet 603 extends. The same applies for the position of the slit-

shaped beamlet 607 with respect to the slit-shaped beamlet 605, and the slit-shaped beamlet 609 with respect to slit-shaped beamlet 607. The slit-shaped beamlets 611, 613, 615, 617 and 619 are arranged in a substantially the same configuration as the slit-shaped beamlet 601, 603, 605, 607, 609, except that while the starting location of the slit-shaped beamlet 611 is the same as of the slit-shaped beamlet 601 along the Y-direction, the slit-shaped beamlet 611 is offset along the X-direction by a particular length 635. According to an exemplary embodiment of the present invention, the top edge 634 of the slit-shaped beamlet 611 is provided slightly above a line C on which the bottom edge 633 of the slit-shaped beamlet 609 extends. The configuration of the intensity pattern 600 is provided such that the first row 640 of the intensity pattern 600 (consisting of the slit-shaped beamlets 601, 603, 605, 607, 609) is provided above the second row 641of the intensity pattern 600 (consisting of the slit-shaped beamlets 611, 613, 615, 617, 619) along the -X direction, followed by the third row 642, etc. The intensity pattern 600 can include a large number of rows of slit-shaped beamlets, e.g., 100, 1000, etc., depending on the width of the irradiation laser beam 149 impacting the mask 150, and the configuration of the slits and opaque regions of the mask 150.

Figure 9 shows the grain structure of a portion of an exemplary first conceptual column 210 of the sample 40 having the silicon thin film 52 therein, as the intensity pattern 600 of the masked irradiated beam pulse 164 of Figure 8 impinges the respective portions of the silicon thin film 52, at an exemplary stage of SLS processing according to a second exemplary embodiment of the method of the present invention. Using the exemplary embodiment of the method shown in Figure 9, longer grains can be grown on the silicon thin film 52. This exemplary embodiment of the method according to the present invention can be implemented in a substantially the same manner as the embodiment described above with reference to Figures 4, 5A-5G and 6A-6B, while utilizing the intensity pattern 600 instead of the intensity pattern 235 to irradiate, and completely melt the silicon thin film 52 in the first conceptual column 210 of the sample 40.

In particular, Figure 9 illustrates this exemplary embodiment when the silicon thin film 52 in the first conceptual column 210 of the sample 40 is irradiated by the intensity pattern 600, while the sample 40 is continuously translated in the Y-

direction. The silicon thin film 52 in the areas 650, 652, 654, 656, 658, 660, 662, 664, 666, 668, etc. of the first conceptual column 210 of the sample 40 are completely melted throughout its thickness. It should be understood that these particular areas are being irradiated because the slit-shaped beamlets 601, 603, 605, 607, 609, 611, 613, 615, 617, 619, etc. of the intensity pattern 600 of the masked irradiated beam pulse 164 impinged such areas 650, 652, 654, 656, 658, 660, 662, 664, 666, 668, etc. to completely melt the silicon thin film 52 provided therein (i.e., throughout the thickness of the silicon thin film 52).

The silicon thin film 52 provided in most of the areas 650 was not subjected to the previous lateral solidification. With the respect to the area 652, the slit-shaped beam 603 impinging on the silicon thin film 52 provided in this area 652 melts more than half of the re-solidified section of corresponding to the location thereof (which was previously irradiated by the slit-shaped beamlet 601). In particular, the top edge of the area 652 is provided slightly above a line M on which a boundary 644 extend along the M-axis, the boundary 644 being formed by the previous irradiation and grain growth by the slit-shaped beamlet 601. It should be understood that due to such position of the area 652, the center 653 thereof is provided above a line N along which a lower edge of the area 650 extends. Similarly, the center 655 of the area 654 is positioned slightly above an axis along with the lower edge of the area 652 extends, the center 657 of the area 656 is positioned slightly above a line along with the lower edge of the area 654 extends, and the center 659 of the area 658 is positioned slightly above an axis along with the lower edge of the area 656 extends. Therefore, the areas 650, 652, 654, 656, 658 are provided in a configuration which substantially corresponds to that of the slit-shaped beamlets 601, 603, 605, 607, 609 of the first row 640 of the intensity pattern 600 of the masked irradiated beam pulse 164.

The areas 660, 662, 664, 666, 668, in which the silicon thin film 52 is completely melted throughout its thickness, are arranged in a substantially the same configuration as that of the areas 650, 652, 654, 656, 658, except that the area 660 is provided at an offset, along the -X direction, from the area 650, with the distance of the offset being approximately equal to the distance 635 between the slit-shaped beamlet 601 and the slit-shaped beamlet 611 as described above with reference to Figure 8. In

addition, the area 658 has a small portion 670 which overlaps the region of the silicon thin film 52 which was previously irradiated by the slit-shaped beamlet 611. It is preferable to utilize this small portion 670 such that the small grain regions provided at the edges of the re-solidified areas of the silicon thin sample 52 are minimized or even eliminated.

Figure 10 shows the progression of the SLS of the first column 210 using the mask of Figure 8 as the sample 40 is continuously translated along the Y-direction. In this manner, a number of rows 710, 720, 730, etc. of the silicon thin film 52 in the first conceptual column 210 are produced. The number of these rows 710, 720, 730, etc. corresponds to the number of the rows 640, 641, 642, etc, of the intensity pattern 600 illustrated in Figure 8. Similarly to the method of Figure 4, when the sample 40 is translated so that the masked irradiated beam pulse 164 reaches the lower edge 47 of the sample 40, and the masked irradiated beam pulse 164 no longer impinges the silicon thin film 52 provided on the sample 40, the sample is translated in the X-direction to reach a particular location to position the sample 40 for further translation so that the irradiation beam 164 may impinge the silicon thin film 52 in the second conceptual column 220 of the sample 40. Thereafter, the sample 40 is translated in the -Y direction and the silicon thin film 52 in the second conceptual column 220 of the sample 40 is irradiated in a substantially the same manner as provided above with reference to Figures 9 and 10. However, the slit-shaped beamlets 609, 619 (and not the slit-shaped beamlets 601, 611) first irradiate the silicon thin film 52 in the second conceptual column 220, starting from the lower edge 47, and completing the irradiation of the second column of the sample 40 at the top edge 45. In this manner, the silicon thin film 52 in all conceptual columns of the sample 40 can be effectively subjected to the continuous motion SLS, with longer grains being grown thereon.

The exemplary velocity V to translate the sample 40 and irradiate it using the intensity profile 600 of the masked irradiated beam pulse 164 illustrated in Figure 8 is provided as follows:

$$V = L_B * f_{LASER} \tag{6}$$

where L_B is the width of one of the slit-shaped beamlets 601, 603, 605, 607, 609, 611, 613, 615, 617, 619, etc. of the intensity pattern 600 shown in Figure 8, and f_{LASER} is the frequency of the irradiation beam 149 emitted by, e.g., the excimer laser 110. In the exemplary embodiment illustrated in Figure 8, L_B equals to 0.2mm, and f_{LASER} can equal to 300 hertz. Thus the exemplary velocity V of the sample translation can equal to 60mm/seconds for five (5) beamlets provided in each row 640, 641, 642, etc. of the intensity pattern 600. According to the exemplary embodiment of the present invention, if the number of slit-shaped beamlets of the intensity profile 600 per row increases to, e.g., ten (10) slits, then the length of each slit-shaped beamlet is preferably reduced by half to, e.g., 0.1mm. Therefore, with 10 slit-shaped beamlets per column of the intensity pattern 600 and using the above calculations, the velocity of the sample translation is equal to 30mm/second. However, using a higher number of the slit-shaped beamlets in a single row of the intensity pattern 600, it is possible to obtain longer grains on the silicon thin film 52 of each conceptual column of the sample 40.

Figure 11 shows an enlarged illustration of a third exemplary embodiment of an intensity pattern 800 of the irradiation beam pulse as defined by another mask 150 utilized by the system and method of the present invention as it impinges the silicon thin film on the substrate. Similar to the intensity pattern 235 of Figure 3, the intensity pattern 800 includes the first beamlet section 250 and the second beamlet section 260. In addition, the intensity pattern 800 includes one reduced intensity section 810 bordering the second beamlet section 260. The reduced intensity portion 810 has only 70% of the intensity of the homogenized irradiation beam 149, and can be generated by a gray-scale portion of the mask 150 by irradiation the homogenized irradiation beam 149 through such gray-scale portion of the mask 150. This reduced intensity portion 810 does not melt an area of the silicon thin film 52 which it impacts throughout the entire thickness thereof; indeed, this reduced intensity portion 810 of the masked irradiated beam pulse 164 only partially melts the area of the silicon thin film 52 that it irradiates.

The intensity pattern 800 shown in Figure 11 can be used for irradiating the sample 40 via the exemplary embodiment of the method according to the present invention illustrated in Figures 5A-5G and 6A-6B. Due to the presence of the reduced intensity portion 810 in the intensity pattern 800, the width of the cross-section of the

masked irradiated beam pulse 164 can be approximately 1.5mm (as opposed to having the width of the masked irradiated beam pulse 164 being 1mm as provided for the intensity pattern 235 of Figure 3) so as to utilize all areas of the intensity pattern 800, including the reduced intensity portion 810. However, while the width of the masked irradiated beam pulse 164 is increased, the sample 40 may be translated at the same predetermined velocity as the velocity used with the intensity pattern 235 with reference to Figures 4, 5A-5G and 6A-6B.

The illustration of the continuous motion SLS process according to the present invention using the intensity pattern 800 is substantially the same as for the intensity pattern 235 for the first two irradiation beam pulses impacting the silicon thin film 152 as provided above with reference to Figures 5A-5D. However, for the third irradiation beam pulse shown in Figure 5E, the area labeled as 820 would be completely irradiated using the reduced intensity portion 810 of the intensity pattern 800. While the area 820 is irradiated by the reduced intensity portion 810 of the intensity pattern 820, it is only partially melted. Thereafter, the area 820 re-solidifies while maintaining the integrity of the grains grown therein. This partial melting is advantageous because upon re-solidification of the area 820, the surface thereof is flattened, and thus peaks and valleys on this surface are minimized. This procedure continues for the first conceptual column 210 of the sample 40 until the sample 40 is continuously translated so that the masked irradiated beam pulse 164 just passes the bottom edge 47 of the sample 40.

The procedure described above with reference to Figure 4 is continued in a substantially the same manner as described above which utilizes the intensity pattern 235. However, according to this embodiment of the method according to the present invention which utilizes the intensity pattern 800 for irradiating the silicon thin film 52 provided on the sample 40, after the masked irradiated beam pulse 164 stops impinging any area of the first column 210 of the sample 40, and before it starts impinging the second column 220 of the sample 40, the reduced intensity portion 810 of the intensity pattern 800 is placed such that when the masked irradiated beam pulse 164 starts irradiating the second conceptual column 220 of the sample 40. Thus, the reduced intensity portion 810 of the intensity pattern 800 of the masked irradiated beam pulse 164 is provided at the back of the two beamlet sections 250, 260 of the intensity pattern 800.

This can be done by, e.g., rotating the mask 150 by 180°. In this manner, the reduced intensity portion 810 can partially irradiate the previously-irradiated and re-solidified areas of the second column 220 (i.e., already subjected to the SLS via the beamlets of the first and second beamlet sections 250, 260 of the intensity pattern 800). Upon reaching the top edge 45 of the sample, the reduced intensity portion 810 of the intensity pattern 800 can again be placed in the same configuration as was utilized when the first conceptual column 210 of the sample 40 was being irradiated by the masked irradiated beam pulse 164 (e.g., by rotating the gray-scale portion of the mask 150 by 180°). In this manner, the silicon thin film 52 of the entire sample 40 can be effectively subjected to the continuous motion SLS, while flattening the surface of the irradiated, re-solidified and crystalized silicon thin film 52 on the entire periphery thereof.

Figure 12 shows an enlarged illustration of a fourth exemplary embodiment of an intensity pattern 830 of the irradiated beam pulse as conceptually defined by yet another mask utilized by the system and method of the present invention. as it impinges the silicon thin film on the substrate. Similar to the intensity pattern 800 of Figure 3, the intensity pattern 830 includes the first beamlet section 250, the second beamlet section 260 and a first reduced intensity section 810 bordering the second beamlet section 260. In addition, the intensity pattern 830 includes second reduced intensity section 810 bordering the first beamlet section 250. As with the first reduced intensity portion 810, the second reduced intensity portion 840 has only 70% of the intensity of the homogenized irradiation beam 149, and can be generated by another gray-scale portion of the mask 150 by irradiation the homogenized irradiation beam 149 there through.

It should be understood that the intensity pattern illustrated in Figure 12 is shown as if both first and second reduced intensity portions 810, 840 are being used for irradiating the silicon thin film 52 provided on the sample 40. However, as shall be described in further detail below, only one of these reduced intensity portions 810, 840 of the intensity pattern 830 are to be used for such irradiation.

The intensity pattern 830 shown in Figure 12 can be used for irradiating the silicon thin film 52 with the method according to the present invention in a similar manner as described above with reference to the use of the intensity pattern 800 of Figure

11. Again, the width of the cross-section of the masked irradiated beam pulse 164 is also approximately 1.5mm. In particular, when the sample 40 is continuously translated so that the masked irradiated beam pulse 164 irradiates the first conceptual column 210, only the first beamlet section 250, the second beamlet section 260 and the first reduced intensity portion 810 of the intensity pattern 830 of the masked irradiated beam pulse 164 is irradiated and impinges the silicon thin film 52 on the sample 40, while the second reduced in tensity portion 840 is not utilized. Then, the procedure for the SLS of the first conceptual column 210 continues in substantially the same manner as the procedure described above for the first conceptual column 210 which uses the intensity pattern 800.

Then, after the masked irradiated beam pulse 164 stops impinging any area of the first conceptual column 210, and before it starts impinging the second conceptual column 220 of the sample 40, the mask 150 is positioned or shifted in the Y-direction by the mask translation stage such that the second reduced intensity portion 840 of the intensity pattern 830 is utilized when the masked irradiated beam pulse 164 starts irradiating the second conception column 220 of the sample, while not utilizing the first reduced intensity portion 810 for any irradiation of the silicon thin film 52 in the second conceptual column 220 of the sample. In this manner, the second reduced intensity portion 840 of the intensity pattern 830 of the masked irradiated beam pulse 164 is provided at the back end of the first and second sections 250, 260 of the intensity pattern 830 of the masked irradiated beam pulse 164 to irradiate the silicon thin film 52 in the second conceptual column 220 of the sample 40. Upon reaching the top edge 45 of the sample 40, the mask 150 is positioned or shifted in the negative Y-direction by the mask translation stage so that the intensity pattern 830 is provided in the same configuration as was utilized when the first conceptual column 210 of the sample 40 was irradiated by the masked irradiated beam pulse 164.

Figures 13A-13D show the radiation beam pulse intensity pattern and the grain structure of a portion of an exemplary first conceptual column of a silicon thin film 52 on the sample 40 at various sequential stages of SLS processing according to another exemplary embodiment of the method of the present invention. In this exemplary embodiment, the silicon thin film 52 of the entire sample 40 has already undergone the continuous motion SLS, and then rotated 90° in a clock-wise direction by the sample

translation stage 180 (i.e., controlled by the computer 106). After such rotation, the sample 40 is again conceptually subdivided into, e.g., 15 columns, the sample 40 is translated in the same manner as described above with reference to Figures 4, 5A-5G and 6A-6B.

In particular, Figure 13A shows melted areas 860 of a first conceptual column 850 which were irradiated by the beamlets 255 of the first beamlet section 250 of the intensity pattern 235 illustrated in Figure 3, as the sample 40 is continuously translated the Y-direction. As discussed above for the areas 210 in reference to Figure 5A, the areas 860 are melted throughout their entire thickness. Contrary to the areas 210, the areas 860 of the first column 850 were previously subjected to the SLS prior to their melting. Then, as shown in Figure 13B, the areas 860 cool, re-solidify and re-crystalize. The grain seeding and growth takes place starting from the borders of the areas 860. In this embodiment, because the silicon thin film 52 of the sample 40 had already underwent the SLS, the grains provided at the edges of the areas 860 (which were grown in the controlled manner) seed the areas 860, and start growing into the re-solidifying areas 860 to form areas 865 which have larger areas of single grain growth. The procedure continues as shown in Figure 13C such the sample 40 is translated in the Y-direction and irradiated in a substantially similar manner as described above with reference to Figure 5C. Similarly to the areas 435, 445, certain areas 870, 875 of the silicon thin film 52 in the first conceptual column 850 are melted. As with the areas 435, 445, particular portions of the areas 870, 875 overlap certain portions of the previously irradiated and re-solidified areas 865 of Figure 13B. As shown in Figure 13D, upon cooling and re-solidification of the areas 870, the lateral grain growth is seeded and promoted from their borders using the grains grown using the process described above with reference to Figures 5A-5G to form the resultant areas 885. With respect to the cooling, re-solidification and re-crystallization of the areas 875, the grain growth in the resultant areas 880 is promoted using the grains of the re-solidified areas 865 provided at the borders of the areas 875. According to the procedure described above with reference to Figures 13A-13D as it relates to the technique described above with reference to Figures 5A-5G and 6A-6B, its is possible to effectuate the SLS which provides larger regions 900 of single grains on the silicon thin film 52 of the sample 40, as illustrated in Figure 14.

Referring next to Figure 15, there is shown a flow diagram of exemplary steps carried out with the aid of the computer 106 (or other control devices) for the single-step, continuous motion SLS processing in accordance with the present invention to control the shape and size of grains, and the location and orientation of grain boundaries in the silicon thin film 52 of the sample 40. As shown in the flow diagram of Figure 15, in step 1000 the hardware components of the system of Figure 1, such as the excimer laser 110, the beam energy density modulator 120, the beam attenuator 130 and the shutter 152 are first initialized at least in part by the computer 106. A sample 40 is loaded onto the sample translation stage 180 in step 1005. It should be noted that such loading may be performed either manually or automatically using known sample loading apparatus under the control of the computer 106. Next, the sample translation stage 180 is moved, preferably under the control of the computer 106, to an initial position in step 1010. The various other optical components of the system are adjusted manually or under the control of the computer 106 for a proper focus and alignment in step 1015, if necessary. The radiation beam pulses 164 are then stabilized in step 1020 to a desired intensity, pulse duration and pulse repetition rate. In step 1021, it is determined whether a next radiation beam pulse irradiates the silicon thin film 52 after each melted region thereof has completely re-solidified following the irradiation by a previous radiation beam pulse. If not, in step 1022, the pulse repetition rate of the excimer laser 110 is adjusted. In step 1024 it is determined whether each beamlet of the intensity pattern of each radiation beam pulse has sufficient intensity to melt each one of the silicon thin film 52 overlapped thereby throughout its entire thicknesses without melting an adjacent region overlapped by a shadow region of the intensity pattern. If under-melting or over melting occurs, in step 1025, the attenuator 130 is adjusted so that each radiation beam pulse has sufficient energy to fully melt the metal layer in irradiated areas without over melting adjoining unirradiated regions.

In step 1027, the sample 40 is positioned to point the masked irradiated beam pulse 164 at the first conceptual column 210 of the sample 40. In step 1030, the current column of the sample 40 is irradiated using the radiation beam pulse 164 having an intensity pattern controlled by the mask 150, 700, 800, 830. In step 1035, the sample 60 is continuously translated so that the masked irradiated beam pulse 164 irradiates the

silicon thin film 52 along the current column of the sample 40 in a predetermined direction.

In step 1045, it is determined whether all conceptual columns of the sample 40 having the silicon thin film 52 provided thereon have been subjected to the SLS processing. If not, the sample 40 is translated to the next unirradiated conceptual column of the sample 40, and the process loops back to step 1030 for a further translation along a predetermined direction (e.g., an opposite direction), and for the irradiation of the next conceptual column of the sample 40 by the radiation beam pulse 164. If the SLS processing has been completed for all columns of the sample 40, the hardware components and the beam of the system shown in Figure 1 can be shut off (step 1055), and the process terminates.

The foregoing exemplary embodiments merely illustrate the principles of the present invention. Various modifications and alterations to the described embodiments will be apparent to those skilled in the art in view of the teachings herein without departing from the scope of the invention, as defined by the appended claims.

CLAIMS

1. A method for processing a silicon thin film sample on a substrate having a surface portion that does not seed crystal growth in the silicon thin film, the film sample having a first edge and a second edge, the method comprising the steps of:

(a) controlling an irradiation beam generator to emit successive irradiation beam pulses at a predetermined repetition rate;

(b) masking each of the irradiation beam pulses to define a first plurality of beamlets and a second plurality of beamlets, the first and second plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to melt irradiated portions of the film sample throughout their entire thickness;

(c) continuously scanning, at a constant predetermined speed, the film sample so that a successive impingement of the first and second beamlets of the irradiation beam pulses occurs in a scanning direction on the film sample between the first edge and the second edge;

(d) during step (c), successively irradiating a plurality of first areas of the film sample by the first beamlets of the irradiation beam pulses so that the first areas are melted throughout their thickness and leaving unirradiated regions between respective adjacent ones of the first areas;

(e) during step (c), allowing each one of the first areas irradiated by the first beamlets of each of the irradiation beam pulses to re-solidify and crystalize; and

(f) during step (e), successively irradiating a plurality of second areas of the film sample by the second beamlets of the irradiation beam pulses so that the second areas are melted throughout their thickness, wherein each one of the second areas partially overlaps a respective pair of the re-solidified and crystalized first areas and the respective unirradiated region therebetween.

2. The method of claim 1, further comprising the step of:

(g) during step (f), successively irradiating third areas of the film sample by the first beamlets to completely melt the third areas throughout their thickness, each of the third areas partially overlapping a respective one of the re-solidified and crystalized first areas and leaving further unirradiated regions between respective adjacent ones of the third areas.

3. The method of claim 2,

wherein one of the first areas and one of the third areas lie on a first line which is parallel to the scanning direction,

wherein one of the second areas lies of a second line which is parallel to the scanning direction, and

wherein the first line extends at an offset from the second line.

4. The method of claim 2, further comprising the step of:

(h) during step (g), allowing each one of the second areas irradiated by the first beamlets of each of the irradiation beam pulses to re-solidify and crystalize.

5. The method of claim 4, further comprising the steps of:

(i) during step (c), allowing each one of the third areas irradiated by the first beamlets of each of the irradiation beam pulses to re-solidify and crystalize; and

(j) during steps (h) and (i), successively irradiating a plurality of fourth areas of the film sample by the second beamlets of the irradiation beam pulses so that the fourth areas are melted throughout their thickness, wherein each one of the fourth areas partially overlaps a respective pair of the re-solidified and crystalized third areas and the respective further unirradiated region therebetween.

6. The method of claim 1, wherein the first edge is located on a side of the film sample which is opposite from a side of the film sample on which the second edge is located.

7. The method of claim 6, wherein steps (c) through (f) are continued until the successive impingement by the first and second beamlets of the irradiation beam pulses the film sample passes the second edge of the film sample, and further comprising the steps of:

(k) after steps (c) through (f), positioning the film sample so that the first and second beamlets of the irradiation beam pulses impinge on at a first location outside of boundaries of the film sample with respect to the film sample; and

(l) after step (k), positioning the film sample so that the successive impingement of the first and second beamlets with respect to the film sample moves from the first location to a second location, the second location being outside of the boundaries of the film sample.

8. The method of claim 7, wherein, after steps (c) through (f) and before step (k), a completed portion of the film sample having a predetermined width has been irradiated, melted throughout its entire thickness and re-solidified, the film sample having a controlled crystalline grain growth in the entire cross-section of the completed portion.

9. The method of claim 8,

wherein the particular direction extends along a first axis,

wherein, in step (l), the film sample is translated along a second axis, the first axis being perpendicular to the first axis, and

wherein the second location is provided at the distance from the first location approximately equal to the predetermined width.

10. The method of claim 9, further comprising the steps of:

(m) after step (l), continuously scanning, at the constant predetermined speed, the film sample so that the successive impingement of the first and second beamlets of the irradiation beam pulses occurs in a further direction on the film sample between the second edge and the first edge, the further direction being opposite to the scanning direction; and

(n) during step (m), successively irradiating a plurality of fifth areas of the film sample with the second beamlets of the irradiation beam pulses so that the fifth areas are melted throughout their thickness and leaving additional unirradiated regions between respective adjacent ones of the fifth areas;

(o) during step (m), allowing each one of the fifth areas irradiated by the second beamlets of each of the irradiation beam pulses to re-solidify and crystalize; and

(p) during step (o), successively irradiating a plurality of sixth areas of the film sample by the first beamlets of the irradiation beam pulses so that the sixth areas are melted throughout their thickness, wherein each one of the sixth areas partially overlaps a respective pair of the re-solidified and crystalized fifth areas and the respective additional unirradiated region therebetween.

11. The method of claim 1, wherein steps (a) through (f) are performed without executing any microtranslation of the impingement of the first and second beamlets of the irradiation beam pulses with respect to the film sample.

12. The method of claim 1, further comprising the steps of:

(q) during step (g), allowing each one of the second areas irradiated by the first beamlets of each of the irradiation beam pulses to re-solidify and crystalize;

(r) masking portions of the irradiation beam pulses to emit successive partial intensity irradiation pulse which have a reduced intensity so that when the

successive partial intensity irradiation pulses irradiate a particular region of the film sample, the particular region is melted for less than the entire thickness of the film sample;

(s) after steps (q) and (r), successively irradiating each of the re-solidified and crystalized second areas by the respective one of the successive partial intensity irradiation pulses.

13. A system for processing a silicon thin film sample on a substrate having a surface portion that does not seed crystal growth in the silicon thin film, the film sample having a first edge and a second edge, the system comprising:

a memory storing a computer program; and

a processing arrangement executing the computer program to perform the following steps:

(a) controlling an irradiation beam generator to emit successive irradiation beam pulses at a predetermined repetition rate,

(b) masking each of the irradiation beam pulses to define a first plurality of beamlets and a second plurality of beamlets, the first and second plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to melt irradiated portions of the film sample throughout their entire thickness,

(c) continuously scanning, at a constant predetermined speed, the film sample so that a successive impingement of the first and second beamlets of the irradiation beam pulses occurs in a scanning direction on the film sample between the first edge and the second edge,

(d) during step (c), successively irradiating a plurality of first areas of the film sample using the first beamlets of the irradiation beam pulses so that the first areas are melted throughout their thickness and leaving unirradiated regions between respective adjacent ones of the first areas,

(e) during step (c), allowing each one of the first areas irradiated using the first beamlets of each of the irradiation beam pulses to re-solidify and crystalize, and

(f) during step (e), successively irradiating a plurality of second areas of the film sample using the second beamlets of the irradiation beam pulses so that the second areas are melted throughout their thickness, wherein each one of the second areas partially overlaps a respective pair of the re-solidified and crystalized first areas and the respective unirradiated region therebetween.

14. The system of claim 13, wherein, during step (f), the processing arrangement successively irradiates third areas of the film sample using the first beamlets to completely melt the third areas throughout their thickness, each of the third areas partially overlapping a respective one of the re-solidified and crystalized first areas and leaving further unirradiated regions between respective adjacent ones of the third areas.

15. The system of claim 14,
wherein one of the first areas and one of the third areas lie on a first line which is parallel to the scanning direction,
wherein one of the second areas lies of a second line which is parallel to the scanning direction, and
wherein the first line extends at an offset from the second line.

16. The system of claim 14, wherein, after the third areas are being irradiated by the first beamlets, each one of the second areas irradiated using the first beamlets of each of the irradiation beam pulses is allowed to re-solidify and crystalize.

17. The system of claim 16,

wherein, during step (c), each one of the third areas irradiated using the first beamlets of each of the irradiation beam pulses is allowed to re-solidify and crystalize, and

wherein, after the second and third areas re-solidify and crystalize, the processing arrangement successively irradiates a plurality of fourth areas of the film sample using the second beamlets of the irradiation beam pulses so that the fourth areas are melted throughout their thickness, wherein each one of the fourth areas partially overlaps a respective pair of the re-solidified and crystalized third areas and the respective further unirradiated region therebetween.

18. The system of claim 13, wherein the first edge is located on a side of the film sample which is opposite from a side of the film sample on which the second edge is located.

19. The system of claim 18,

wherein the processing arrangement performs steps (c) through (f) until the successive impingement by the first and second beamlets of the irradiation beam pulses the film sample passes the second edge of the film sample,

wherein, after steps (c) through (f), the processing arrangement positions the film sample so that the first and second beamlets of the irradiation beam pulses impinge on at a first location outside of boundaries of the film sample with respect to the film sample, and

wherein, after the irradiation beam pulse impinge on the first location, the processing arrangement positions the film sample so that the successive impingement of the first and second beamlets with respect to the film sample moves from the first location to a second location, the second location being outside of the boundaries of the film sample.

20. The system of claim 19, wherein, after steps (c) through (f) and after the successive impingement of the irradiation beam pulses passes the second edge of

the film sample, a completed portion of the film sample having a predetermined width has been irradiated, melted throughout its entire thickness and re-solidified, the film sample having a controlled crystalline grain growth in the entire cross-section of the completed portion.

21. The system of claim 20,
wherein the particular direction extends along a first axis,
wherein the processing arrangement translates the successive impingement from the first location to the second location with respect to the film sample along a second axis, the first axis being perpendicular to the first axis, and
wherein the second location is provided at the distance from the first location approximately equal to the predetermined width.

22. The system of claim 21, wherein the processing arrangement performs the following further steps:

(g) after the successive impingement is translated from the first location to the second location, continuously scanning, at the constant predetermined speed, the film sample so that the successive impingement of the first and second beamlets of the irradiation beam pulses occurs in a further direction on the film sample between the second edge and the first edge, the further direction being opposite to the scanning direction, and

(h) during step (g), successively irradiating a plurality of fifth areas of the film sample with the second beamlets of the irradiation beam pulses so that the fifth areas are melted throughout their thickness and leaving additional unirradiated regions between respective adjacent ones of the fifth areas;

(i) during step (g), allowing each one of the fifth areas irradiated by the second beamlets of each of the irradiation beam pulses to re-solidify and crystalize; and

(j) during step (i), successively irradiating a plurality of sixth areas of the film sample by the first beamlets of the irradiation beam pulses so that the

sixth areas are melted throughout their thickness, wherein each one of the sixth areas partially overlaps a respective pair of the re-solidified and crystalized fifth areas and the respective additional unirradiated region therebetween.

23. The system of claim 13, wherein the processing arrangement performs steps (a) through (f) without executing any microtranslation of the impingement of the first and second beamlets of the irradiation beam pulses with respect to the film sample.

24. The system of claim 13, wherein the processing arrangement performs the following further steps:

(k) after the first beamlets successively irradiate the third areas, allowing each one of the second areas irradiated by the first beamlets of each of the irradiation beam pulses to re-solidify and crystalize,

(l) masking portions of the irradiation beam pulses to emit successive partial intensity irradiation pulse which have a reduced intensity so that when the successive partial intensity irradiation pulses irradiate a particular region of the film sample, the particular region is melted for less than the entire thickness of the film sample,

(m) after steps (k) and (l), successively irradiating each of the re-solidified and crystalized second areas by the respective one of the successive partial intensity irradiation pulses.

25. A method for processing a silicon thin film sample on a substrate having a surface portion that does not seed crystal growth in the silicon thin film, the film sample having a first edge and a second edge, the method comprising the steps of:

(a) controlling an irradiation beam generator to emit successive irradiation beam pulses at a predetermined repetition rate;

(b) masking each of the irradiation beam pulses to define a first plurality of beamlets and a second plurality of beamlets, the first and second plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to melt irradiated portions of the film sample throughout their entire thickness;

(c) continuously scanning, at a constant predetermined speed, the film sample so that a successive impingement of the first and second beamlets of the irradiation beam pulses occurs in a scanning direction on the film sample between the first edge and the second edge;

(d) during step (c), successively irradiating a plurality of first areas of the film sample by the first beamlets of the irradiation beam pulses so that the first areas are melted throughout their thickness and leaving unirradiated regions adjacent to the first areas, each of the first areas having a border with a first width, the border extending along a first line which is perpendicular to the scanning direction;

(e) during step (c), allowing each one of the first areas irradiated by the first beamlets of each of the irradiation beam pulses to re-solidify and crystalize; and

(f) during step (e), successively irradiating a plurality of second areas of the film sample by the second beamlets of the irradiation beam pulses so that the second areas are melted throughout their thickness, wherein a first region of each one of the second areas completely overlaps at least one of the re-solidified and crystalized first areas, and a second region of the respective one of the second areas overlaps the unirradiated region provided adjacent to the at least one of the re-solidified and crystalized first areas, the first region having a second border extending along a second line which is parallel to and offset from the first line, the second width being greater than half of the first width.

26. A system for processing a silicon thin film sample on a substrate having a surface portion that does not seed crystal growth in the silicon thin film, the film sample having a first edge and a second edge, the system comprising:

a memory storing a computer program; and

a processing arrangement executing the computer program to perform the following steps:

(a) controlling an irradiation beam generator to emit successive irradiation beam pulses at a predetermined repetition rate,

(b) masking each of the irradiation beam pulses to define a first plurality of beamlets and a second plurality of beamlets, the first and second plurality of beamlets of each of the irradiation pulses being provided for impinging the film sample and having an intensity which is sufficient to melt irradiated portions of the film sample throughout their entire thickness,

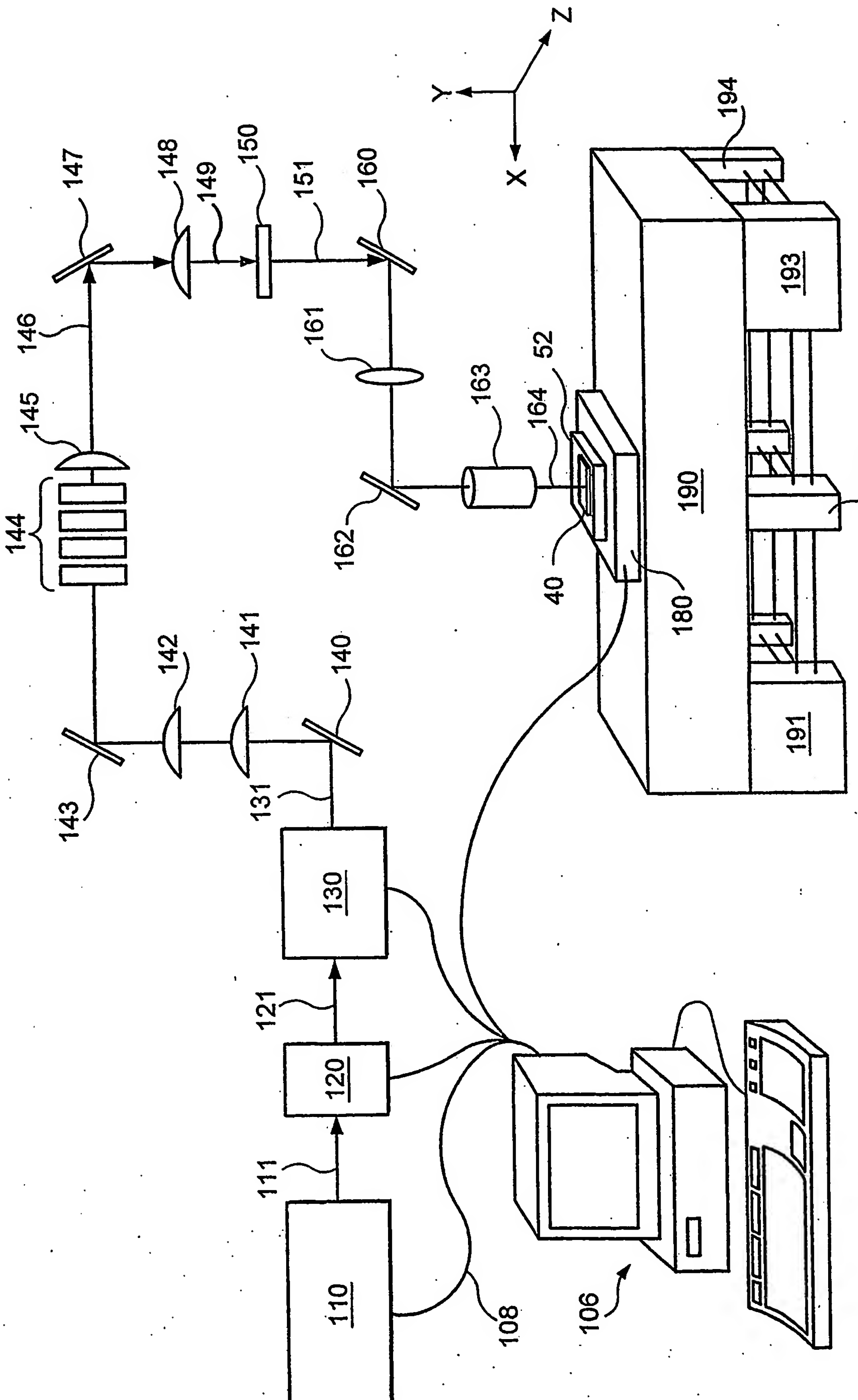
(c) continuously scanning, at a constant predetermined speed, the film sample so that a successive impingement of the first and second beamlets of the irradiation beam pulses occurs in a scanning direction on the film sample between the first edge and the second edge,

(d) during step (c), successively irradiating a plurality of first areas of the film sample by the first beamlets of the irradiation beam pulses so that the first areas are melted throughout their thickness and leaving unirradiated regions adjacent to the first areas, each of the first areas having a border with a first width, the border extending along a first line which is perpendicular to the scanning direction;

(e) during step (c), allowing each one of the first areas irradiated by the first beamlets of each of the irradiation beam pulses to re-solidify and crystalize; and

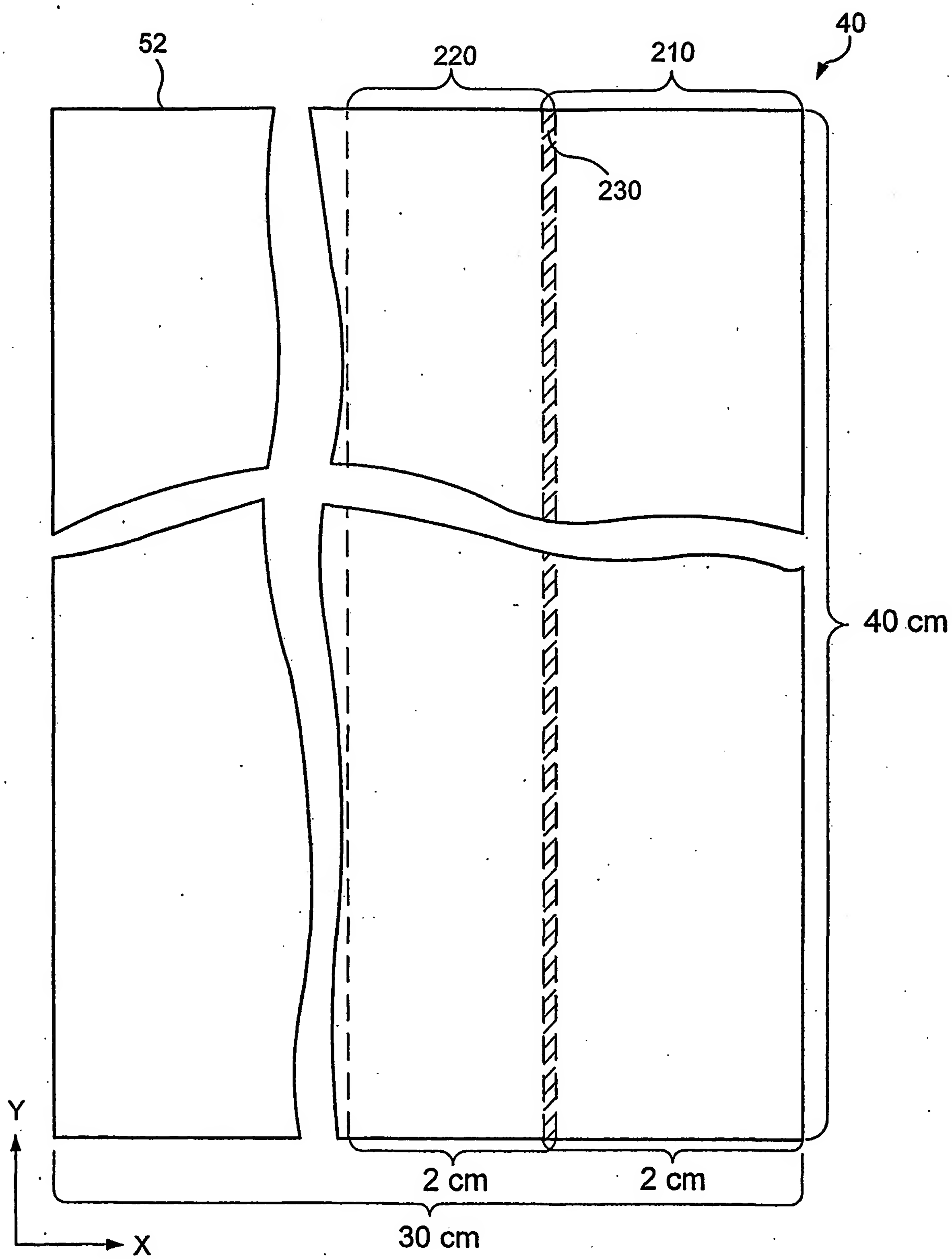
(f) during step (e), successively irradiating a plurality of second areas of the film sample by the second beamlets of the irradiation beam

pulses so that the second areas are melted throughout their thickness, wherein a first region of each one of the second areas completely overlaps at least one of the re-solidified and crystalized first areas, and a second region of the respective one of the second areas overlaps the respective unirradiated region provided adjacent to the at least one of the re-solidified and crystalized first areas, the first region having a second border extending along a second line which is parallel to and offset from the first line, the second width being greater than half of the first width.

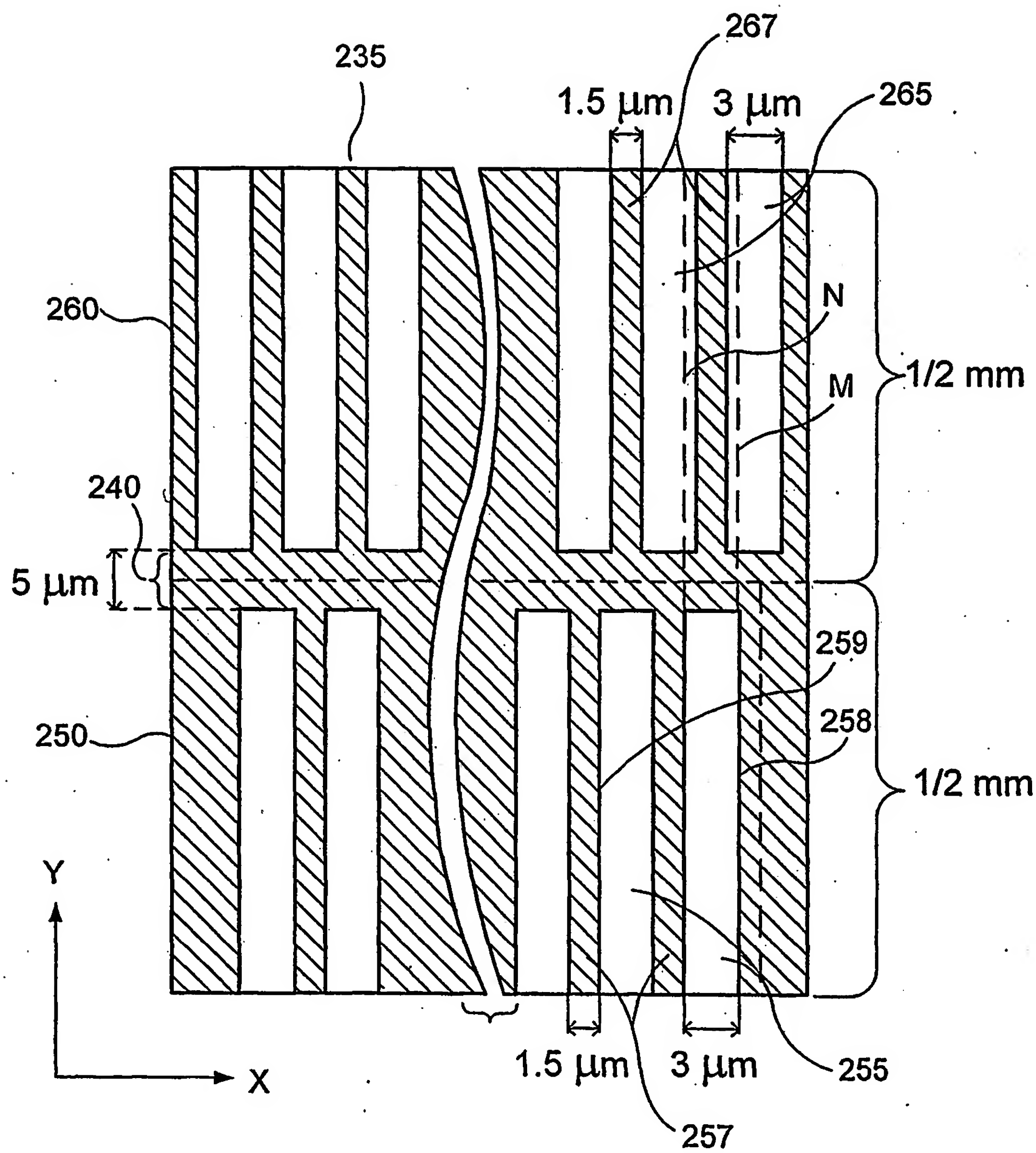


Z
Y
X
110
111
120
121
130
131
140
141
142
143
144
145
146
147
148
149
150
151
160
161
162
163
164
52
40
180
190
191
192
193
194
108
106

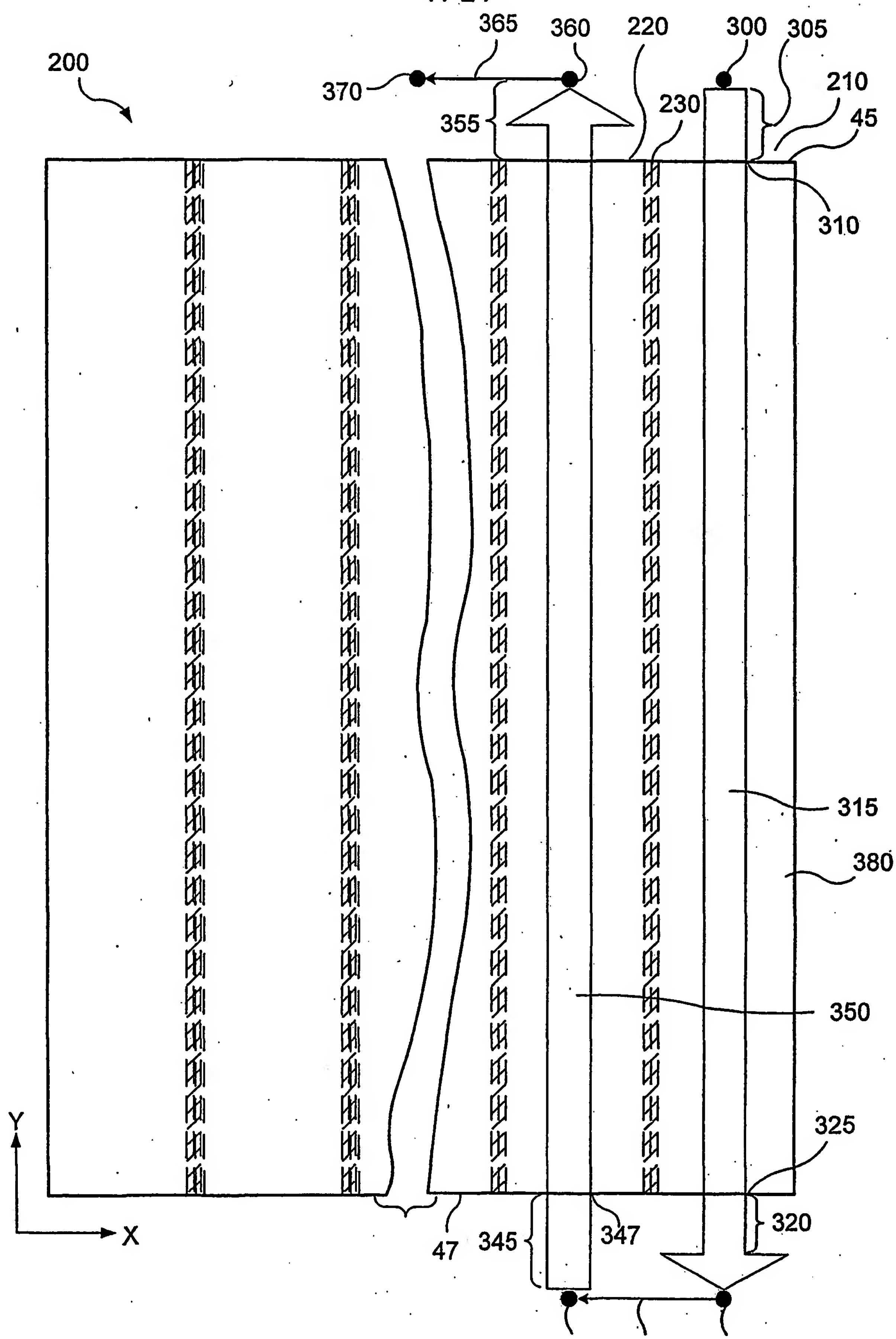
FIG. 1



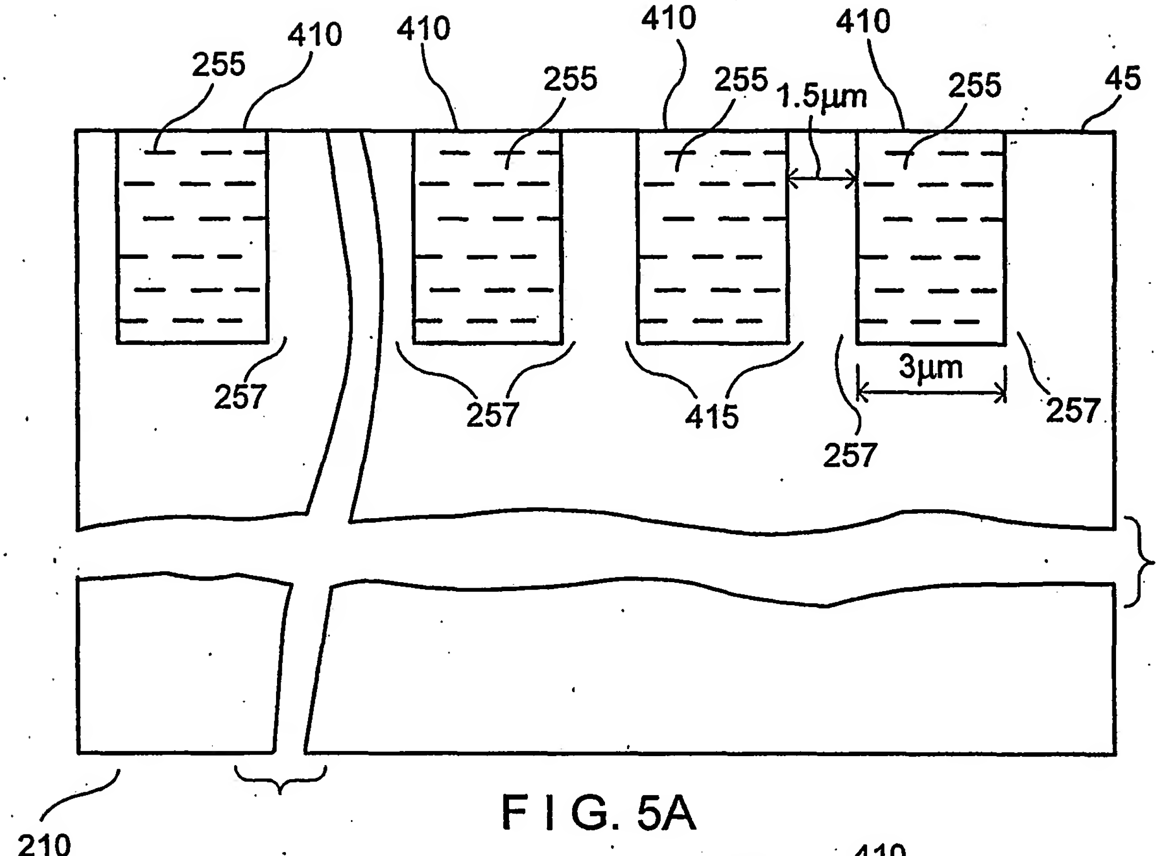
F I G. 2


235
267
1.5 μm
3 μm
265
260
N
M
1/2 mm
240
5 μm
259
250
258
1/2 mm
Y
X
1.5 μm
3 μm
255
257

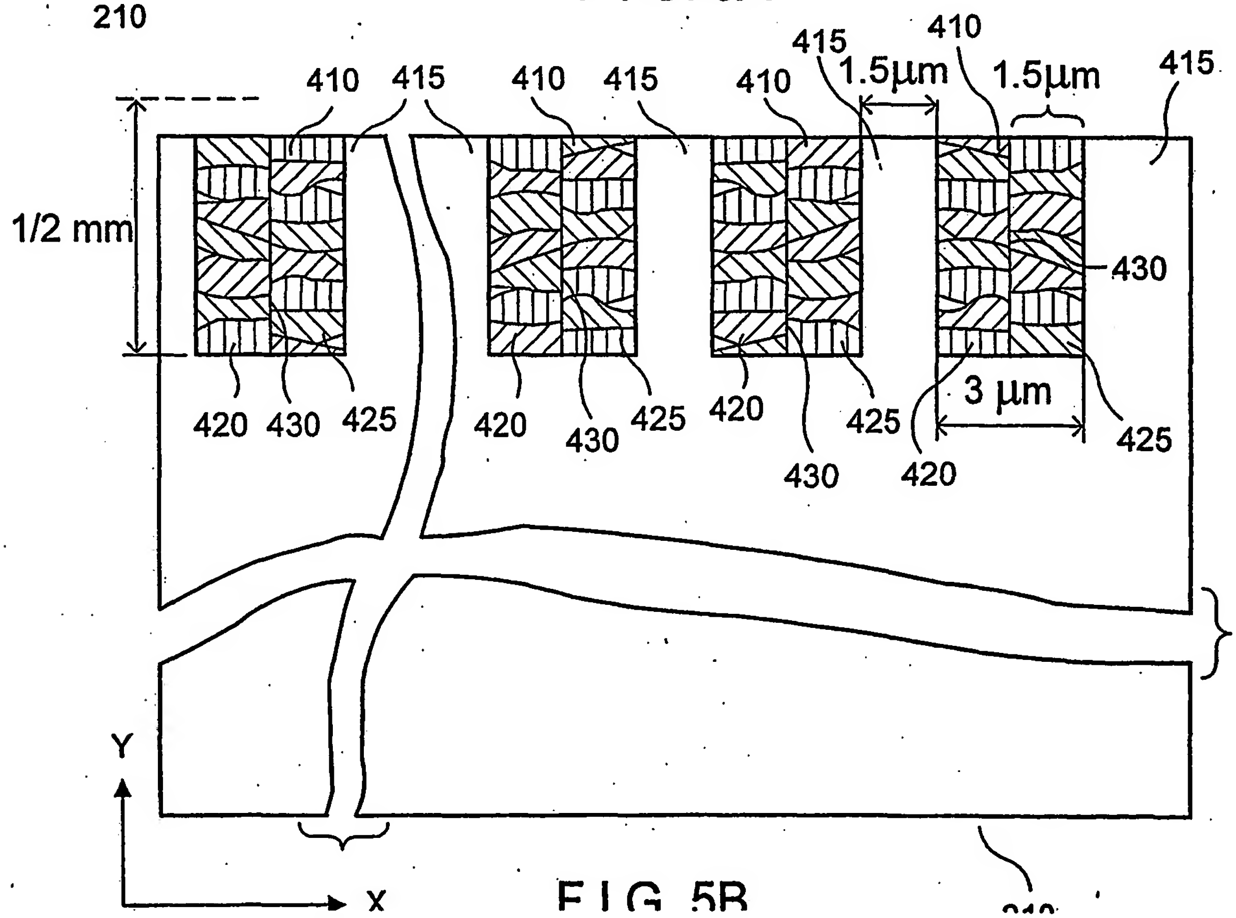
F I G. 3



200
365
360
220
300
305
370
355
230
210
45
310
315
380
350
325
Y
X
47
345
347
320


255
410
410
255
410
255
1.5µm
410
255
45
257
257
415
3µm
257
257
210

F I G. 5A


410
415
410
415
410
415
1.5µm
410
1.5µm
415
1/2 mm
430
420
430
425
420
430
425
420
430
425
420
3 µm
425
Y
X

F I G. 5B

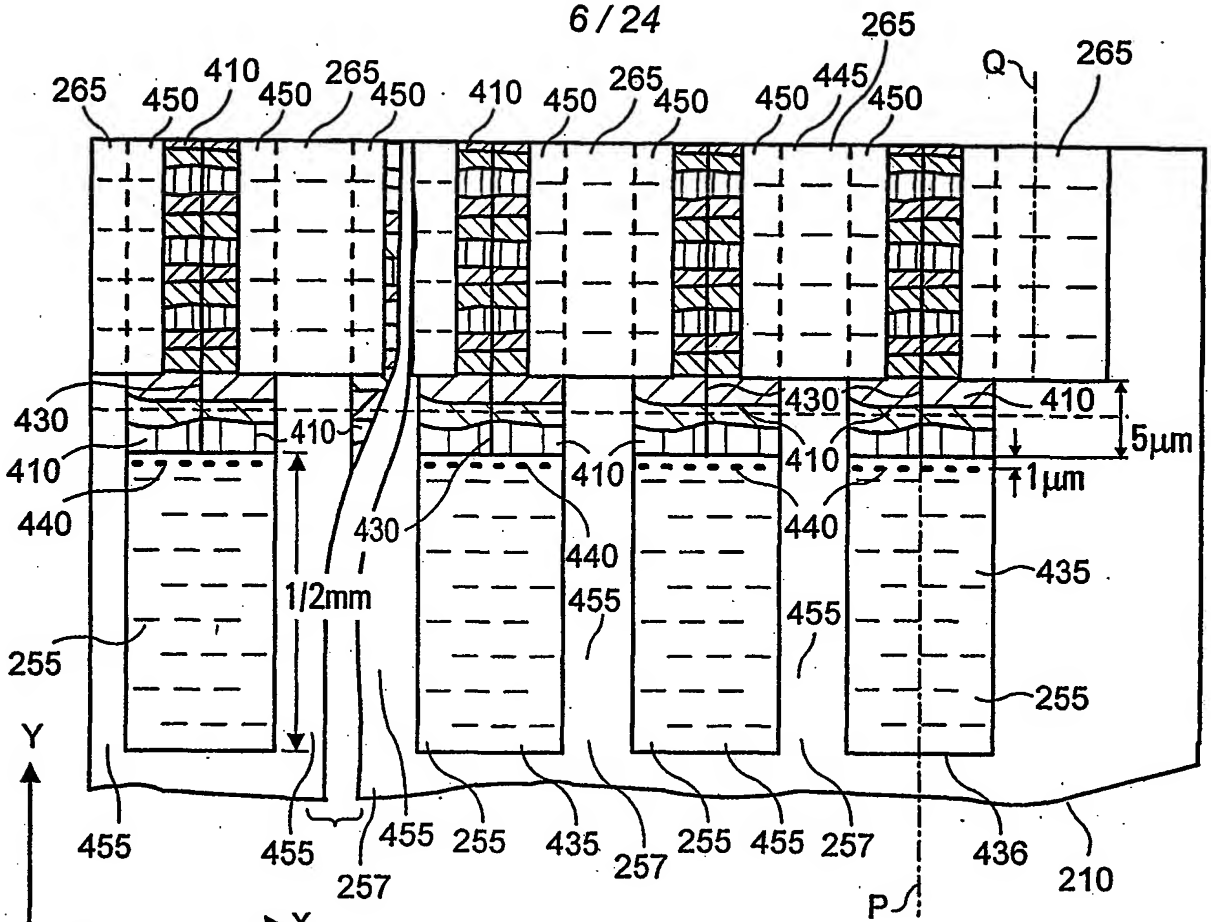
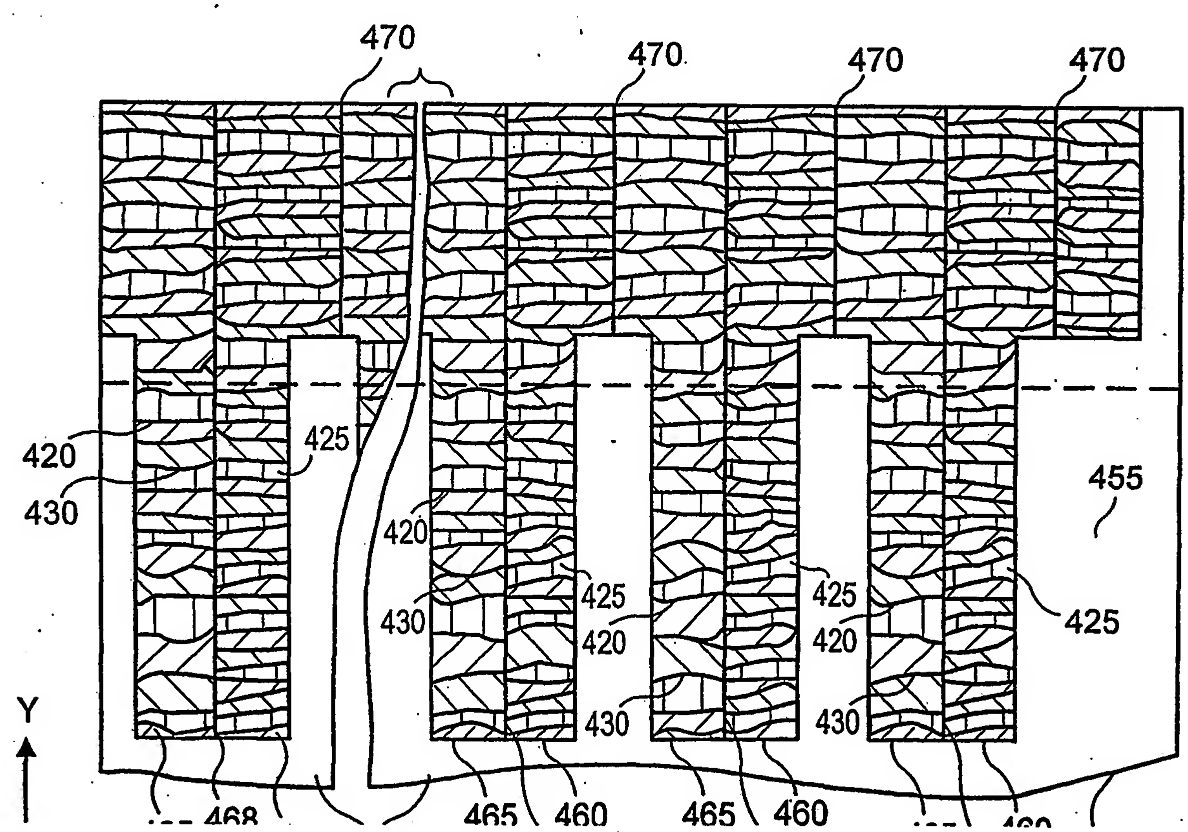
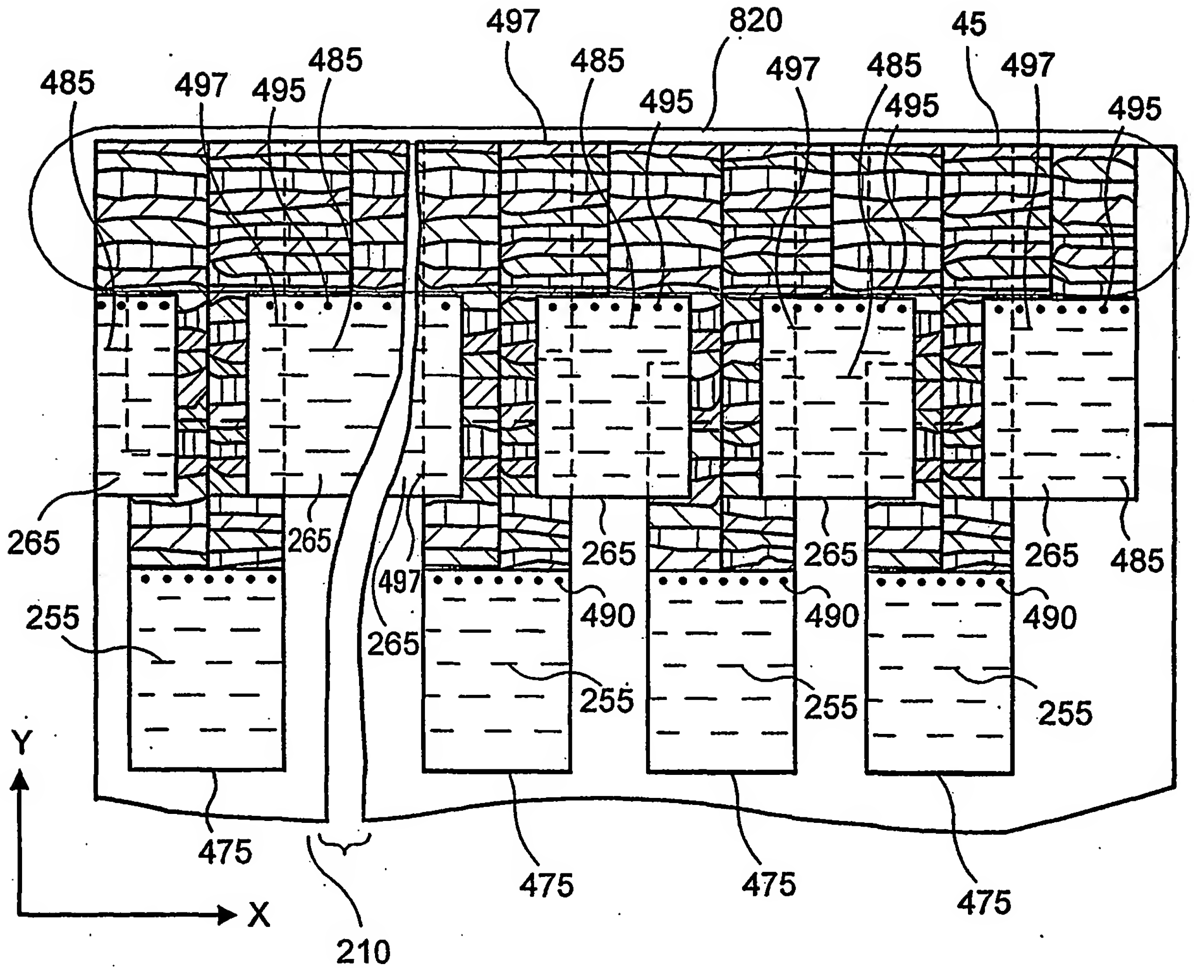

265
450
410
450
265
450
410
450
265
450
450
445
450
265
Q
265
430
410
440
410
430
410
410
430
410
440
440
440
5μm
1μm
1/2mm
435
455
455
255
255
Y
455
455
257
455
255
435
257
255
455
257
436
210
P
X

FIG. 5C


470
470
470
470
420
430
425
455
420
430
425
420
425
420
425
430
430
430
Y
468
465
460
465
460


497
820
45
485
497
495
485
485
495
497
485
495
497
495
265
265
265
265
265
485
497
490
490
490
255
265
255
255
255
Y
X
475
475
475
475
210

F I G. 5E

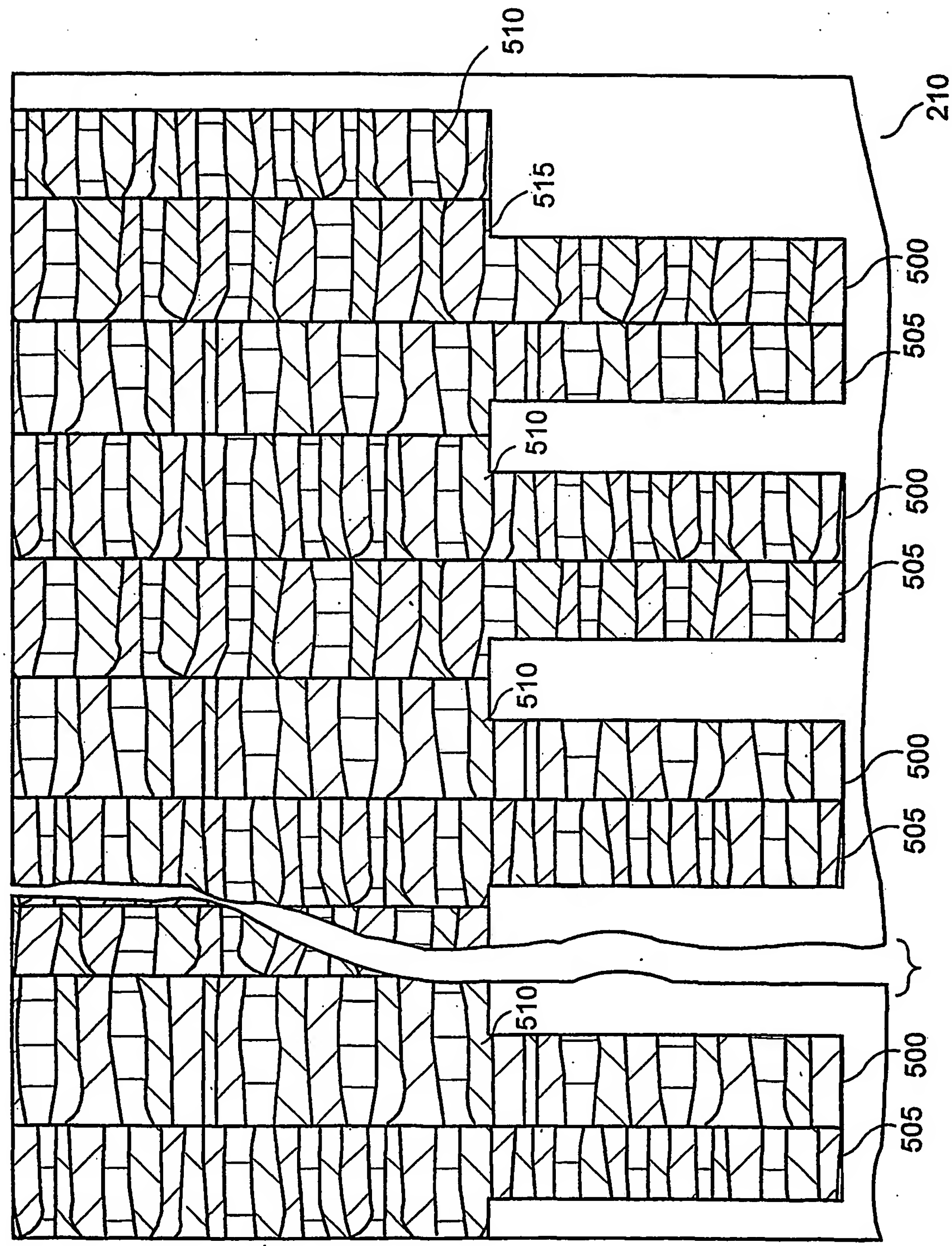


FIG. 5F

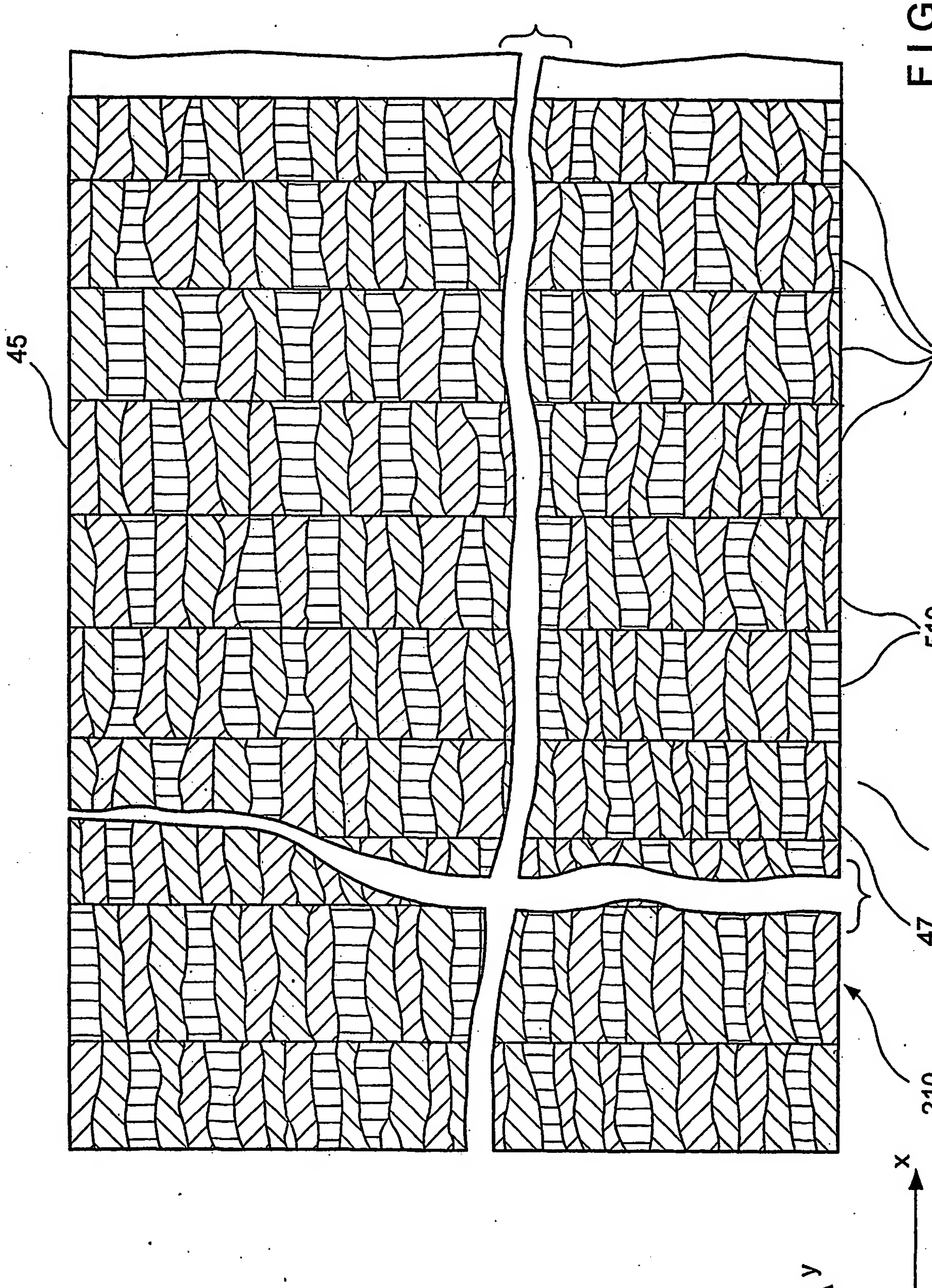


FIG. 5G

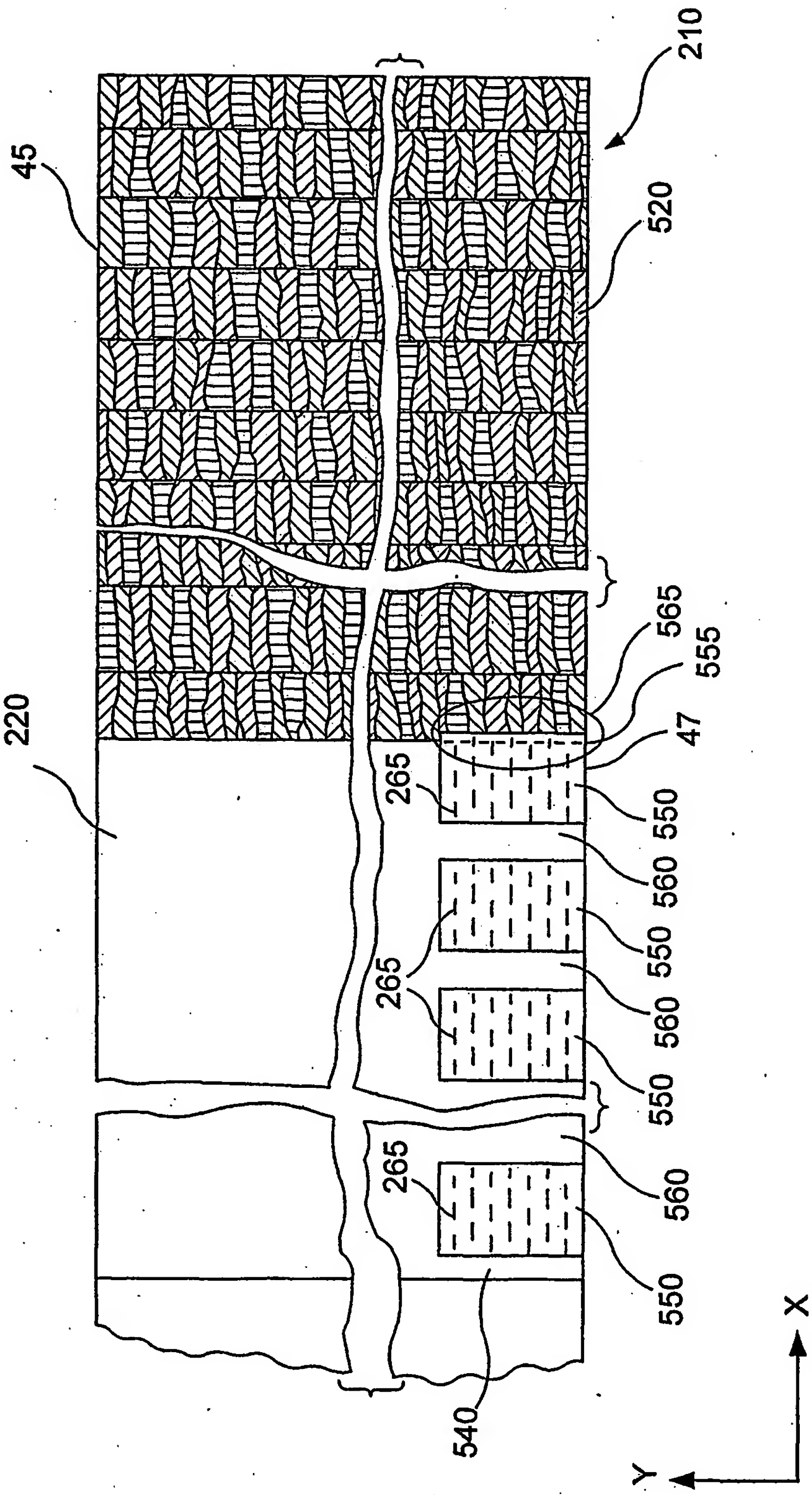

210
45
520
220
565
555
47
265
550
560
265
550
560
550
265
560
550
540
X
Y

FIG. 6A

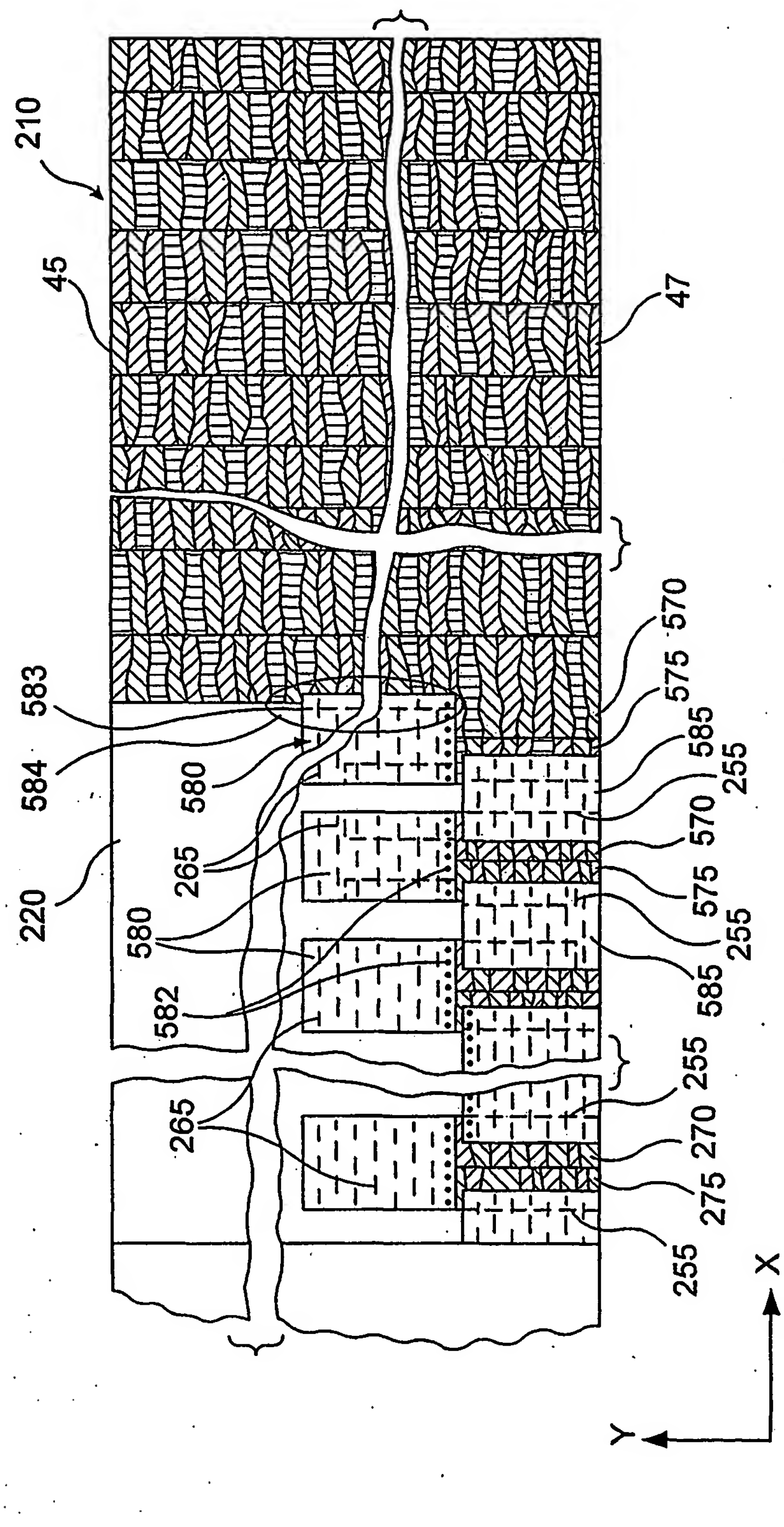

210
45
47
583
584
580
220
265
580
582
265
570
575
585
255
570
575
255
585
255
270
275
255
X
Y

FIG. 6B

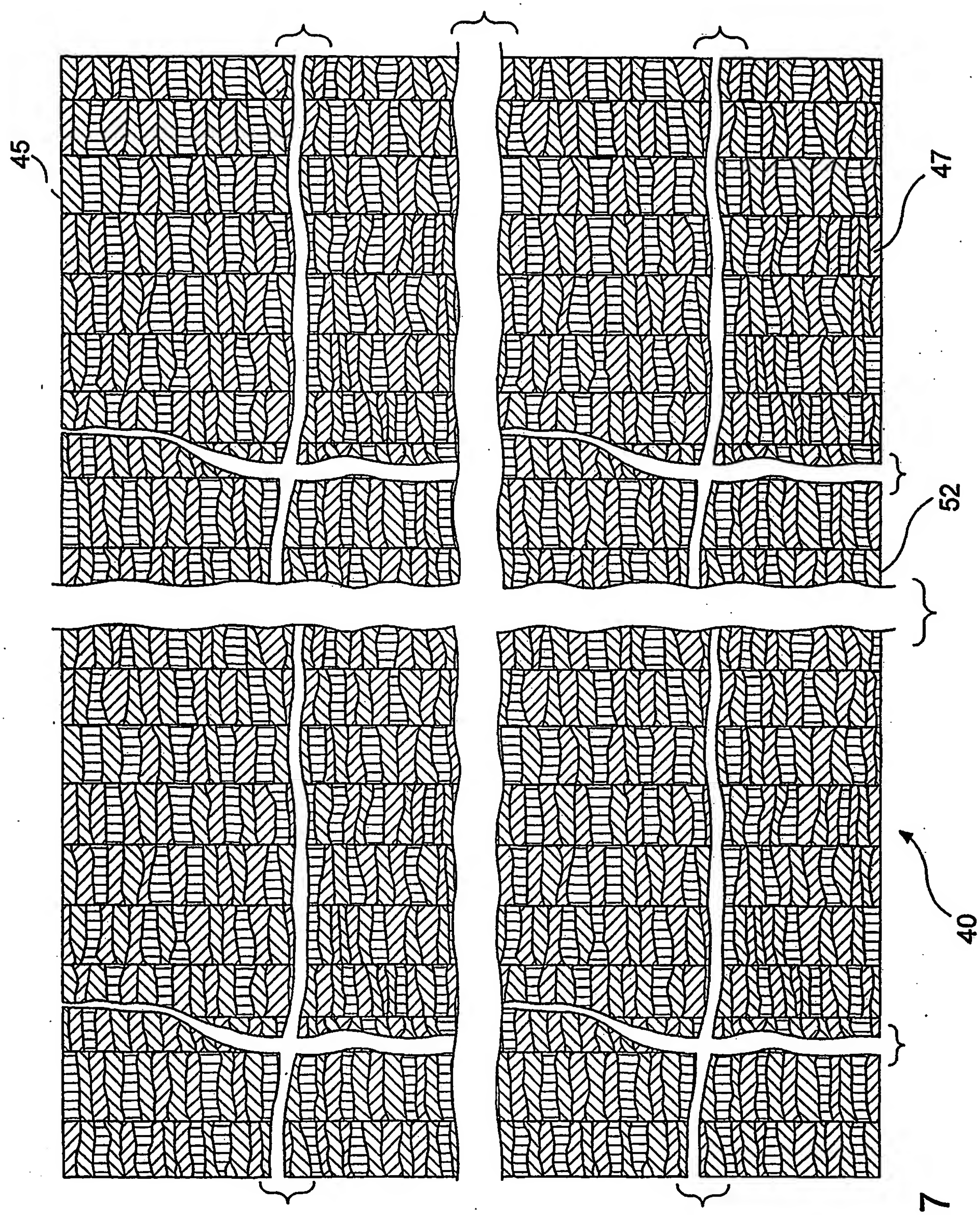


FIG. 7

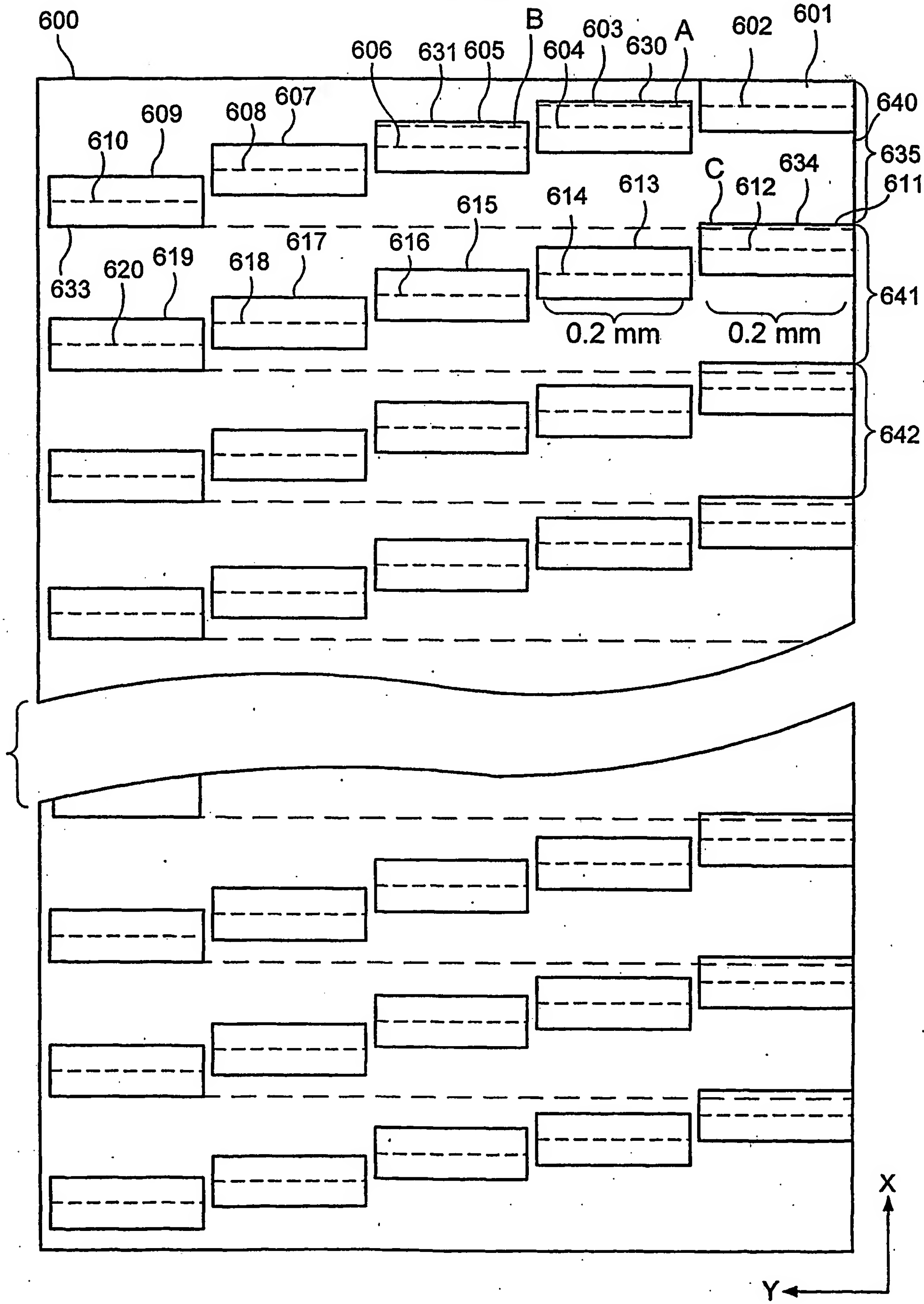
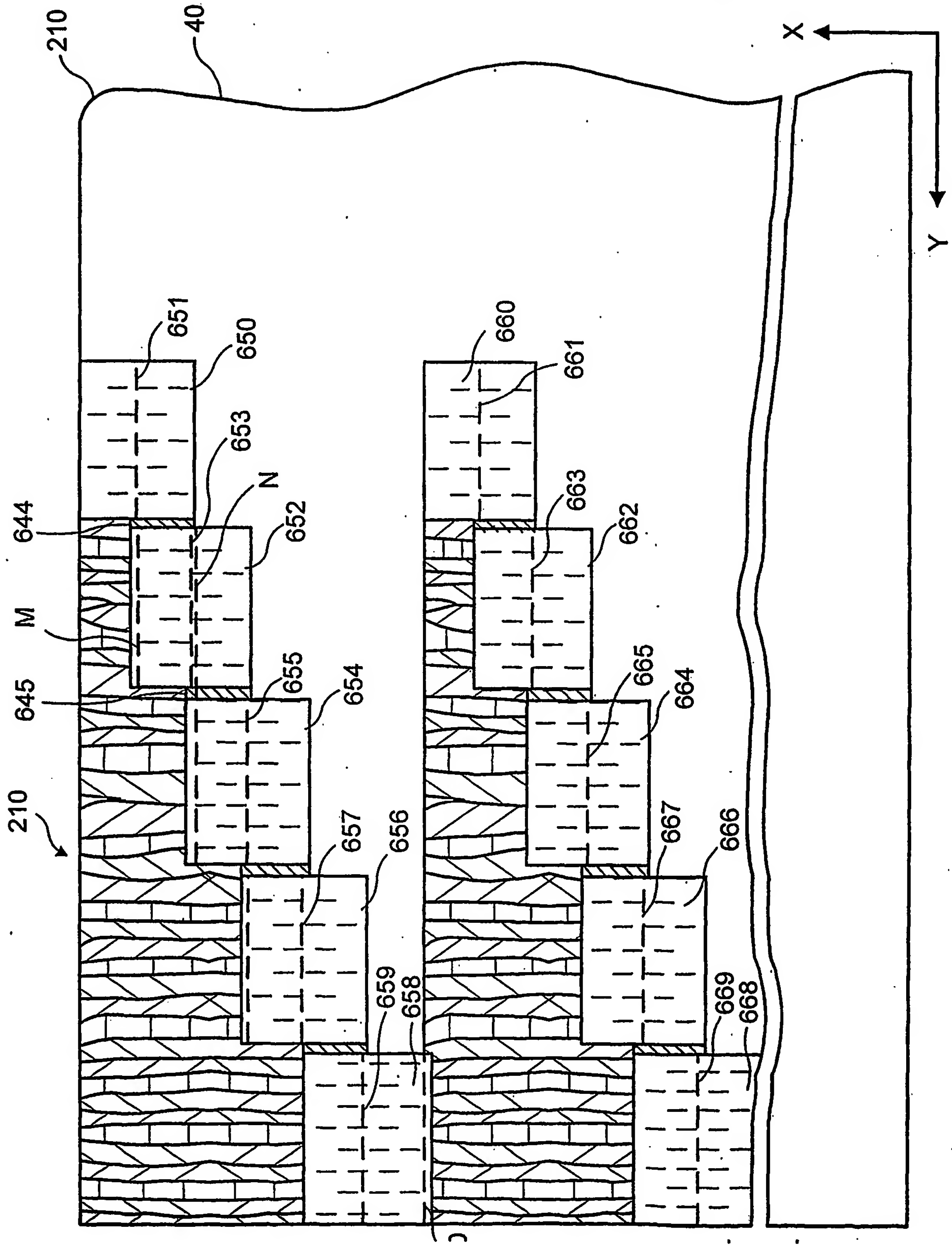

600
606
631
605
B
604
603
630
A
602
601
640
610
609
608
607
635
C
612
634
611
615
614
613
633
620
619
618
617
616
641
0.2 mm
0.2 mm
642
X
Y

FIG. 9


210
40
X
Y
651
650
660
661
653
N
652
644
M
663
662
645
655
654
665
664
210
657
656
667
666
659
658
669
668

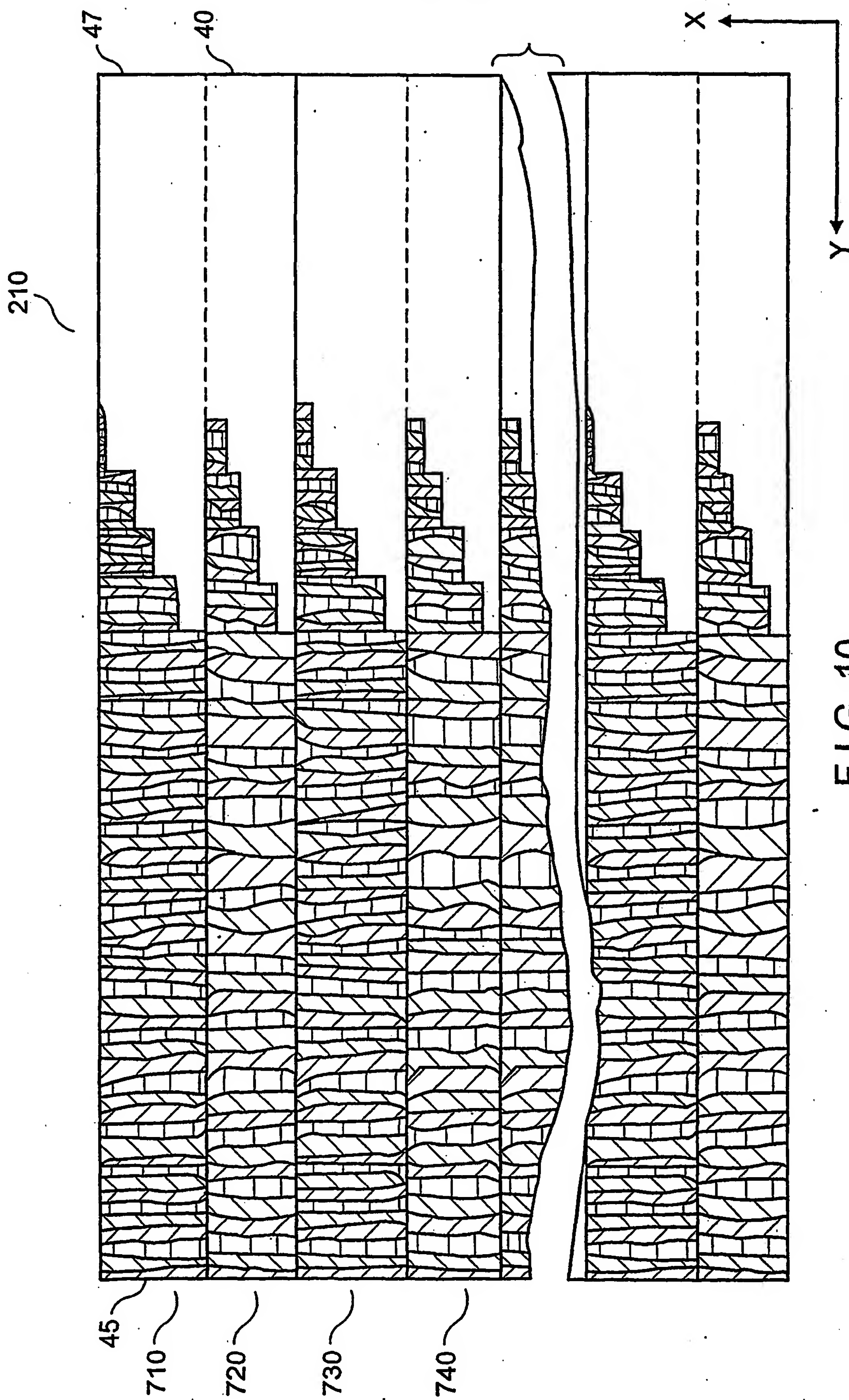
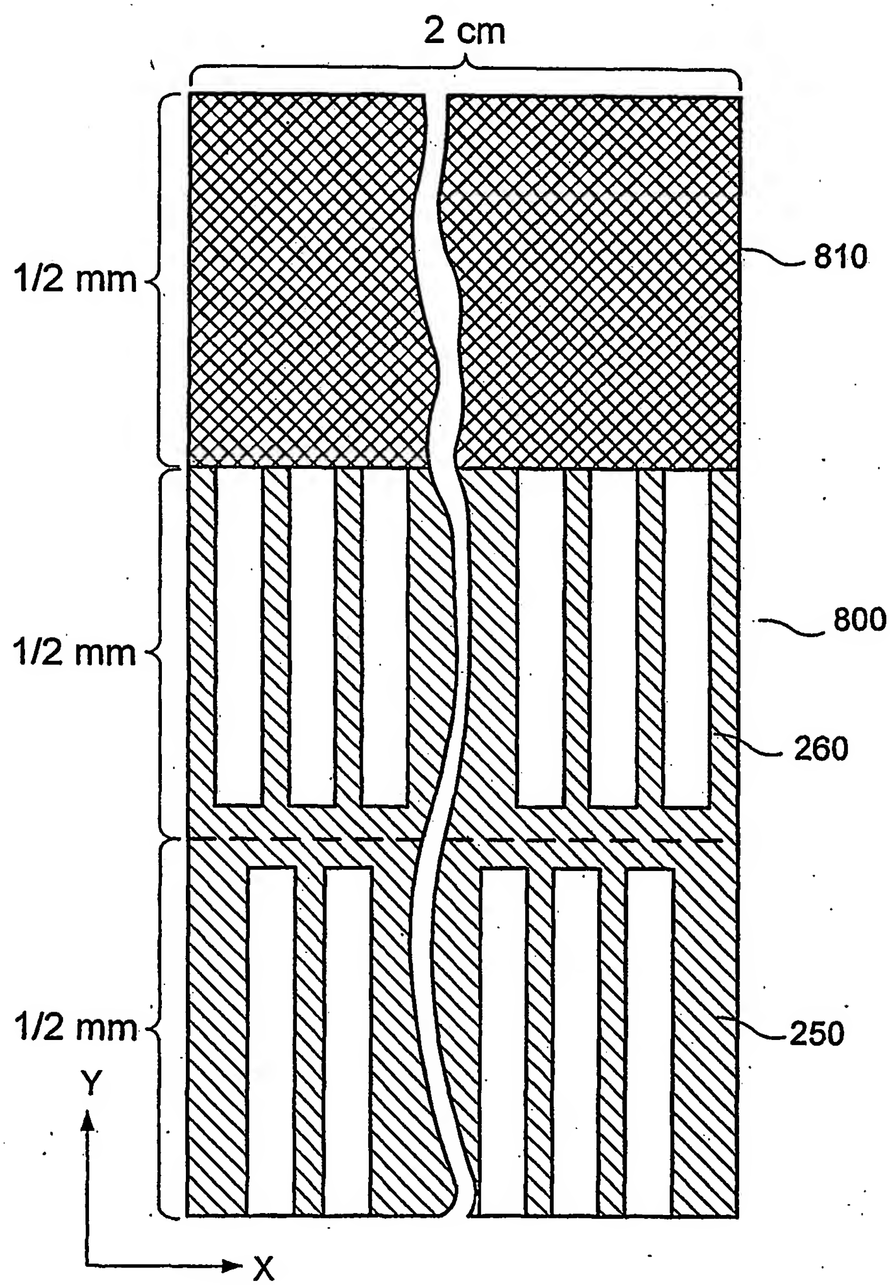


FIG. 10



F I G. 11

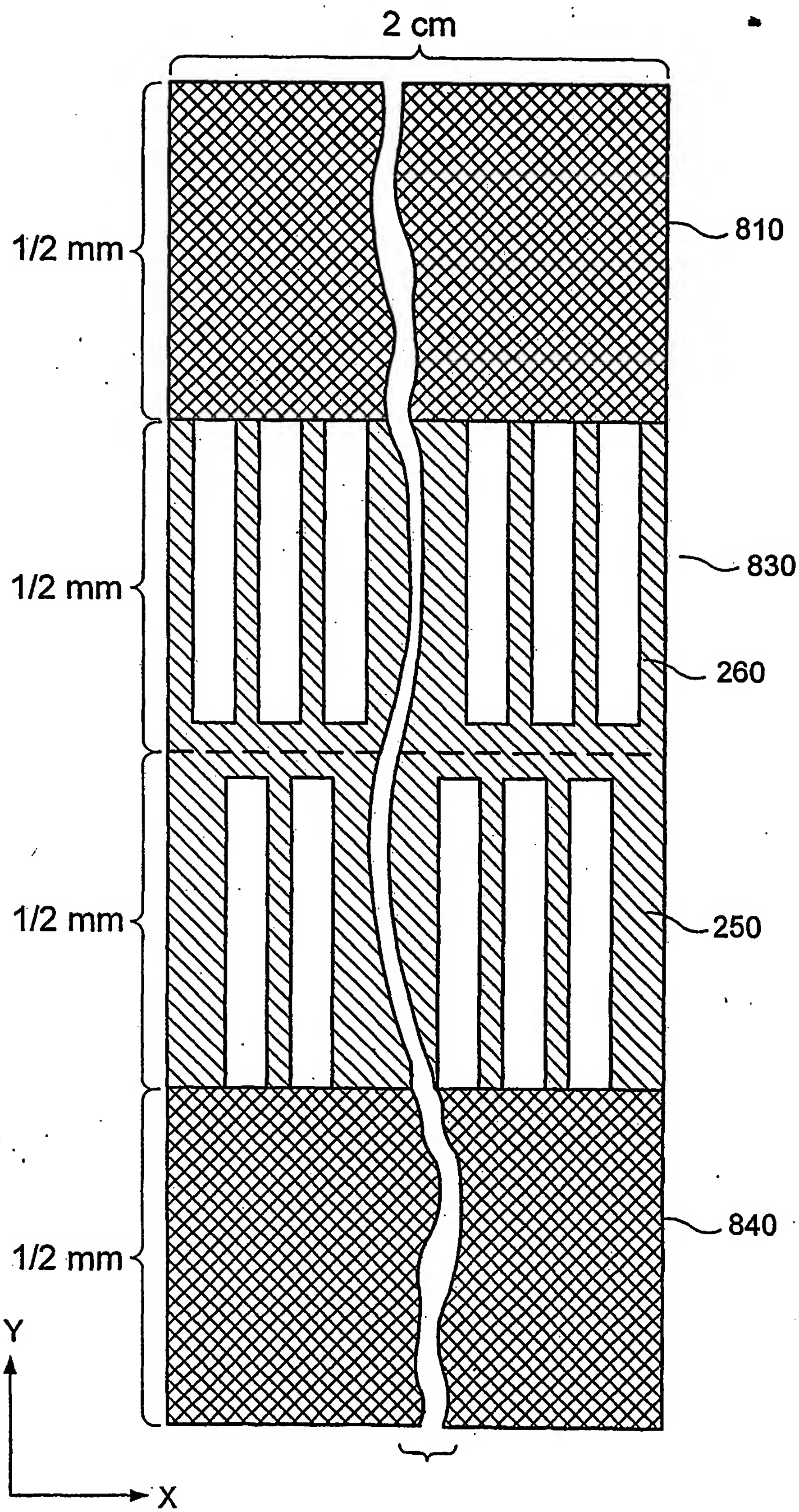


FIG. 12

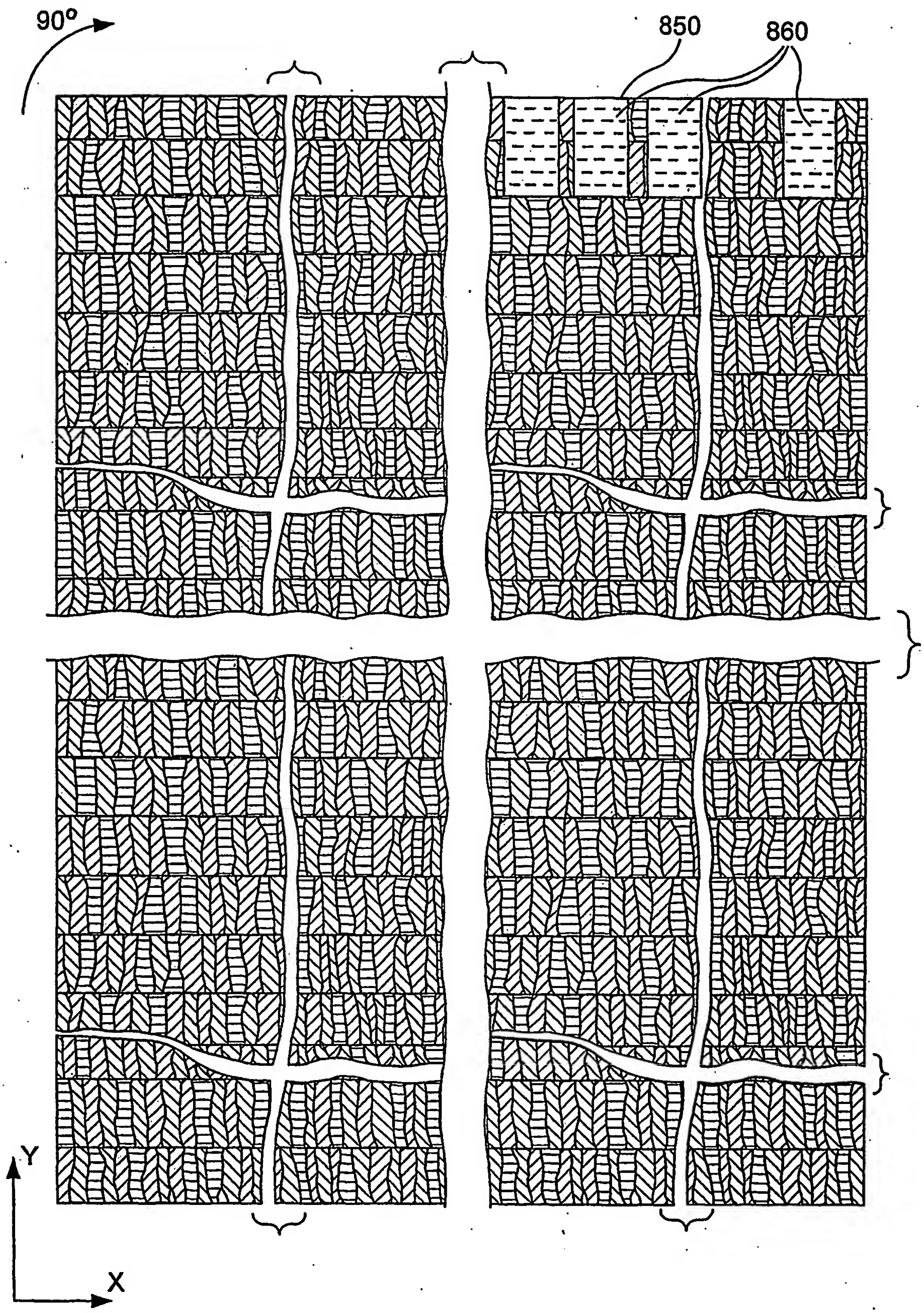
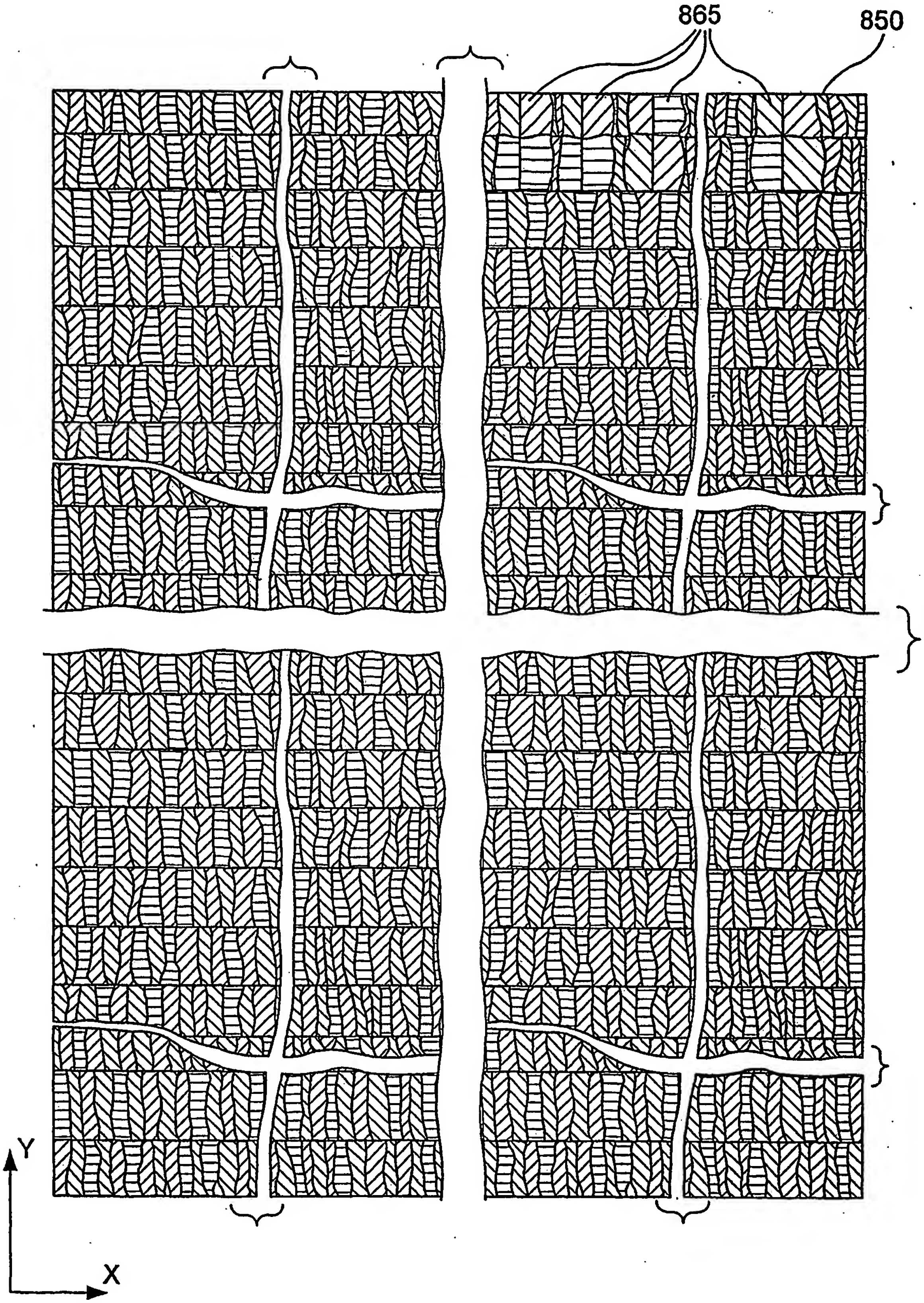
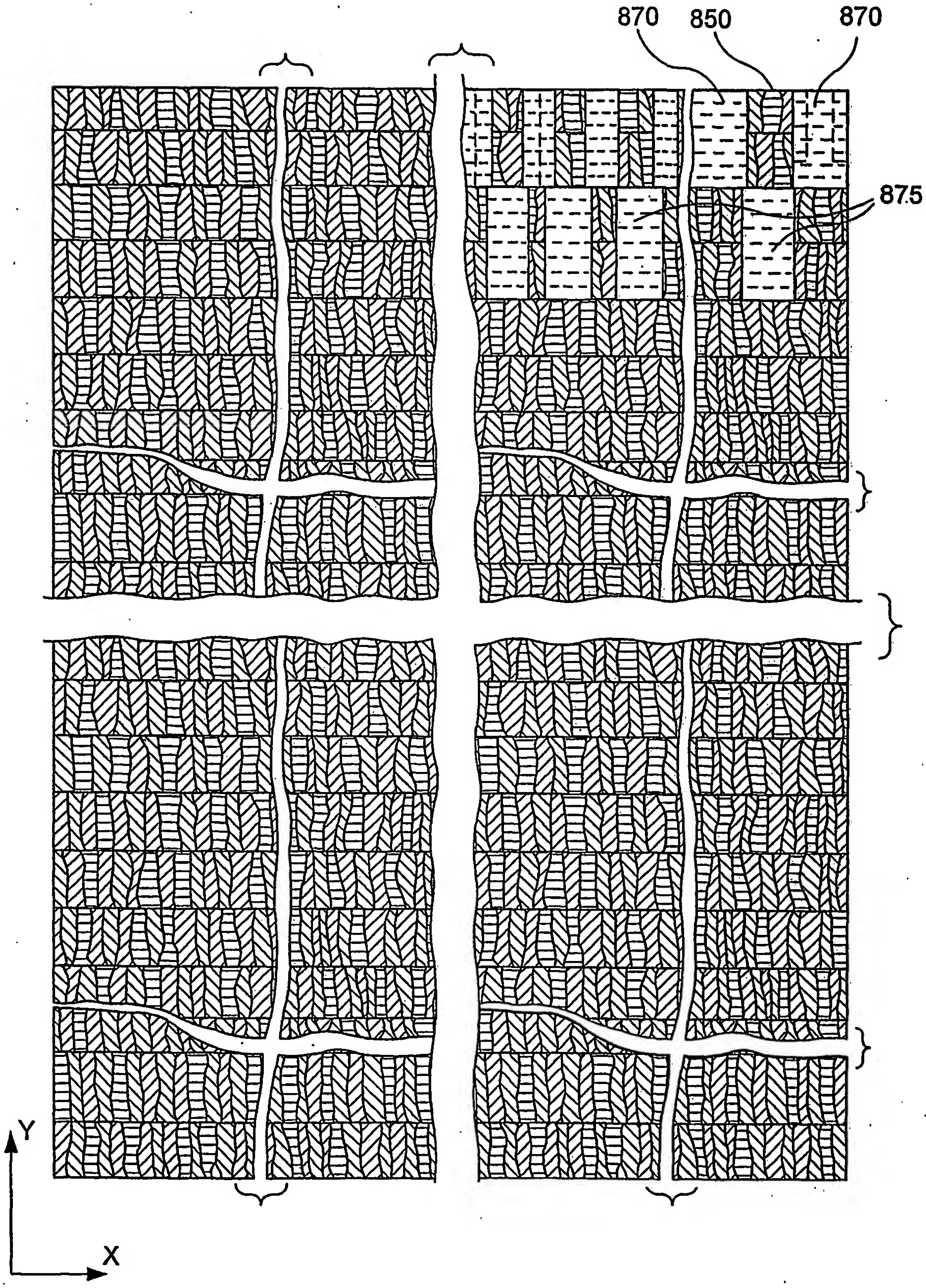


FIG. 13A



F I G. 13B



F I G. 13C

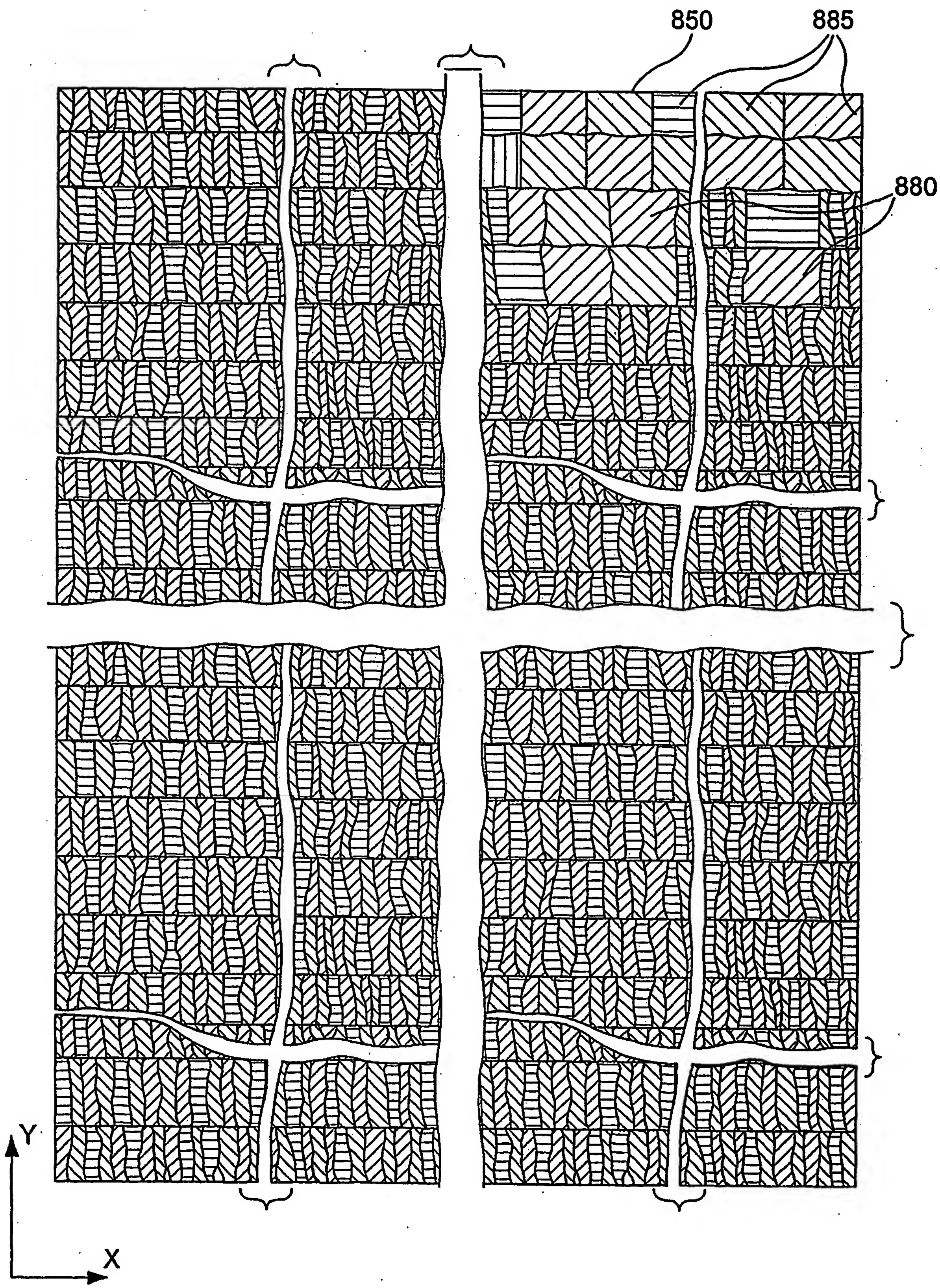


FIG. 13D

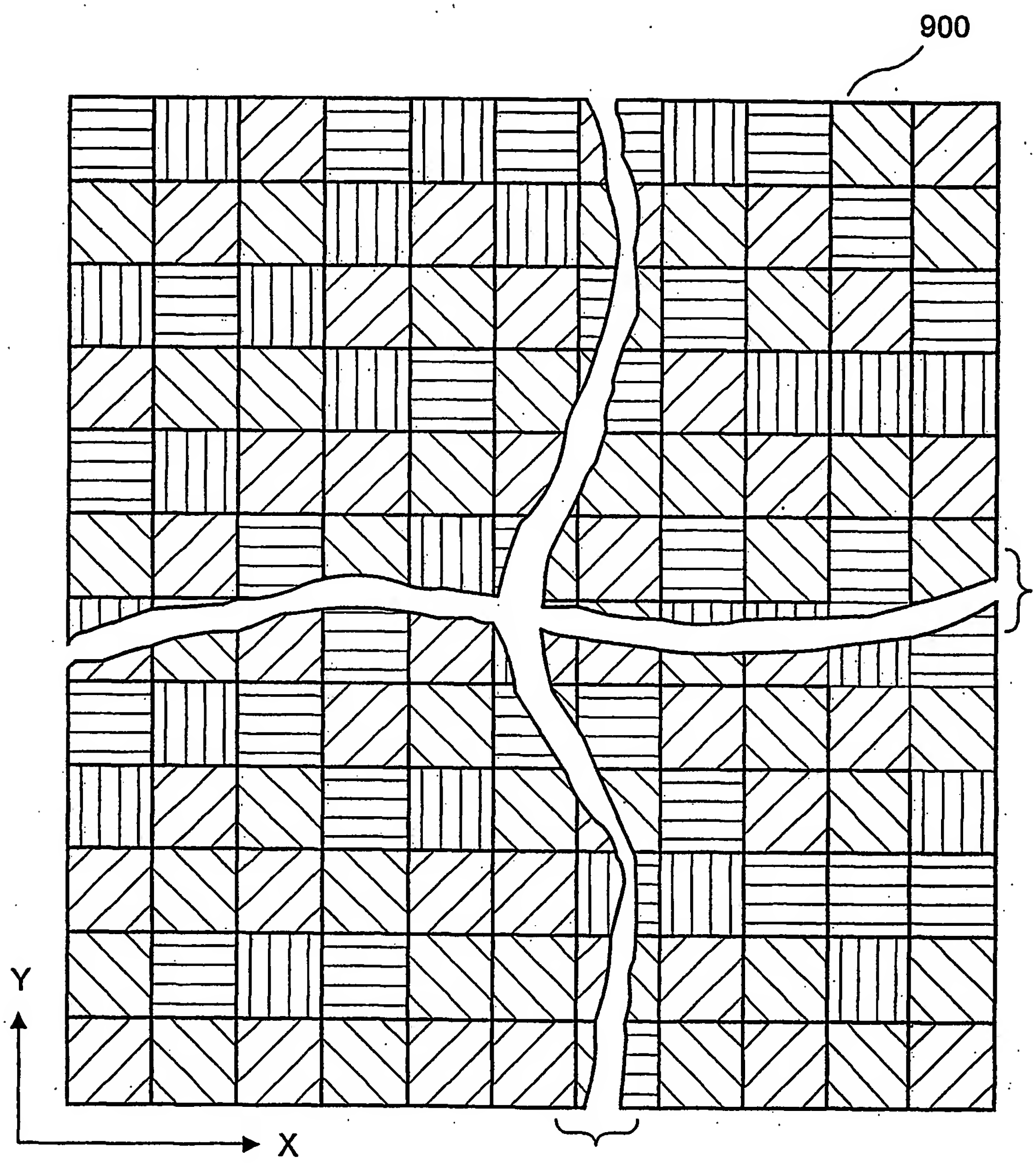
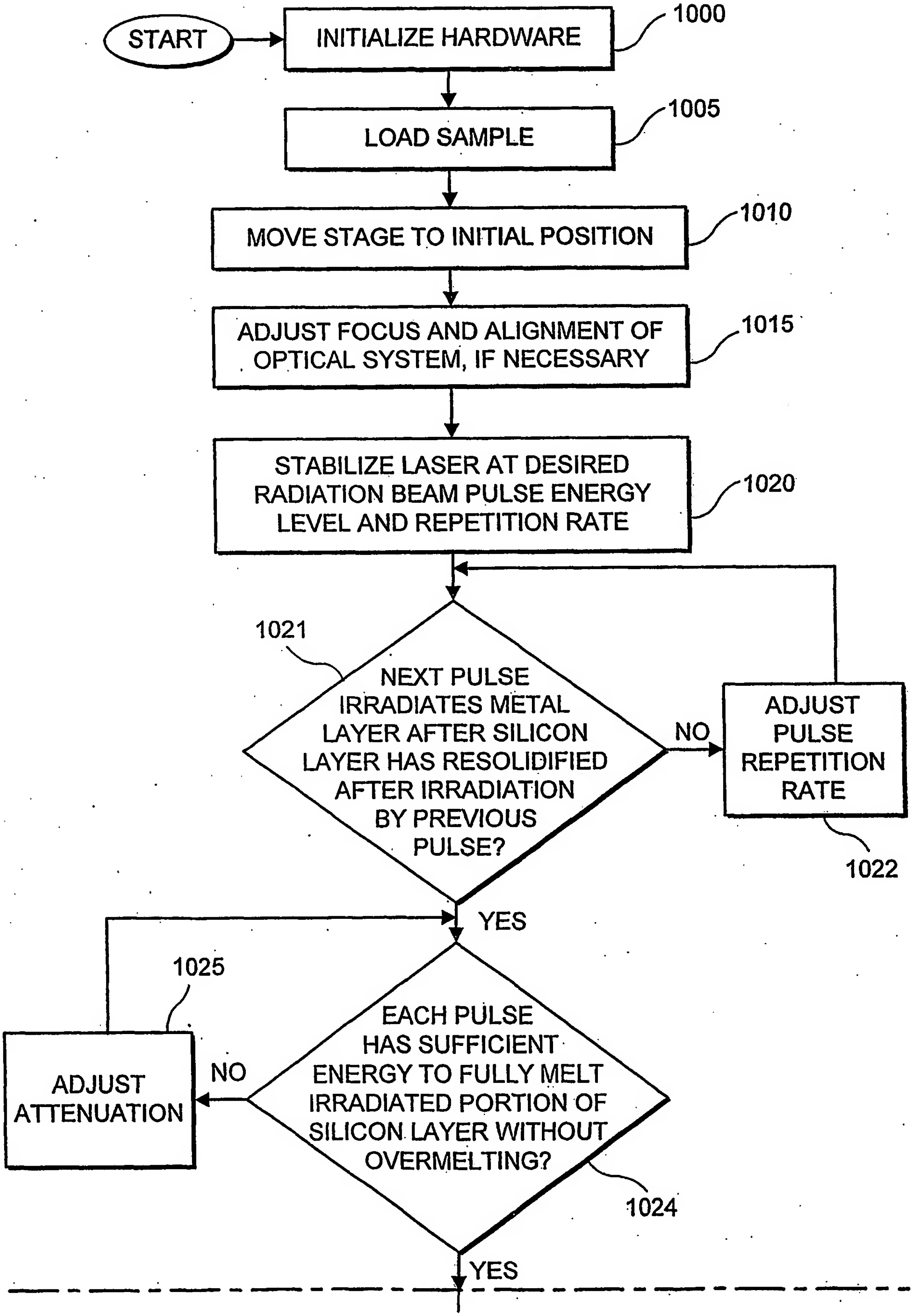
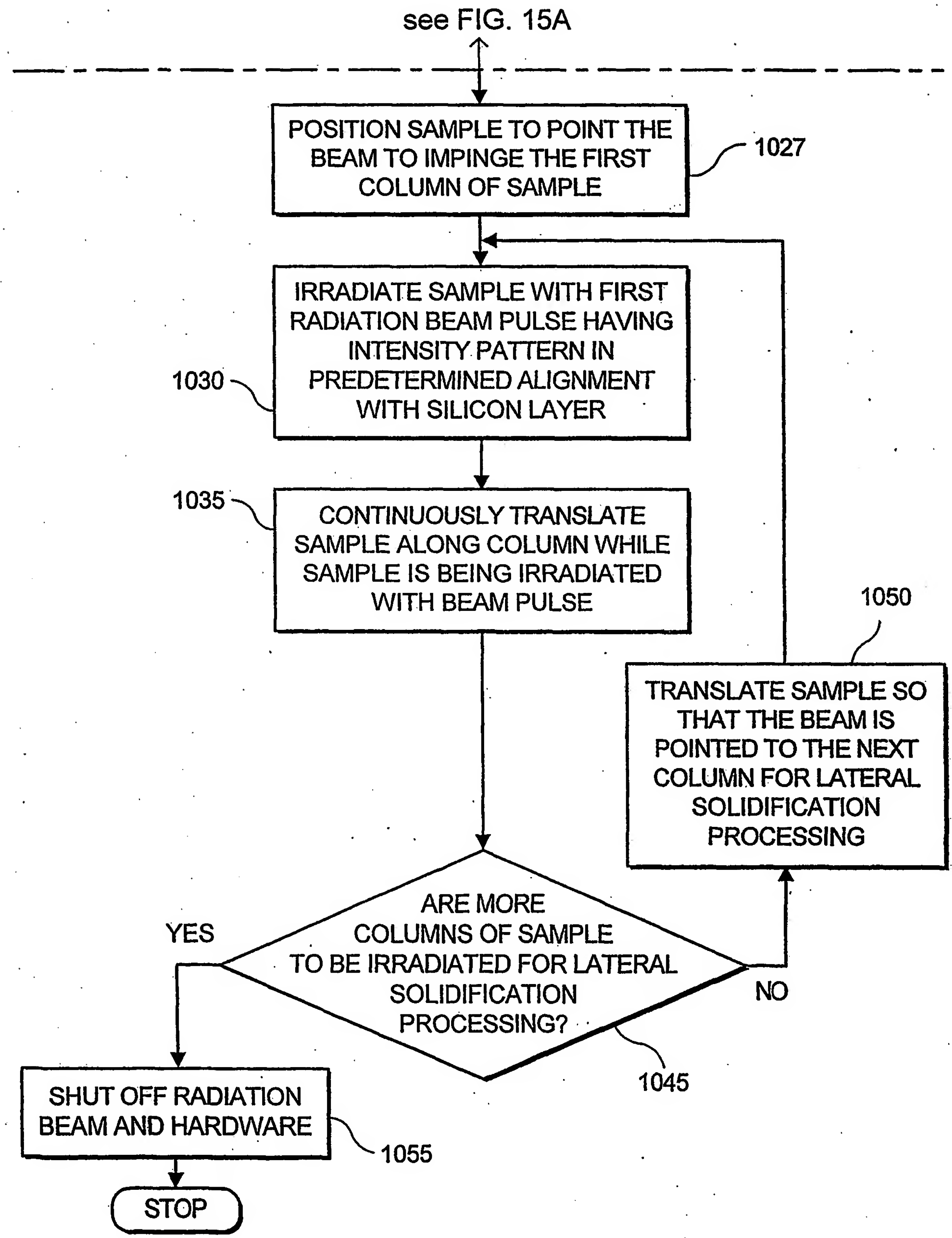


FIG. 14



START
INITIALIZE HARDWARE
1000
LOAD SAMPLE
1005
MOVE STAGE TO INITIAL POSITION
1010
ADJUST FOCUS AND ALIGNMENT OF OPTICAL SYSTEM, IF NECESSARY
1015
STABILIZE LASER AT DESIRED RADIATION BEAM PULSE ENERGY LEVEL AND REPETITION RATE
1020
1021
NEXT PULSE IRRADIATES METAL LAYER AFTER SILICON LAYER HAS RESOLIDIFIED AFTER IRRADIATION BY PREVIOUS PULSE?
NO
ADJUST PULSE REPETITION RATE
1022
YES
1025
ADJUST ATTENUATION
NO
EACH PULSE HAS SUFFICIENT ENERGY TO FULLY MELT IRRADIATED PORTION OF SILICON LAYER WITHOUT OVERMELTING?
1024
YES


see FIG. 15A
POSITION SAMPLE TO POINT THE BEAM TO IMPINGE THE FIRST COLUMN OF SAMPLE
1027
IRRADIATE SAMPLE WITH FIRST RADIATION BEAM PULSE HAVING INTENSITY PATTERN IN PREDETERMINED ALIGNMENT WITH SILICON LAYER
1030
CONTINUOUSLY TRANSLATE SAMPLE ALONG COLUMN WHILE SAMPLE IS BEING IRRADIATED WITH BEAM PULSE
1035
1050
TRANSLATE SAMPLE SO THAT THE BEAM IS POINTED TO THE NEXT COLUMN FOR LATERAL SOLIDIFICATION PROCESSING
YES
ARE MORE COLUMNS OF SAMPLE TO BE IRRADIATED FOR LATERAL SOLIDIFICATION PROCESSING?
NO
1045
SHUT OFF RADIATION BEAM AND HARDWARE
1055
STOP

F I G. 15B

INTERNATIONAL SEARCH REPORT

In   nal Application No
PCT/US 01/12799

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/268

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 01 18855 A (UNIV COLUMBIA) 15 March 2001 (2001-03-15) abstract; figure 1	13-24,26
X	US 6 117 752 A (SUZUKI KOUJI) 12 September 2000 (2000-09-12)	13-24,26
A	column 3, line 45 -column 5, line 36	1-12,25
A	US 5 145 808 A (SAMESHIMA TOSHIYUKI ET AL) 8 September 1992 (1992-09-08) column 2, line 3 - line 58; figure 1	1-26
A	WO 01 18854 A (UNIV COLUMBIA) 15 March 2001 (2001-03-15) figure 5	1-26

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 December 2001	18/12/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Le Meur, M-A

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	GB 2 338 342 A (LG PHILIPS LCD CO LTD ;LG LCD INC (KR)) 15 December 1999 (1999-12-15) abstract; figure 12 column 7, line 5 - line 16 ---	1-26
A	NEBEL C E: "LASER INTERFERENCE STRUCTURING OF A-SI:H" AMORPHOUS SILICON TECHNOLOGY - 1996. SAN FRANCISCO, CA, APRIL 8 - 12, 1996, MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS. VOL. 420, PITTSBURGH, PA: MRS, US, vol. 420, 8 April 1996 (1996-04-08), pages 117-128, XP000871547 ISBN: 1-55899-323-1 figure 2 ---	1
A	JEON J-H ET AL: "Two-step laser recrystallization of poly-Si for effective control of grain boundaries" JOURNAL OF NON-CRYSTALLINE SOLIDS, NORTH-HOLLAND PUBLISHING COMPANY, AMSTERDAM, NL, vol. 266-269, May 2000 (2000-05), pages 645-649, XP004198581 ISSN: 0022-3093 abstract -----	1-26

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 01/12799

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
WO 0118855	A	15-03-2001	AU	7084800 A	10-04-2001
			WO	0118855 A1	15-03-2001
US 6117752	A	12-09-2000	JP	11064883 A	05-03-1999
US 5145808	A	08-09-1992	JP	2973492 B2	08-11-1999
			JP	4102311 A	03-04-1992
WO 0118854	A	15-03-2001	AU	7573600 A	10-04-2001
			WO	0118854 A1	15-03-2001
GB 2338342	A	15-12-1999	NONE		

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☐ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: ______________________

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.